Vol. 8 Issue 05, May-2019

Performance Analysis of Interleaved Buck Converter for Switching & Conduction Losses for Femtocell Technology

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Abstract—This paper describes about a performance analysis of Interleaved Buck converter for switching and conduction losses for Femto Technology. The evolution of wireless broadband technology improves the data speed rates and coverage and avoids the web surfing of the network which can be done by using Femtocells without the need of the expensive cell towers [1]. In the hardware architecture of the femto cell, the DC-DC converter such as Buck converter plays a important role which used to convert from the higher voltage to lower voltage towards the supply side of the femto cell[2]. As this converter has the disadvantage of higher switching losses and increased inductor AC, reduction of efficiency, power density and power factor are also less[3]. In order to overcome from all these limitations, Interleaved buck converter has been introduced which has low switching losses & improves step down conversion ratio suitable for high input with the duty ratio of 0.4.A closed loop control is achieved by designing a digital PID controller to achieve the proper regulator for this converter[4]. As increasing the switching frequency but reduces the size of the components of the converter, therefore it become importance to reduce the switching losses. In this proposed paper the switching and conduction losses of both the transistor and the diodes of the Interleaved buck converter by using the PSIM software tool.

Index Terms - Femtocells, Interleaved Buck Converter, PID controller, Switching loss, Conduction loss, Power supply unit

INTRODUCTION

In cellular network communications, the high-speed coverage connection and generation of large traffic data of the network has been consumed by many services like web surfing, video streaming, email downloading, image downloading and video calls. The attenuations of the walls, multiple losses, scattering of the spectrum analysis are the primary problem for the poor cellular network communication [1]. The main challenge of the operators is to provide the good indoor coverage in cost effective manner with excellent network strength. The invent of the femtocells help to reduce the cell phone traffic which is soon riding on the consumers broadband line[2]. The poor coverage slows down the high speed data rates and reduces the quality of video and voice applications. But these cells has a disadvantage of high capital cost, leased back haul of increases the electricity bills etc. Hence all these problem has lead to the solution of the cost effective technology which is a Femtocell[3].

A small box that plugs into the users existing broadband internet connections and works with the existing mobile networks is a Femtocell. These femto cells are fully featured, short range mobile phone base station has been evolved in

order to avoid the existing problems like lack of indoor coverage and low data rates[4]. It is a low power base station with the low power range can be deployed in residence, office and enterprise applications. The main difference between the base station and femtocell is the radius of base station and femtocells are 20-30meter and 10 meter respectively[5]. The plug and play capability of the femtocells helps the user for the easy installation and usage. It provides excellent mobile coverage and data speed at home, office, and public areas for both voice and data. For 3G, 4G or Long term Evolution these Femto cells has been developed and approaching to NextGen i.e 5G by 2020 for better enhancement and data speed rates with multiple access[6].

There are many four types of small cells namely, the first one is Femtocells which is closed access with the 4-8 users are operating within the radius of 10m[7]. The second one is Metrocells which is hybrid/open access with the 8 -32 users can be operated with the radius range of 200m. The third one is Pico or Micro cells which is a open access with the 32 -more than 100 users[8]. The fourth one is Macrocell which is a open access with more than 1000 users. The femtocell can be classified into three cells i.e Home cell, Enterprise cell and Metro cells[9]. It supports 4 users in a residential setting & 4 to 32 users in enterprise cell, 16 users in metro cells[10]. The different types of femtocell is as shown in the figure 1.2(a)(b)(c).



Fig 1.2(a): Front and back view of Femtocell



Fig 1.2(b): Different types of Metro Femtocell

ISSN: 2278-0181

Vol. 8 Issue 05, May-2019



Fig1.3: Various components of Femtocell

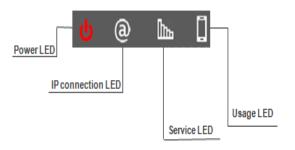


Fig1.4: Significance of LED of Femtocell

2. HARDWARE ARCHITECTURE OF FEMTOCELL TOWARDS SUPPLY SIDE

The components present in the hardware architecture of the femtocell are namely, DC -DC converter as Buck converter, PWR switching, Power Over Ethernet (POE) and PMIC chip which manages all the associated elements for the processing of the operations [1]. The block diagram of Femtocell towards supply side is as shown in Fig2.

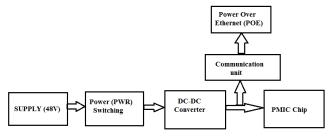


Fig 2: Block Diagram of FEMTO cell towards supply side

- Supply: The primary function of a power supply is to convert electric current from a source of 48V for enterprise cell and 12V for home cell which delivers power to the load [2].
- Power (PWR) Switching: Power switching is a Switch Mode Power Supply (SMPS) is an electronic power supply that incorporates a switching regulator to convert electrical power more efficiently.
- DC-DC Converter: A DC-to-DC converter is an electronic circuit that converts a source of direct current (DC) from one voltage level to another. A buck converter (stepdown converter) is a DC-to-DC power converter which steps down voltage from its input (supply) to its output (load). It has a input voltage of 12V converts into the output voltage of 5V efficiently which extends prolonged battery life, reduces heat dissipation.
- Power Over Ethernet (POE): Power over Ethernet or POE is a standard system which pass electric power along with

data on twisted pair Ethernet cabling. This allows a single cable to provide both data connection and electric power to devices such as wireless access points like LAN port.

PMIC: They are integrated circuits for managing power requirements of the system. It is often included in battery-operated devices such as mobile phones and portable media players to decrease the amount of space required. Power management ICs are solid state devices that control the flow and direction of electrical power[5]. It has a ability to perform some basic electrical functions including voltage conversion, voltage scaling, power source selection. It is equally suitable for DC-to-DC conversion on board without losing the bit of accuracy and quality of the signal. It is used for individual power conversion, where more than one function can be employed on the single IC based on the nature and quality of the product they are going to be installed. These Integrated chips help in reducing the number of components required to perform number of functions on a single chip[6].

3. METHODOLOGY OF SWITCHING & CONDUCTION LOSSES OF INTERLEAVED BUCK CONVERTER

In the supply side of the Femtocell has a buck converter which converts from higher voltage of 12V to a lower voltage to 5V but this converter has a limitations of higher switching losses and reduces efficiency. In order to overcome from this limitations, the interleaved buck converter are introduced which provides a high efficiency, less output current ripple, simple in structure and operates with high switching frequency. The word 'Interleaving' refers to paralleling which shares the power flow between two or more conversion chain and helps to minimize the input current ripple and increases efficiency on the converter. Switching losses are "Frequency" dependent where as the conduction losses coincides with the interval in which power is being processed hence it is "Duty ratio" dependent.By understanding the sequence events of switching during each transition and quantifying the losses associated with each event become a key expectation of any power supply designers. Higher the switching frequency, greater the no. of times the switch changes state per second i.e. losses proportional to switching frequency of the converter. As the switching frequency increases but reduces the size of the components of the converter. Hence it become importance to reduce the switching losses. The block diagram of closed loop of Interleaved buck converter is as shown in the Fig 3. It is mainly consists of following

- DC supply: The function of the DC supply is to provide 12V DC like battery which gives power for the operation of the converter.
- Design and development of Interleaved converter: This converter shares the power flow between two or more conversion chain which helps to minimize the input current ripple and to achieve high efficiency on the converter. It implies a reduction in the size, weight and volume of the inductors and capacitors.
- Due to the simple structure and low control complexity of interleaved buck converter, it is used in applications where non isolation, step down conversion ratio, high output current with low ripple is required[3].

- Design and development of PID Controller: To meet the steady state stability by minimizing the transients in the initial conditions. It avoids the fluctuations and ripple present in the output voltage.
- Design and loss analysis of this Converter: Switching losses are "Frequency" dependent where as the conduction losses coincides with the interval in which power is being processed hence it is "Duty ratio" dependent. Both these losses can be estimated in PSIM software tool.

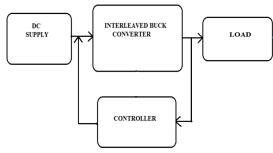


Fig 3: Block diagram of closed loop of Interleaved buck converter for the Femto cell technology

4. POWER LOSSES IN SWITCHES

Power loss generated in the switch is the product of the current through the switch and voltage across the switch. When the switch is ON, it has a current of (Vs/Rl) but there is no voltage drop hence no power loss.. The circuit diagram of the power switch is closed which connecting to the resisitive load is shown in the figure 4.1 The equation of the current and the voltage when the switch is closed is given by Isw(closed) = I load and Vsw (closed) = 0. Hence power absorb by the switch is given by P closed = Vsw (closed)* I sw(closed) = 0. When the switch is OFF, there is no current through it (no Vs across it) hence there is no power dissipation. The circuit diagram of the power switch is open which connecting to the resisitive load is shown in the figure 3.8. The equation of the current and the voltage when the switch is open is given by Isw(open) = 0and Vsw (open) = V source. The power absorbed by the switch is given by P open = Vsw (open)* Isw(open) = 0. Hence the total power loss in the switches is given by P loss = P closed + P open = 0 thus the switching loss & conduction loss are zero.

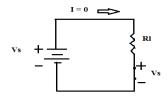


Fig 4.1: Circuit Diagram of the Power switch is closed

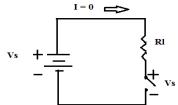


Fig 4.2: Circuit Diagram of the Power switch is open

Ideally the fall & rise time of the switch (i.e on time & off time of switch) are zero. Ideal switches have zero on-state drop, hence no conduction losses i.e conducting forward drop is zero. It has a zero leakage current hence there is no off-state losses. The turn on and turn off of the power switches transition are instantaneous thus there is no energy loss during switching transitions (Voltage collapse immediately & current rise immediately). When the switch is ON state, the voltage across the device is zero and when the switch is OFF state, the current flowing through the device is zero. The switching period is the time taken to change the from ON state to OFF state and vice-versa. The waveform of the voltage and the current in the ideal conduction is shown in the figure 4.1

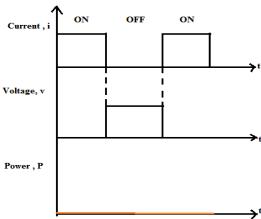


Fig 4.1: Waveform of the voltage and the current in the ideal conduction of switches

Practically the fall & rise time of the switch (i.e on time & off time of switch) are not zero. In this practical switching of the devices there is a finite forward drop presence hence conduction loss exists. There is a negligible leakage current & off state loss are also present in this practical switches. The turn on and turn off of the power switches transition are not instantaneous thus there is significant energy loss during switching transitions (Voltage does not collapse immediately & current rise does not immediately) When the switch is ON state, the voltage across the device is not zero and when the switch is OFF state, the current flowing through the device is not zero. The switching period is the time taken to change the from ON state to OFF state and vice-versa. Hence the switching losses and the conduction losses are present in the practical switches such that switching losses are greater than conduction losses. The waveform of the voltage and the current in the ideal conduction is shown in the figure 4.4

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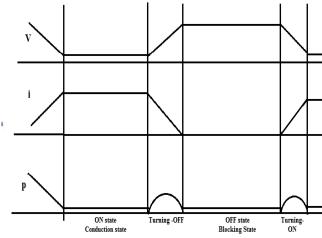


Fig 4.2: Waveform of the voltage and the current in the practical conduction

Total power loss of the power semiconductor devices is equal to the sum of the conduction loss or ON- state loss and switching losses i.e (turn on loss + turn off loss). For the switching operation of any device, power loss are mainly classified into two types namely

- Switching losses: It occurs when the device is transitioning from the blocking state to the conducting state and vice-versa. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the frequency to obtain the switching losses Switching losses occurs during turning on and turning off time of the devices.
- Conduction losses: It occurs when the device is in full conduction. The current in the device is whatever is required by the circuit and the voltage at its terminals is the voltage drop due to the device itself. These losses are in direct relationship with the duty cycle not on frequency dependent. The way to reduce conduction losses is by lowering the forward drops across the diode and switch

There are 4 extra nodes on each thermal module of IGBT than the normal IGBT. These 4 nodes are for the power losses, and theyare (from top to bottom)

- 1. Transistor conduction losses,
- 2. Transistor switching losses
- 3. Diode conduction losses
- 4. Diode switching losses.

They are in the form of electric currents, and flows out of these nodes in order to measure the losses values, connect an ammeter to each node.

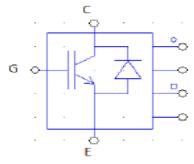


Fig 4.3: Thermal module of IGBT

5. CIRCUIT DIAGRAM OF INTERLEAVED BUCK CONVERTER FOR FEMTOCELL TECHNOLOGY

The Interleaved Buck Converter has low switching losses and improved step-down conversion ratio, which is suitable for the applications where the input voltage is high and the operating duty is below 50%. The voltage stress across all the active switches is half of the input voltage before turn-on or after turn-off when the operating duty is below 50%, the capacitive discharging and switching losses can be reduced. The circuit diagram of interleaved buck converter is as shown in the Fig 5.1. It consists of two active switches Q1 & Q2, inductors L1 & L2, diodes D1 & D2, capacitor C, resistor R load and the voltage source Vin.

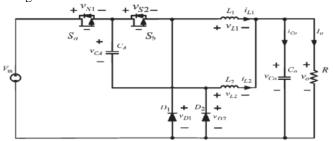


Fig 5.1: Circuit diagram of the Interleaved buck converter

The capacitor C should be large should be large enough in order to maintain the constant output voltage Vo. All the power semiconductors should be ideal in nature. The two inductors L1 & L2 should be same. Coupling capacitor helps to connects the two circuit which allows AC i.e high frequency and blocks DC i.e low frequency should be large which acts as a voltage source. The circuit diagram of interleaved buck converter consists of 4 modes namely

Mode 1 (t0 - t1): Mode 1 begins when Q1 is turned ON & D2 is Forward biased at to. The current iL1(t) flows through Q1, Cb & L1 and voltage of coupling capacitor Vcb is charged. The voltage across inductor L1 is VL1= Vs-Vcb-Vo (+ve value), hence iL1(t) increases linearly and voltage across inductor L2 is VL2= -Vo(-ve value),hence iL2(t) decreases linearly. The voltage across the switch Q2 and diode D1 are Vq2= Vs & Vd1= Vs- Vcb respectively. The circuit diagram of the mode 1 operation is shown in the figure 5.2. The equation obtained during the mode 1 operation is as follows

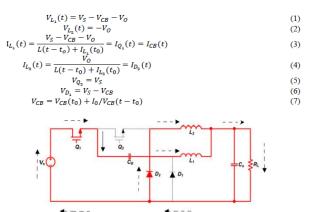


Fig 5.2: Circuit diagram for Mode 1 operation

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Mode 2 (t1 - t2): The Mode 2 begins when Q1 is turned OFF at t1. The currents iL1(t) and iL2(t) freewheels through D1 and D2 respectively. The voltage across inductor L1 and L2 are VL1(t) = VL2(t) = -Vo (-ve value) hence iL1(t)and II2(t) decreases linearly. The voltage across the switch Q1 and diode Q2 are Vq1(t) = Vs - Vcb and Vq2(t) = Vcbrespectively. The circuit diagram of the mode 2 operation is shown in the figure 5.3. he equation obtained during the mode 2 operation is as follows

$$V_{L_{1}}(t) = V_{L_{2}}(t) = -V_{0}$$

$$I_{L_{1}}(t) = I_{L_{1}}(t_{1}) - \binom{V_{0}}{L}(t - t_{1}) = I_{D_{1}}(t)$$

$$I_{L_{2}}(t) = I_{L_{2}}(t_{1}) - \binom{V_{0}}{L}(t - t_{1}) = I_{D_{2}}(t)$$

$$V_{Q_{1}}(t) = V_{S} - V_{CB}$$

$$V_{Q_{2}}(t) = V_{CB}$$

$$(11)$$

$$V_{Q_{2}}(t) = V_{CB}$$

$$V_{Q_{3}}(t) = V_{CB}$$

$$V_{Q_{4}}(t) = V_{CB}$$

$$V_{Q_{5}}(t) = V_{CB}$$

Fig 5.3: Circuit diagram for Mode 2 operation

.Mode 3 (t2 - t3): The Mode 3 begins when Q2 is turned ON at t2. The current iL1(t) freewheels through D1 and iL2(t) flows through D1, Cb, Q2 & L2. Thus Vcb is discharged. The voltage across inductor L1 is VL1= -Vo (-ve value), hence iL1(t) decreases linearly. The voltage across VL2=Vcb-Vo(+ve value),hence iL2(t) inductor L2 is increases linearly. The voltage across the switch Q1 and diode D1 are Vq1= Vs - Vcb & Vd1= Vcb respectively. The circuit diagram of the mode 3 operation is shown in the figure 5.4. The equation obtained during the mode 3 operation is as follow

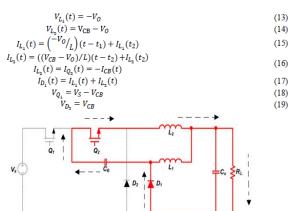


Fig 5.4: Circuit diagram for Mode 3 operation

Mode 4 (t3 - t4): Mode 4 begins when Q2 is turned OFF at t3, and its operation is same as Mode 2. The gate pulses given for the interleaved buck converter is shown in the figure 5.5

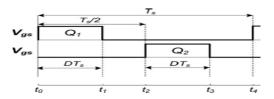


Fig 5.5: Gate pulses given for Interleaved Buck Converter

According to the design the inductor value is given by the equation $L = \frac{(Vs-Vo)}{diL^*} 2f^*D$ and L1 = L2 = L/2. The capacitor value is given by the equation C = (1-2D)/8*L*(dV/Vo)*(2*f)^2. The components value present in the circuit diagram is shown in the table 1

Table 1: Specification the components value according to the design

Sl.no	Name of the	Values
	parameter	
1.	Input Voltage	48V
2.	Output Voltage	12V
3.	Power Rating	30W
4.	Inductor L1 & L2	5uH
5.	Capacitor	470uF
6.	Switching frequency	100KHz
7.	Resistance	50ohm

6. LOSS CALCULATION BY USING PSIM SOFTWARE TOOL

The IGBT switching losses and conduction loss are calculated using Powersim (PSIM) software tool. PSIM provides a powerful and efficient environment to meet the simulation needs with he fast simulation and easy-to-use interface technology. In order to calculate these losses of IGBT, thermal module is required. Thermal Module is an additional option to the PSIM software which gives the information about the switching losses and conduction losses of transistor and diode of the semiconductor devices. It allows users to add more semiconductor device like mosfet, diodes specification of data sheet information into a database, and use these devices in the simulation for the loss calculation. Thermal Module provides a quick way of estimating device conduction losses and switching losses. For the simulation analysis of losses the CM1000HA-24H is a 1200V (VCE), 1000 Ampere Single IGBT Module Type has been selected for the thermal module is shown in the figure 6.1

ISSN: 2278-0181 Vol. 8 Issue 05, May-2019

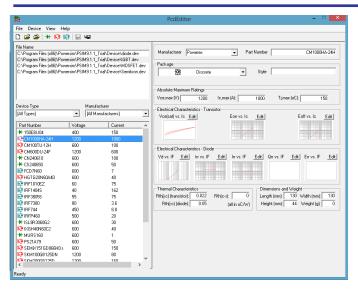


Fig 6.1: CM1000HA-24H IGBT Module Type selection for power loss calculation

7. SIMULATION RESULTS OF THE LOSS ANALYSIS OF THE INTERLEAVED BUCK CONVERTER

• Open loop simulation

The simulation circuit and result of the interleaved buck converter in open loop is as shown in figure 7.1(a)(b)(c)

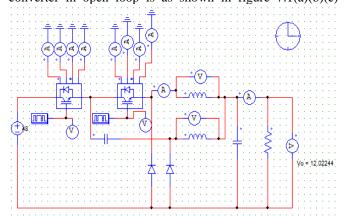


Fig 7.1(a): Open Loop Simulation of the interleaved buck converter

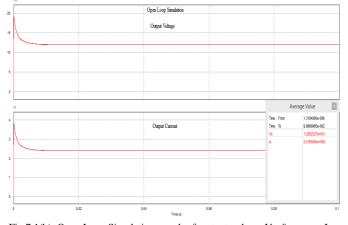


Fig 7.1(b): Open Loop Simulation $\,$ result of $\,$ output voltage Vo & current Io $\,$

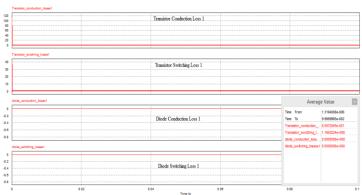


Fig 7.1(c): Open Loop Simulation result of Conduction & switching loss of diode and transistor of switch 1

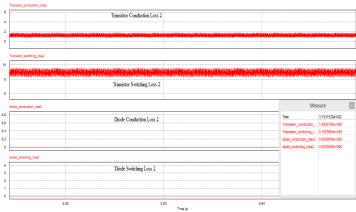


Fig 7.1(d): Open Loop Simulation result of Conduction & switching loss of diode and transistor of switch 2

• Closed loop simulation

The simulation circuit and result of the interleaved buck converter in closed loop is as shown in figure 7.2(a)(b)(c)

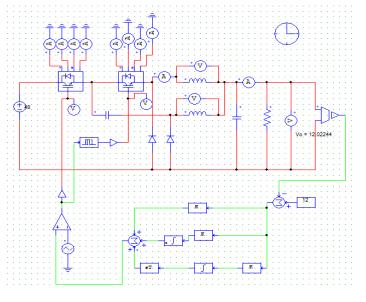


Fig 7.2(a): Closed Loop Simulation of the interleaved buck converter with PID controller

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ISSN: 2278-0181 Vol. 8 Issue 05, May-2019

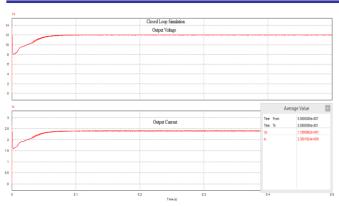


Fig 7.2(b): Closed Loop Simulation result of output voltage Vo & current

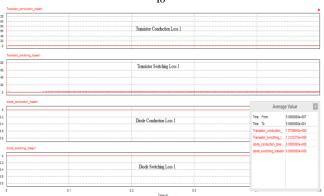


Fig 7.2(c): Open Loop Simulation result of Conduction & switching loss of diode and transistor of switch 1

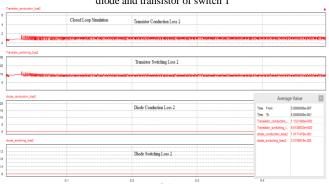


Fig 7.2(c): Open Loop Simulation result of Conduction & switching loss of diode and transistor of switch 2

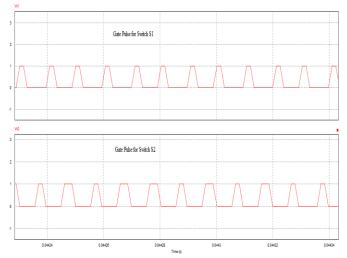


Fig 7.2(d): Gate pulse of switch S1 and switch S2

8. RESULTS AND DISCUSSION

The overall outcome of the interleaved buck converter for Femto cell is outlined as follows:

Table 2: Open Loop simulation loss analysis results of Interleaved Buck converter for femtocell technology

S	Parameters	Switch S1	Switch S2	Result
1.	Turumeters	5 witch 51	5 witch 52	values
n				
О				
1	Input Voltage Vin	-	-	48V
2	Output Voltage Vo	-	-	12.09V
3	Output Current Io	-	-	2.4A
4	Transistor conduction loss of switch S1	8.59A	1.49A	-
5	Transistor switching loss of switch S1	1.16A	8.19A	-
6	Diode conduction loss of switch S1	0	0	-
7	Diode conduction loss of switch S2	0	0	-

Table 3: Closed Loop simulation loss analysis results of Interleaved Buck converter for femtocell technology

S	Parameters	Switch	Switch S2	Result
1.		S1		values
n				
0				
1	Input Voltage Vin	-	-	48V
2	Output Voltage Vo	-	-	11.80V
3	Output Current Io	-	-	2.36A
4	Transistor conduction loss of switch S1	1.07A	1.13A	-
5	Transistor switching loss of switch S1	1.21A	8.61A	-
6	Diode conduction loss of switch S1	0	0.001017	-
7	Diode conduction loss of switch S2	0	0.0000257	-

- 1. In order to maintain output voltage constant wrt flautation of the input, PID controller has been used.
- 2. In the closed loop condition, the switching and conduction losses of transistor of switch S1 & S2 are less when compared to the open loop condition.
- 3. The efficiency of this converter for femtocell technology in open loop is 78% but in the closed the efficiency has increased upto 85%.
- 4. Interleaved refers to parellelling of the two circuits which reduces the input ripples of the voltage and current compared to conventional buck converter.
- 5.By using the thermal module of IGBT, the data sheet information can be added and analyze the switching and conduction losses of the transistor & diode

9. CONCLUSION

In this paper, the different types of small cells network used to strengthen the network connectivity along with the femtocell technology has been discussed. In order to reduce the input voltage ripple and to increase the efficiency interleaved buck converter is suitable for the supply side of the femtocell. The role of power electronics on the supply side of the femto cells

are discussed. The power loss analysis of the conduction & switching of both transistor and diode has been analyzed by selecting IGBT thermal of module has been discussed. Hence the comparison of the open loop and the closed operation loss analysis of the interleaved buck converter has been done with the increasing in the stability along with the dynamic performance by using PID controller has been achieved with the simulation results .

REFERENCES

- II-Oun Lee, Shin-Young Cho, and Gun-Woo Moon, "Interleaved Buck Converter Having Low Switching Losses and Improved Step-Down Conversion Ratio", IEEE Transaction on Power Electronics, Vol. 27, No. 8, August 2018.
- [2] Ashwini A. Patill, D. S. Chavan, "Comparative Analysis of Buck Converter and Modified Interleaved Buck Converter for Standalone Wind Energy System", International Journal of All Research Education and Scientific Methods (IJARESM) ISSN: 2455-6211, Volume 4, Issue 5, May- 2017.
- [3] Y. M. Chen, S. Y. Teseng, C. T. Tsai, and T. F. Wu, "Interleaved buck converters with a single-capacitor turn-off snubber," IEEE Trans. Aerosp. Electronic Syst., vol. 40, no. 3, pp. 954–967, Jul. 2016.
- [4] V. Chandrasekhar, J. G. Andrews and A. Gatherer, "Femtocell networks: A survey," IEEE Comm. Magazine, vol. 46, no. 9, pp. 59– 67, Sep. 2008.
- [5] A. Damnjanovic, J. Montojo, Y. Wei, T. Ji, T. Luo, M. Vajapeyam, T. Yoo, O. Song, and D. Malladi, "A survey on 3GPP heterogeneous networks," IEEE Wire. Com.
- [6] V. Chandrasekhar, J. G. Andrews, T. Muharemovic, Z. Shen and A.Gatherer, "Power control in two-tier femtocell networks," IEEE Trans. Wireless Commun., vol. 8, no. 8, pp. 4316–4328, Aug. 2009.
- [7] 3GPP TR 25.967 (Release 10), "Universal Mobile Telecommunications System (UMTS); Home Node B (HNB) Radio Frequency," pp. 1–56, 2011, version 10.0.0.
- [8] P. Xia, V. Chandrasekhar, and J. G. Andrews, "Open vs. closed access femtocells in the uplink," IEEE Trans. on Wireless Communications, vol. 9, no. 12, pp. 3798 – 3809, Dec. 2010.
- [9] D. Calin, H. Claussen, and H. Uzunalioglu, "On femto deployment architectures and macrocell offloading benefits in joint macro-femto deployments," IEEE Comm. Mag., vol. 48, no. 1, pp. 26–32, 2010.
- [10] H. A. Mahmoud and 'I. Guvenc", "A comparative study of different deployment modes for femtocell networks," in IEEE 20th Inter. Symp. on Personal, Indoor and Mobile Radio Commun., Tokyo, Japan., pp. 1–5, Sep. 2009.