Performance Analysis of Gate Driver Circuit for TFT – LCD

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Abstract

This paper presents Performance Analysis of Gate Driver Circuit for TFT-LCD. The output voltage of proposed Gate Driver circuit can be estimated as 40V by using Cadence, Microwind simulators. Measurement results indicate that better frequency response with reduced capacitive coupling effect by which driving speed of the gate driver circuit is improved.

Keywords: Gate driver circuit, capacitive coupling, TFT Switch.

I. Introduction

In past history of display technology having wide range like PMLCD, AMOLED, FPD, etc. but the AMLCD panels are widely used because of low cost, better uniform coverage, addressing and high driving capability [5]-[13]. Recently for getting better results display technology is used gate driver circuit. The conventional gate driver consists three major blocks inside it Shift register block, Level shifter block, Output Buffer block [8].

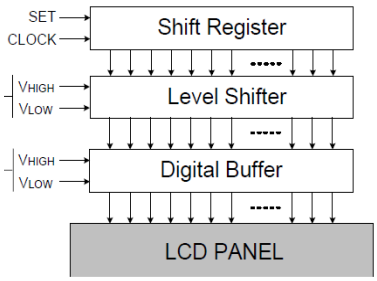


Fig.1 Conventional Gate Driver Circuit.

Gate driver circuit is used active addressing in AMLCD so it has to turn on TFT switches of each row in the form of a row by row succession, as mentioned above Gate driver having Shift Register for scan impulse voltage and pass them to the Level Shifter where input voltage level is decided as per requirement, Output Buffer reduce loading at output port and provide required high voltage signal [6]-[8]. By this voltage TFT switch is turn on and required applied voltage get available for rotating Liquid crystal Molecule the applied voltage should be larger than 10V. So one of major issue to design Gate driver circuit is that having high driving speed, high voltage performance. For that TFT's are used to design gate driver circuit but some problems are identified by references which are as Threshold voltage shift [2], Fluctuation in output voltage, Capacitive Coupling effect, Driving Speed, Power consumption, Life time of the Gate Driver[1]-[10].

In this paper the simulation results shows reduction in Capacitive Coupling effect, reduced fluctuation in output voltage, and high Driving speed is obtained, in comparison to reference work. On the basis of measured results proposed gate driver gives noteworthy performance for TFT-LCD panels.

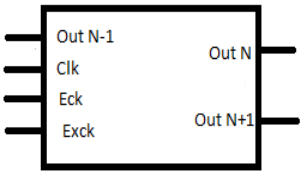


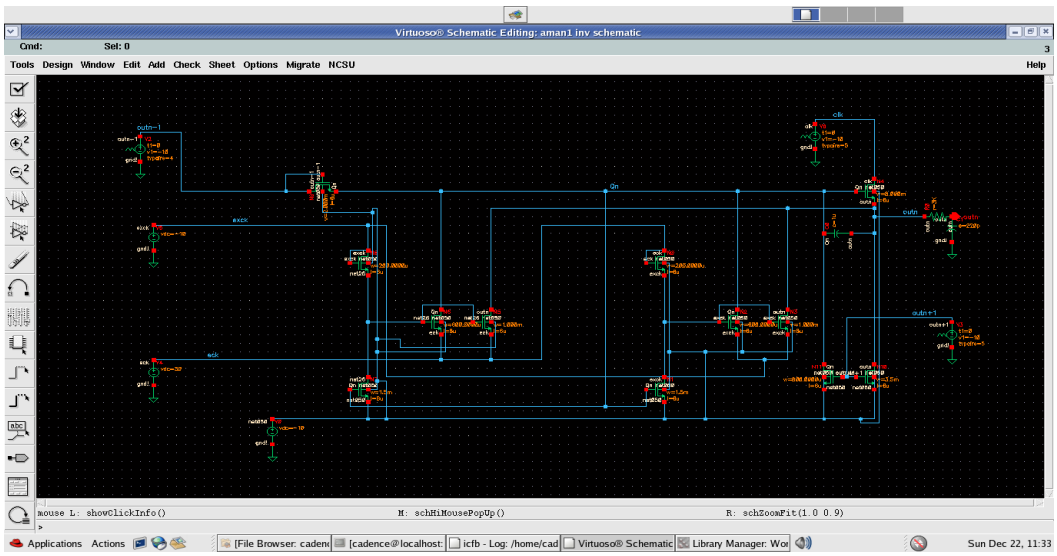
Fig.2 Single Stage Block of Gate Driver

II. Proposed Circuit Operation

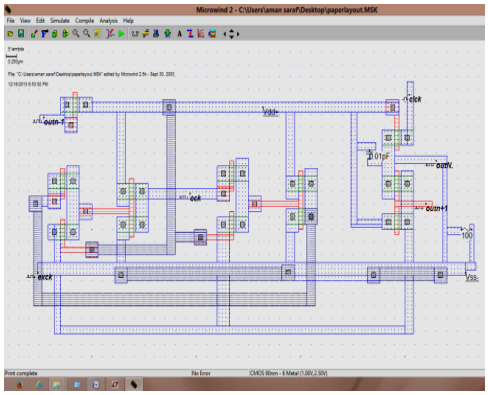
As shown in fig.2 three clocks are used two extended clock and one driving clock. Input is applied at out N-1, and output is calculated from out N port. This output voltage turns on TFT switches and charge the capacitor by which row lines are drive in the form of row by row succession[7]-[8], next row will receive input voltage from first row through discharging the capacitor [13].

Fig.3 shows schematic diagram, timing diagram, and layout diagram of the proposed gate driver circuit. Each stage of gate driver circuit consists of three types of clock signals (one driving clock, two extended clock), one pull-up network (N9, N4), one key pull-down network (N10, N11) and two alternative pull-down network (N8-N5 and N0-N3). Concept of gate driver is cleared through circuit operation. The input signal is applied at Out $_{(N-1)}$ it starts circuit. Here charging and discharging of Out $_{(N)}$ node is controlled by Q_N node. So Nth row line is received high voltage signal through Out $_{(N)}$ node, at this time Out $_{(N-1)}$ is discharged which enables next stage gate driver circuit.

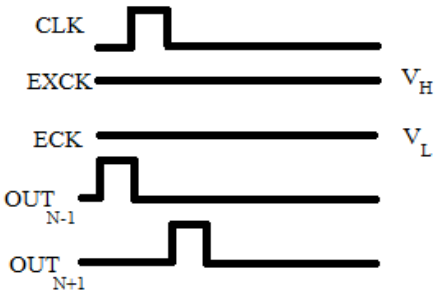
On the basis of reference work capacitive coupling effect and output fluctuation is a sevior problem due to charge trapping in a gate insulator at high gate voltage. To overcome this problem an AC driving method is used [8]-[10]. Alternative pull down network are used with gate capacitive coupling [2]-[10]. The driving speed can be improved by changing clk signal. The three main working steps are described below.



(a)



(b)



(c)

Fig.3 Proposed gate driver:
(a) Schematic diagram (b) Layout diagram (c) Timing diagram

As in step1, when high voltage input is applied at Out $_{N-1}$ node, the Q_N node becomes high and it turns on N7, N1. At this time Out $_N$ node becomes low through N4 because clk signal is low but the N7, N1 are turn on and they provide discharging path for N8,N0 to Vss through An, Bn node [13]-[14]. Due to this gate driver becomes free from any internal voltage which creates defects in output signal and output signal shows 40v swing without any fluctuation.

There is no high voltage available for N6, N5, N2, and N3, are then turned off. In the next step clk signal becomes high which boosted up Q_N node (V_H+ΔV) due to gate capacitor coupling of N4, which enhance the driving capability of N4. Therefore, row lines receive high voltage V_H through out_N node. In the next step Out $_{N+1}$ node becomes high and N10, N11 are turn on and discharge Q_N and Out_N nodes at Vss [8],[14].

Notably, while EXCK is still V_H and ECK is still V_L as in step 1, it turns on N2, N3 by which Q_N and Out_N nodes are maintain at Vss. Meanwhile reversed-bias stress in source nodes of N6, N5, Which receives a high voltage supply from the EXCK signal, facilitates recovery of ΔV_{TH}. Here ECK and EXCK signal suppress the excessive switching times of clock signals [14]. Therefore proposed gate driver circuit avoids the fluctuation in output waveform, and improves driving speed of the circuit.

Table.1

Sr.No.	Design Parameter	Reference Results	Proposed Results
1.	Design Technology	0.6µ	0.35µ
2.	Ton Time	50 µSec	25 µSec
3.	Duty Cycle	50%	33%
4.	Test Temperature	120^0C	135^0C
5.	Output Voltage Swing	39.2 V	40 V
6.	Capacitive coupling Effect	Yes	No
7.	Output Fluctuation	Yes	No

III. **Results and Discussions**

Fig.3 shows schematic diagram and layout diagram of proposed gate driver circuit. It uses 12 TFTs and one R-C loading. The result of proposed gate driver verified through cadence and Microwind simulator.

Fig. 4 (b) shows the output voltage exactly follows applied input signal and there is no fluctuation. Moreover, according to fig. 5(a) and fig. 5(b) internal capacitive effects are removed from output this is possible via adopting reverse biased method with two extended clock. As mentioned above circuit operation internal capacitive voltage is maintained at Vss through alternative pull-down network and the switching of pull-down network is controlled by extended clocks [14]. As shown in figures output of gate driver plot between voltage (v) and time (µsec.) i.e. time is being calculated in microsecond which indicate the driving speed of the gate driver is just double in comparison to reference work via changing the clock frequency. Circuit operates stably at 135^0C temperature. The improvements of proposed circuit are compared with previous work listed in table.1.

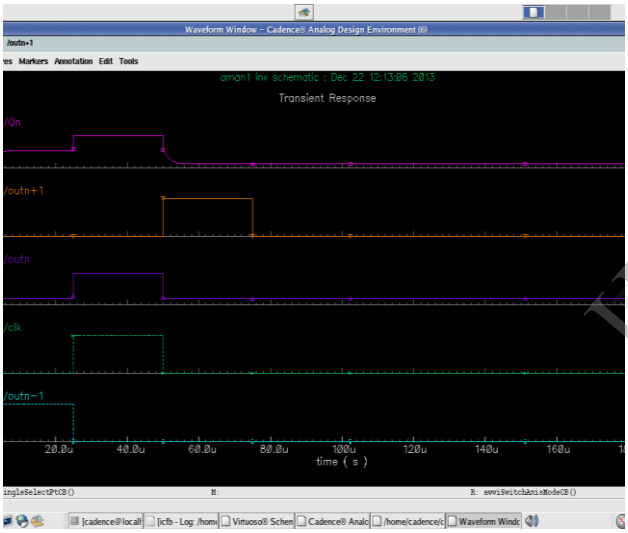


Fig. 4(a)

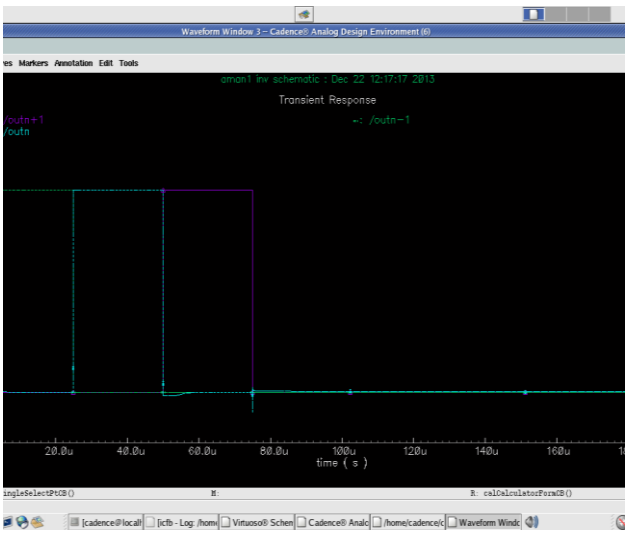


Fig. 4(b)

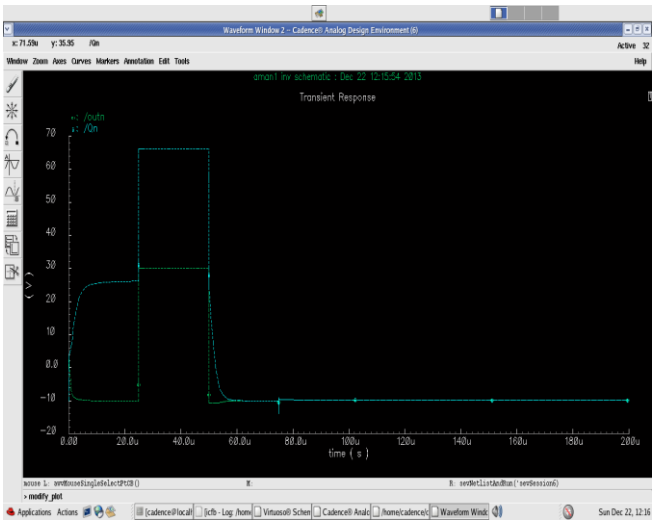


Fig. 5(a)

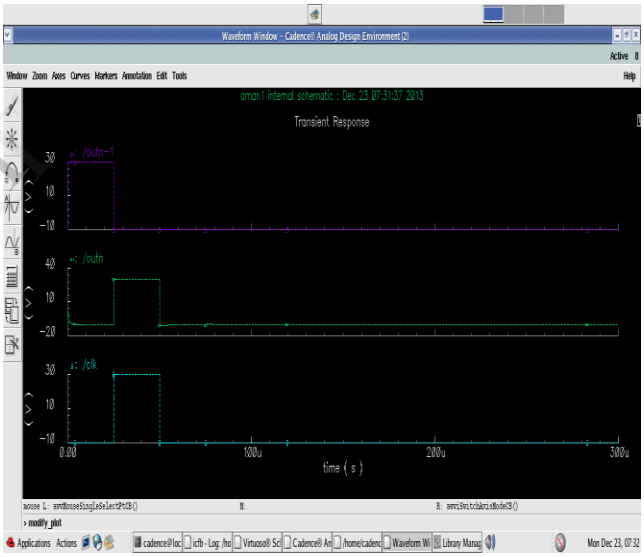


Fig. 5(b)

IV.Conclusion

This paper presents high speed gate driver circuit with no internal capacitive coupling effect due to this output voltage follows its input voltage. Proposed gate driver gives uniform output without fluctuation for large TFT-LCD, via using reverse biased method with change in clock frequency signal.

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