Performance Analysis of a New Single Stage AC-DC Converter for High Power Applications

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***Abstract*— Most of the power conversion equipment employs rectifiers that are made of diodes or thyristor to convert AC voltage to DC voltage before processing it. Such rectifiers produce very poor power factor with a large displacement factor and strong harmonic currents as these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage. Single phase PFC is used in the industry to convert ac mains to output dc voltage. This is the case with low power applications. But in high power applications, the ac-dc conversion consists of two steps-first ac is converted to an intermediate dc. This dc voltage is converted to the required value. The proposedconverter is a single stage converter with excellent input power factor, and with reduced number of semiconductor switches. This converter is a combination of the best features of both single stage and two stage converters. This converter consists of two controllers. One controller is used to control input power factor and the other one to regulate the output voltage. The operation of the proposed converter is confirmed with the results obtained from simulation.**

Key Words:Power factor correction, ac-dc conversion, full bridge converter,PWM technique, single stage converters.

I. INTRODUCTION

Power electronics is afieldthat deals with converting an available form of energy from a power source to the form required by a load. A power converter can be of semiconductor switches such as diodes, MOSFETs and IGBTs to achieve this power conversion. Different types of power converters are AC/DC converter, DC/DC converter, DC/AC inverter or AC/AC converter [3] depending on the application. Many types of power sources can be used for these converters, such as AC single phase, AC three-phase, DC source, battery, solar panel, or an electric generator.

For high power applications, the ac-dc converters [13] are implemented with two converter stages. The first stage is an ac-dc front [10] end boost converter stage that converts ac input voltage to dc intermediate voltage .The second stage is a dc-dc converter that converts this intermediate voltage to a required voltage. The proposed converter combines both PFC correction and dc-dc conversion. This converter has reduced size and cost is low.

Single stage converters are common for low power applications. But for high power applications, single stage full bridge converters are rarely used. This is because it is difficult for single stage converters to perform PFC [5] and dc-dc conversion simultaneously for wide load variations.

There are two types of single stage converters-current fed and voltage fed. In current fed single stage, there is a large input boost inductor [2] which causes ripples in output. But voltage fed converters have a large energy storage capacitor connected across the input section do not have this problem.

In two stage converters there are two controllers to control each section. That is each section has a controller to regulate its output. But the single stage converters consists of only one controller. Therefore there is no controller to regulate the dc bus capacitor voltage that is on the primary side of the main power transformer in the converter. Due to absence of this converter, the primary side dc bus voltage can vary significantly with line and load conditions and it is difficult to shape the input current. This is the problem with all the previously proposed converters for high power applications.

There are many previously proposed converters like [7] resonant converters. But these converters have problems with designing, tuning of the resonant converters and with the size of magnetic components. There are many dc bus capacitor voltage reduction techniques. Each dc bus voltage reduction method tries to affect the dc bus energy equilibrium in some way and all these reduction techniques has it disadvantages also.

These dc bus voltage reduction techniques include the use of very low values of output inductance, using auxiliary windings taken from the main transformer primary to extend the converter's duty cycle , or operating the converter with a "semi-continuous" input current. Since one-controller single stage converters have no controller to actively shape the input current, simultaneous input PFC and dc/dc conversion can only be performed by keeping the converter duty cycle fixed over the entire input line cycle. PFC in this case can only be ensured if the input inductor is designed to be sufficiently small so that the input current is discontinuous for all converters operating conditions and naturally bounded by a sinusoidal envelope. Such small input inductance values, however, restrict the amount of load that the converter can operate with as the input current peaks are extremely high at very high loads and low ac line input. As a result, most single-stage PWM converters have a maximum load of less than 1 kW.Several one-controller single stage converters must operate with non-standard control techniques in order to be able to perform input PFC and dc/dc conversion simultaneously, but these techniques may be extremely sophisticated for many power electronics engineers. For example, the converters proposed in [17]–[20] cannot be

operated with conventional phase-shift PWM and, instead, must operate with PWM techniques that are unique to the converters. In addition to these drawbacks, many single stage converters have increased conduction losses.

A new voltage fed PWM ac-dc converter is proposed. It can work with excellent input power factor, standard and widely used control methods, continuous input and output current. Here bridgeless converter is used in the input section which reduces conduction losses.

The proposed converter is a combination of a single stage converter and a two stage converter. Performance approaches that of two stage converter and cost approaches that of single stage converter. In this converter there are two controllers-one to regulate the output voltage and one for the input section of the converter to regulate the dc bus capacitor voltage and actively shape the input current.

II. Operation of the Proposed Converter

The proposed converter combines an input section that consists of input inductors $L_{in1}$and L_{in2} and rectifying diodes D_1 and D_2 with a dc-dc section. Components D_1,$L_{in1}$and D_2, L_{in2} form a bridgeless input. Blocking diodes D_{b1} and D_{b2} are included to prevent any dc circulating current. A dc blocking capacitor, C_{b1} is connected in series with the transformer primary.

Of the proposed converter's two independent controllers, one is used to regulate the voltage across primary side dc bus capacitor C_b by sending appropriate gating signals to S_2 and S_4.The gating signals of $S_1$and S_3 are complimentary signals of S_2 and S_4respectively. The other controller is used to regulate the output voltage by setting an appropriate phase shift between the gating signals of S_2 and S_4.Based on the output signals from each controller; some simple logic can be used to develop the appropriate gating signal for each converter switch. Although the output signals of the two controllers are combined at the end of the gating signal generation process, the two controllers are independent of each other from the point of view of control.

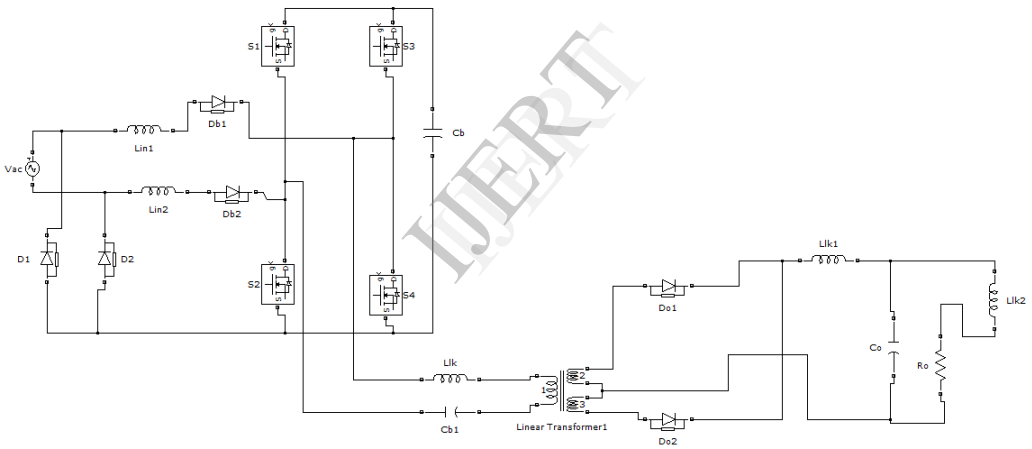

Fig 2.1 Proposed converter

III. Modes of Operation of the Proposed Converter

The converter's typical modes of operation are as follows:

Mode 1(t_0< t < t_1)*:*During this mode, the body diodes of switches *S*1 and *S*4, D_{S1} and D_{S4}, respectively, are conducting. A positive voltage of V_{bus}, is impressed across the transformer leakage inductance. This results in the transformer primary currentI_{pri}changing with a slope of

$$\frac{di_{pri}}{dt} = \frac{V_{bus}}{L_{lk}} \qquad (1)$$

WhereL_{lk} is the leakage inductance of the transformer referred to the primary side and V_{bus} is the dc bus voltage. The transformer primary current in this mode is given by

$$i_{pri}(t) = I_{pri}(t_0) + \frac{V_{bus}}{L_{lk}}(t - t_0) \text{for } (t_0 < t < t_1) \qquad (2)$$

Where$I_{pri}(t0)$ is the transformer primary current at time t_0. At time t_1, the transformer primary current reaches zero. The output inductor current during this mode is given by

$$i_{Lo}(t) = I_{L0}(t_0) + \frac{V_0}{L_0}(t - t_0) \text{for } (t_0 < t < t_1) \qquad (3)$$

Where L_o is the output inductor, V_o is the output dc voltage and $I_{Lo}(t0)$ is the current in the output inductor at

time t_0.Moreover, a positive voltage of $|V_M \sin \omega SuTk|$ is impressed across input inductor Lin1, and its current also starts to rise during this mode. V_M is the peak ac input voltage, $\omega Su$is the angular frequency of the input ac voltage and $T_k$is the k[th] switching cycle under consideration.

Mode 2($t_1 < t < t_2$)*:*At$t = t_1$, the current through the transformer primary reduces to zero, reverses, and starts flowing through switches $S1$ and $S4$. The transformer primary current during this mode is given by

$$i_{pri}(t) = \frac{V_{bus}}{L_{lk}}(t - t_1) \text{for } (t_1 < t < t_2) \quad (4)$$

The output inductor current during this mode is given by

$$i_{Lo}(t) = I_{Lo}(t_1) + \frac{V_0}{L_0}(t - t_1) \text{for } (t_1 < t < t_2) \quad (5)$$

At the end of this mode, the current in the transformer primary equals the current in the output inductor reflected on the transformer primary so that the freewheeling of the output inductor current ends at time t_2 such that

$$I_{pri}(t_2) = I'_{L0}(t_2) \quad (6)$$

Where$I'_{Lo}(t2)$ is the output inductor current reflected to the transformer primary.

Mode 3($t_2 < t < t_3$)*:*This is an energy transfer mode as energy is transferred from the dc bus to the output through the transformer. A positive voltage of V_{bus} is impressed across the series combination of the transformer leakage inductor. The transformer primary current during this mode is given by

$$ipri(t) = Ipri(t_2) + \frac{V_{bus} - NV_0}{N^2L_0 + L_{lk}}(t - t2) \text{for } (t_2 < t < t_3) \quad (7)$$

And the output inductor current reflected to the transformer primary is given by

$$i_{L0}(t)' = I_{L0}(t_2) + \frac{V_{bus} - NV_0}{N^2L_0 + L_{lk}}(t - t_2) \text{for } (t_2 < t < t_3) \quad (8)$$

Where N is the turns ratio of transformer primary and secondary turns..

Mode 4 ($t_3 < t < t_4$)*:*Att = t_3, the gate pulse of switch$S1$ reduces to zero and initiates the turn-off of switch $S1$.The current in the transformer starts charging and dischargingthe output capacitors of switches $S1$ and $S2$, C_{S1} and C_{S2},respectively. At the end of this mode, thebody diode of $S2$ starts conducting. The duration of this modes small enough so that the following relations hold.

$$I_{pri}(t_3) \approx I_{pri}(t_4) \quad \text{and} \quad I'_{L0}(t_3) \approx I'_{L0}(t_4) \quad (9)$$

From t_1 and t_4, a positive voltage of V_{bus} is incident across the magnetizing inductance L_M.

Mode 5($t_4 < t < t_5$):The voltage at the transformer primary reduces to zero at time t_4. During this mode, the currents in both the transformer leakage inductor and the output inductor start decreasing. The transformer primary current during this mode is given by

$$i_{pri}(t) = I_{pri}(t_4) + \frac{-NV_0}{N^2L_0 + L_{lk}}(t - t_4) \text{ for } (t_4 < t < t_5) \quad (10)$$

and the output inductor current reflected to the transformer primary is as follows:

$$i_{Lo}(t)' = I'_{Lo}(t_4) + \frac{-NV_0}{N^2L_0 + L_{lk}}(t - t_4) \text{ for } (t_4 < t < t_5) \quad (11)$$

Mode 6($t_5 < t < t_6$):At the beginning of this mode, at $t=t_5$, switch S_4 is turned off. The currents in the transformer and the input inductor Lin start charging and discharging the output capacitors of switches S_4 and S_3, C_{S4} and C_{S3}, respectively, to and from V_{bus}. At the end of this mode, the body diode of $S3$ starts conducting. The duration of this mode is small enough so that the following relations hold.

$$I_{pri}(t_5) \approx I_{pri}(t_6) \quad \text{and} \quad I'_{Lo}(t_5) \approx I'_{Lo}(t_6) \quad (12)$$

Mode 7($t_6 < t < t_7$):During this mode, the body diodes of switches $S2$ and $S3$, D_{S2} and D_{S3}, respectively, are conducting so that a negative voltage of V_{bus} is impressed across the transformer leakage inductance. This results in the transformer primary current I_{pri} changing with a slope of

$$\frac{di_{pri}}{dt} = -\frac{V_b}{L_{lk}} \quad (13)$$

So that the transformer primary current in this mode is given by

$$i_{pri}(t) = I_{pri}(t_6) - \frac{V_{bus}}{L_{lk}}(t - t_6) \text{ for } (t_6 < t < t_7) \quad (14)$$

WhereI_{pri} ($t0$) is the transformer primary current at time t_0. The output inductor current during this mode is given by

$$i_{Lo}(t) = I_{Lo}(t_6) - \frac{V_0}{L_0}(t - t_6) \text{ for } (t_6 < t < t_7) \quad (15)$$

Also, during this mode, a net negative voltage of ($|VM \sin \omega SuTk| - V_{bus}$) is impressed across input inductorL_{in1}, and its current also starts to fall during this mode.

Mode 8($t_7 < t < t_8$)*:*At$t = t_7$, the current through the transformer primary reduces to zero, reverses, and starts flowing through switches S_2 and S_3. The output inductor current still continues it's freewheeling, similar to Mode-7. The transformer primary current during this mode is given by

$$i_{pri}(t) = -\frac{V_{bus}}{L_{lk}}(t - t_7) \text{ for } (t_7 < t < t_8) \quad (16)$$

The output inductor current during this mode is as follows:

$$i_{Lo}(t) = I_{Lo}(t_7) + \frac{V_0}{L_0}(t - t_7) \quad \text{for } (t_7 < t < t_8) \tag{17}$$

At the end of this mode, the current in the transformerprimary equals the current in the output inductor that is reflected to the transformer primary so that the freewheeling of the output inductor current ends at time t_8 such that

$$|I_{pri}(t_8)| = I'_{Lo}(t_8) \tag{18}$$

Mode 9($t_8 < t < t_9$):This is another energy transfer mode as energy is transferred from the dc bus to the output through the transformer. A negative voltage of $-V_b$ is impressed across the series combination of the transformer leakage inductor and the equivalent output inductor reflected to the primary side. This causes the currents in transformer primary (in the direction opposite to that in Mode-3) and the output inductor L_o to rise during this mode. The transformer primary current during this mode is given by

$$i_{pri}(t) = I_{pri}(t_8) - \frac{V_{bus} - NV_0}{N^2L_0 + L_{lk}}(t - t_8) \tag{19}$$

and the output inductor current reflected to the transformer primary is as follows:

$$i_{Lo}(t)' = I'_{Lo}(t_8) - \frac{V_{bus} - NV_0}{N^2L_0 + L_{lk}}(t - t_8) \text{ for } (t_8 < t < t_9) \tag{20}$$

Mode 10($t_9 < t < t_{10}$)***:***At $t = t_9$, the gate pulse of switch S_2 reduces to zero and initiates the turn-off of switch S_2. At the end of this mode the body diode of S_1 starts conducting so that $S1$ can be turned on with ZVS. The duration of this mode is smallenough so that the following relations hold.

$$I_{pri}(t_9) \approx I_{pri}(t_{10}) \quad \text{and} \quad I'_{Lo}(t_9) \approx I'_{Lo}(t_{10}) \tag{21}$$

Mode 11($t_{10} < t < t_{11}$):The voltage at the transformer primary reduces to zero at time t_{10}. During this mode, the currents in both the transformer leakage inductor (in the direction opposite to that in Mode-4) and the output inductor start decreasing. The transformer primary current during this mode is given by

$$i_{pri}(t) = I_{pri}(t_{10}) + \frac{NV_0}{N^2L_0 + L_{lk}}(t - t_{10}) \quad \text{for } (t_{10} < t < t_{11}) \tag{22}$$

and the output inductor current reflected to the transformer primary is given by

$$i_{Lo}(t)' = I'_{Lo}(t_{10}) + \frac{NV_0}{N^2L_0 + L_{lk}}(t - t_{10}) \quad \text{for } (t_{10} < t < t_{11}) \tag{23}$$

Mode 12($t_{11} < t < t_{12}$):At the beginning of this mode, at $t = t_{11}$, switch $S3$ is turned off. The current in the transformerstarts charging and discharging the output capacitorsof switches $S3$ and $S4$, C_{S3} and C_{S4}, respectively, to andfrom V_{bus}. The duration ofthis mode is small enough so that the following relation should

$$I_{pri}(t_{11}) \approx I_{pri}(12) \quad \text{and}$$

$$I'_{Lo}(t_{11}) \approx I'_{Lo}(t_{12}) \quad \text{where } t_{12} = T_{sw} + t_0 \tag{24}$$

During this mode, a net negative voltage of ($|VM \sin \omega SuTk| - V_{bus}$) remains impressed across theinput inductor Lin1 and its current continues to fall during this mode.From $t10$ to $t12$, the primary current remains at $-(\varphi/2\pi)(V_{bus}TSw/LM)$.

IV. Converter Design

A. Minimum Input Inductor Value

Since the proposed converter is an ac–dc PFC converter that operates with continuous input current, the minimum value of input inductor that will ensure that the input inductor current is continuous over the entire operating range can be determined using the same equations as those used for equations standard PFC converters.

$$\frac{V_M}{I_M} \leq \frac{2L_{in}}{T_{sw}} \tag{25}$$

Where V_M is the peak input ac voltage and I_M is the peak input ac current. This equation is applicable to any ac–dc PFC converter operating with continuous input current. For the purpose of analysis, it can be considered to be a lossless resistance such as

$$R_e = \frac{V_M}{I_M} = \frac{V^2_M}{2P_o} \tag{26}$$

B. DC Bus Capacitor Design

The dc bus capacitor is designed in the same manner as it would be for a conventional two-stage converter. The minimum value of the dc bus capacitor to satisfy this condition for the given converter specifications can be calculated as

$$C_b = \frac{P_o}{4\pi f_{line,min} V^2_{bus} \frac{(\Delta V_{bus} - \Delta I_l \times r_{ESR})}{V_{bus}} \eta_{min}} \approx 700\ \mu F \tag{27}$$

where

$$\Delta I_l = \frac{P_o}{\eta V_{bus}\sqrt{2}} \tag{28}$$

V. Experimental Results

The simulation is done with an input ac voltage $V_{in,ac}$= 85V. The simulation is done with:L_{in1}= L_{in2}= 80 μH, Lo = 2.5 μH, Co = 20mF.

The gating waveforms of all the converter switches are shown in Fig.6.1. It can be seen that the gating signals of each pair of switches $S1 - S2$ and $S3 - S4$ in a converter leg are complimentary to each other, and that the gating waveforms of S1 and S4 are displaced by a phase-shift.

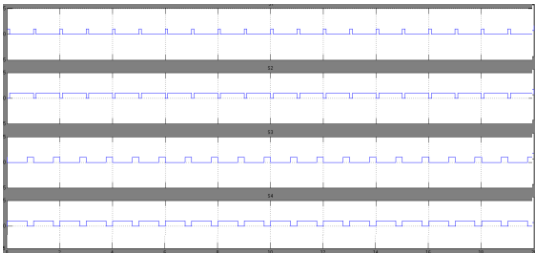

Fig 6.1 Gating Signals

The input voltage waveform obtained is shown in Fig.6.2.It can be seen that the input voltage is 85V AC. A pure sinusoidal input supply is given to the circuit. The sinusoidal signal is shown in Fig 6.2through scope.

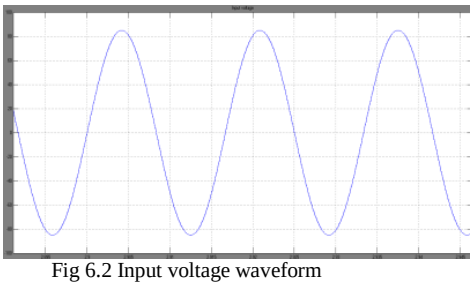

Fig 6.2 Input voltage waveform

The output voltage waveform obtained is shown in Fig.6.3. From the output waveform it can be seen that the output is pure DC. The output voltage=15.36V.

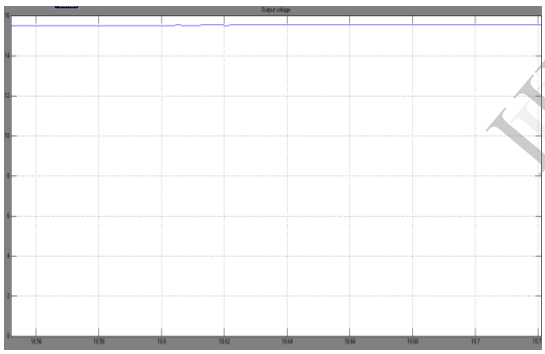

Fig 6.3 Output voltage waveform

The voltage across the inductance Lin 1 is shown in Fig.6.4. A voltage measurement is connected across the input inductance and the voltage is verified using scope.

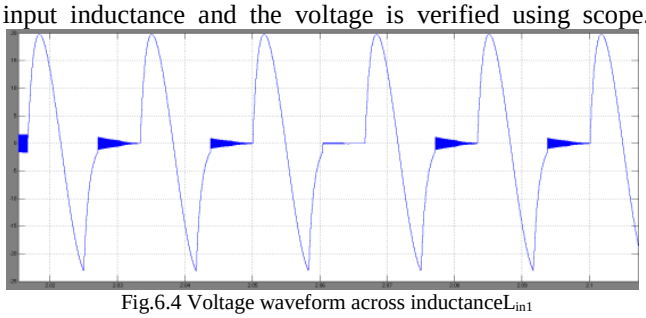

Fig.6.4 Voltage waveform across inductanceL_{in1}

VI. CONCLUSION

A new single stage ac-dc converter with two controllers is developed for high power applications. The proposed converter has reduced size, low cost and excellent input power factor. The complexity in designing the converter for high power applications is also reduced .The new converter is implemented using two controllers-one is used to actively control input power factor and the intermediate bus voltage, the other is used control output voltage. This converter is a combination of both single stage and two stage converters. The bridgeless PFC topology removes the input rectifier conductionlosses and is ableto achieve higher efficiency.

REFERENCES

[1] A.F. Souza and I. Barbi, Jun. 1999, "High power factor rectifier with reduced conduction and commutation losses," in Proc. IEEE INTELEC ,pp. 8-1–8-5.

[2] A. Lazaro, A. Barrado, M. Sanz, V. Salas, and E. Olias, Feb. 2007, "New power factor correction AC-DC converter with reduced storage capacitor voltage,"IEEETrans.Ind. Electron., vol. 54, no. 1, pp. 384–397.

[3] B. Lu, R. Brown, and M. Soldanos, , Mar. 2005 ,"Bridgeless PFC implementation using one cycle control technique," in Conf. Proc. IEEE APEC, pp. 812–817.

[4] C.-M. Wan, C.-H.Lin, C.-H.Liu and T.-C. Yang, 2010 ,"High performance single-stage transformer-isolated AC-DC converter," in Proc. IPEC, pp. 131–136.

[5] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, Jan. 2008, "A single-stage AC-DC converter with high power factor, regulated bus voltage, and output voltage,"IEEE Trans. PowerElectron., vol. 23, no. 1, pp. 218–228.

[6] G. Moschopoulos and P. Jain, Feb 2005 ,"Single-phase single-stage power-factor corrected converter topologies," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 23–35.

[7] G. Moschopoulos, Dec. 2003, "A simple AC-DC PWM full-bridge converter with integrated power-factor correction," IEEE Trans. Ind. Electron., vol. 50,no. 6, pp. 1290–1297.

[8] G. Moschopoulos, M. Qiu, H. Pinheiro, and P. K. Jain, Apr. 2003 ,"PWM full-bridge converter with natural input power factor correction," IEEE Trans. Aerosp. Electron. Syst., vol. 39, no. 2, pp. 660–674.

[9] H. Ma, Y. Ji, and Y. Xu, Jun. 2010 ,"Design and analysis of single-stage power factor correction converter with a feedback winding," IEEE Trans. Power electron., vol. 25, no. 6, pp. 1460–1470.

[10] H. S. Athab and D. D.-C.Lu, May 2010, "A high-efficiency AC-DC converter with quasi-active power factor correction," IEEE Trans. Power Electron., vol. 25, no. 5, pp. 1103–1109.

[11] H.-F. Liu and L.-K. Chang, Jan. 2005 ,"Flexible and low cost design for a fly back AC-DC converter with harmonic current correction," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 17–24.

[12] H.-L. Cheng, Y.-C.Hsieh and C.-S.Lin, Feb. 2011, "A novel single-stage high-power-factor AC-DC converter featuring high circuit efficiency," IEEE Trans. Ind. Electron. vol. 58, no. 2, pp. 524–532.

[13] J. P. R. Balestero, F. LessaTofoli, R. C. Fernandes, G. V. Torrico-Bascopé, and F. J. M. de Seixas, , Mar 2012 ,"Power factor correction boost converter based on the three-state switching cell," IEEE Trans. Ind. Electron., vol. 59, no. 3,pp. 1565–1577.

[14] J. Zhu and A. Pratt, Jun. 2009, "Capacitor ripple current in an interleaved PFC converter," IEEE Trans. Power Electron., vol. 24, no. 6, pp. 1506–1514.

[15] M. Narimani and G. Moschopoulos, Sep. 2013, "A new single-phase single-stage three-level power factor correction AC-DC converter with phase-shift modulation," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3731–3735.

[16] M. Pahlevaninezhad, P. Das, J. Drobnik, P. Jain, and A. Bakhshai, , Aug. 2012, "A nonlinear optimal control approach based on the control-Lyapunov function for an AC-DC converter used in electric vehicles," IEEE Trans. Ind. Informat., vol. 8, no. 3, pp. 596–614.

[17] M. S. Agamy and P. K. Jain, Jun. 2009 ,"A three-level resonant single-stage power factor correction converter: Analysis, design, and implementation," IEEE Trans. Ind.Electron., vol. 56, no. 6, pp. 2095–2107.

[18] N. Golbon and G. Moschopoulos, Aug. 2012, "A low-power AC-DC single-stage converter with reduced DC bus voltage variation," IEEE Trans. PowerElectron., vol. 27, no. 8, pp. 3714–3724.

[19] P. Das, S. Li, and G. Moschopoulos, Dec. 2009, "An improved AC-DC single-stage full-bridge converter with reduced DC bus voltage," IEEE Trans. Ind.Electron., vol. 56, no. 12, pp. 4882–4893.
[20] P. Kong, S. Wang, and F. C. Lee, Jan. 2008, "Common mode EMI noise suppression for bridgeless PFC converter," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 291–297.
[21] PritamDas ,MajidPahlevaninezhad , Gerry Moschopoulos, Nov.2013, "Analysis and design of a new ac–dc single-stage full-bridge PWM converter with two controllers" IEEE transactions on industrial electronics, vol. 60
[22] Q. Zhao, F. C. Lee, and F.-S. Tsai, Jul. 2002 ,"Voltage and current stress reduction in single-stage power factor correction AC-DC converters with bulk capacitor voltage feedback," IEEE Trans. Power Electron., vol. 17, no. 4,pp. 477–484.
[23] R. Liu and C. Q. Lee, 1992 ,"A unified approach to the design of resonant power factor correction circuits," in Conf. Rec. IEEE PESC , pp. 181–188.
[24] H.-J. Chiu, Y.-K. Lo, H.-C. Lee, S.-J.Cheng, Y.-C.Yan, C.-Y.Lin,T.-H. Wang, and S.-C. Mou, Jun.2010 "A single-stage soft-switching fly back converter for power-factor-Correction applications," IEEE Trans. Ind. Electron.,vol. 57, no. 6, pp. 2187–2190.

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