

# Performance Analysis of a Multilevel Inverter-Fed BLDC Motor Drive using MATLAB/Simulink

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**Abstract**—Brushless DC (BLDC) motors are widely used in industrial drives, electric vehicles, and household appliances due to their high efficiency, precise speed control, and low maintenance requirements. However, their performance is strongly influenced by the quality of the supply voltage. Traditional two-level inverters introduce significant voltage harmonics and electromagnetic interference, which degrade torque characteristics and increase motor losses. To address these limitations, this work presents the design and simulation of a multilevel inverter-fed BLDC motor drive system.

In this study, a cascaded H-bridge multilevel inverter topology is employed to synthesize a staircase output voltage with reduced harmonic distortion and lower  $dv/dt$  stress. The proposed architecture enables improved voltage resolution, better waveform quality, and enhanced dynamic response when compared to conventional inverter drives. The BLDC motor is modeled using its back-EMF profile, switching logic, and torque-speed characteristics, while the inverter is analyzed through switching functions and pulse-width modulation strategies. MATLAB/Simulink is used to evaluate system behavior under various loading and speed conditions.

Simulation results demonstrate significant improvements in total harmonic distortion (THD), torque ripple minimization, and efficiency of the BLDC drive. The multilevel inverter also allows smoother commutation and reduced switching losses, making it a suitable choice for medium- and high-performance applications. Overall, the study verifies that multilevel inverter technology provides a reliable and energy-efficient solution for modern BLDC motor drives.

**Index Terms**—BLDC Motor, Multilevel Inverter, MATLAB/Simulink, Total Harmonic Distortion, Cascaded H-bridge, Pulse Width Modulation.

## I. INTRODUCTION

### A. Background

BLDC motors combine the advantages of permanent-magnet synchronous machines with electronic commutation, resulting in high efficiency, high power density and good dynamic response. These motors are widely adopted in applications such as electric vehicles, aerospace actuators, industrial drives and household appliances where precise speed control, fast transients and reduced maintenance are essential.

Electronic commutation requires a power electronic inverter to generate properly timed three-phase voltages from a DC supply. Conventional two-level pulse-width-modulated (PWM) inverters are simple and cost-effective, but at medium and high power they exhibit significant drawbacks, including large

switching losses, high  $dv/dt$  at the motor terminals and substantial harmonic content in the output voltage and current. These factors can cause additional rotor heating, increased acoustic noise, torque ripple and reduced overall efficiency of the BLDC drive.

Multilevel inverters, such as diode-clamped, flying-capacitor and cascaded H-bridge topologies, have emerged as a promising alternative for high-power drives. By splitting the DC bus into multiple levels, these converters can generate staircase-like output voltages that more closely approximate a sinusoidal waveform, enabling lower total harmonic distortion (THD) and reduced voltage stress on each semiconductor switch. Among them, the three-level neutral-point-clamped (NPC) inverter is attractive because it doubles the effective voltage rating for a given device class and can be implemented with a relatively simple structure.

### B. Problem Outline

The demand for high-performance electric drives in industrial, commercial and transportation sectors has accelerated the adoption of brushless DC (BLDC) motors because they offer high efficiency, high power density, and superior dynamic response compared with conventional induction and brushed DC machines. These advantages make BLDC drives attractive for applications such as CNC machines, robotics, electric vehicles, renewable-energy systems and household appliances, where precise speed control, compact size and reliability are critical. Despite these benefits, the overall performance of a BLDC drive depends strongly on the quality of the power electronic interface used to convert DC supply into controlled three-phase voltages.

In most existing BLDC drives, a conventional two-level voltage source inverter (VSI) is used in combination with pulse-width modulation (PWM) techniques to generate the required phase voltages. While two-level VSIs are relatively simple and cost-effective, they exhibit several inherent drawbacks when used in medium and high-power applications. The switching devices must block the full DC-link voltage, which either restricts the usable voltage level or necessitates higher-rated, more expensive devices. In addition, the two-level switching action causes steep voltage transitions (high  $dv/dt$ ) and produces square-like output waveforms with significant low-order and high-frequency harmonics. These harmonics

increase copper and core losses in the motor, generate torque ripple and acoustic noise, and can lead to additional insulation stress and electromagnetic interference (EMI).

Attempts to mitigate these issues using higher switching frequencies or advanced PWM schemes can partially improve waveform quality, but they bring their own penalties. Increasing switching frequency raises switching losses and thermal stress in semiconductor devices, which reduces overall efficiency and complicates thermal management, especially at higher power ratings. Furthermore, practical constraints on device switching speed and gate-driver capability limit how far the switching frequency can be increased without compromising reliability. As a result, there is a clear need for a power-conversion approach that can provide high-quality output waveforms with reduced harmonic content and voltage stress, without excessively increasing the switching frequency or device count.

Multilevel inverter (MLI) topologies have emerged as a promising alternative for high-power motor drives because they synthesize an output voltage from several smaller DC steps, resulting in a staircase waveform that closely approximates a sinusoid. In three-level neutral-point-clamped (NPC) inverters, the DC bus is split into two equal halves, and clamping diodes allow each switch to block only half of the total DC-link voltage while still producing three distinct output levels at the phase terminals. This reduced voltage stress enables operation at higher DC-link voltages using devices with lower voltage ratings, improving efficiency and potentially lowering cost. The stepped line-to-line voltage also leads to lower total harmonic distortion (THD) in the motor currents, which decreases torque ripple, acoustic noise and additional losses in the BLDC machine.

Despite these advantages, integrating a multilevel inverter with a BLDC motor drive introduces challenges in terms of topology selection, DC-link voltage balancing, modulation strategy and control complexity. The gating signals must be carefully generated to maintain the neutral-point voltage, minimize harmonics and guarantee proper commutation of the BLDC motor phases based on rotor position. Different multicarrier sinusoidal PWM techniques such as in-phase disposition (IPD), phase-opposition disposition (POD) and alternative level-shifted strategies offer varying trade-offs between harmonic performance, switching frequency and implementation complexity. Therefore, a systematic investigation using detailed simulation is essential before moving towards hardware realization.

The specific technical problem addressed in this project is to evaluate whether a three-level NPC multilevel inverter, controlled by an appropriate multicarrier PWM strategy, can provide a superior power-conversion interface for BLDC motor drives compared with a conventional two-level VSI. The study must clarify how the multilevel structure influences phase-voltage quality, current ripple, electromagnetic torque profile and speed response of the BLDC motor under typical operating conditions. Additionally, the impact of multilevel switching on device voltage stress and potential reduction

in switching losses must be assessed qualitatively at the simulation stage, forming a basis for quantitative THD analysis and efficiency estimation in subsequent phases of the work.

### C. Objectives

The primary objectives of the work are:

- 1) To study the operating principles, advantages and limitations of BLDC motors and multilevel inverter topologies with emphasis on the three-level NPC configuration.
- 2) To develop a detailed MATLAB/Simulink model of a three-phase diode-clamped multilevel inverter interfaced with a BLDC motor, including DC link, power switches, clamping diodes and commutation logic.
- 3) To implement a suitable multicarrier sinusoidal PWM strategy for the NPC inverter and generate gate pulses that produce three-level phase voltages with reduced harmonic content.
- 4) To analyze the simulated output line-to-line voltages, phase currents, electromagnetic torque and speed response of the BLDC motor under different operating conditions.
- 5) To compare qualitatively the expected harmonic performance and voltage stress of the multilevel drive with that of a conventional two-level inverter, forming a basis for quantitative THD and performance analysis.
- 6) To investigate the influence of key design parameters of the NPC multilevel inverter (DC-link voltage, carrier frequency, modulation index and load conditions) on BLDC motor performance using systematic simulation case studies.
- 7) To observe and interpret the quality of the simulated PWM gating signals and verify correct three-level switching sequences in each inverter leg, ensuring safe device operation and proper neutral-point clamping in the model.
- 8) To validate the correctness of the BLDC motor and inverter models by checking that simulated back-EMF waveforms, torque characteristics and steady-state speeds match the expected theoretical behaviour and rated values.
- 9) To organize all Simulink subsystems (source, DC link, multilevel inverter, PWM and commutation logic, BLDC motor and measurement blocks) in a modular and reusable form, so that the same model can be extended for advanced controllers and THD analysis.

### D. Proposed Model

The proposed method focuses on designing and simulating a three-level neutral-point-clamped multilevel inverter to feed a BLDC motor, using multicarrier sinusoidal PWM to generate three-level phase voltages with reduced harmonics and device stress. It also concentrates on integrating this inverter with a detailed BLDC motor model in MATLAB/Simulink to evaluate speed, torque and waveform quality under different operating conditions.

The proposed system is a three-phase BLDC motor drive fed from a three-level NPC voltage source inverter supplied by a rectified DC bus. The power stage consists of a three-phase diode bridge rectifier, DC link capacitors that split the DC bus into two equal halves, and a three-level NPC inverter leg per phase composed of four active switches and two neutral-point-clamping diodes. This configuration allows each device to block only half of the total DC link voltage while synthesizing three distinct output levels  $\{+V_{dc}/2, 0, -V_{dc}/2\}$  at each phase terminal.

On the control side, a multicarrier sinusoidal PWM scheme is adopted in which a sinusoidal reference for each phase is compared with two in-phase, level-shifted carrier signals to generate the gate pulses. This approach, often termed in-phase disposition SPWM, ensures that the switching sequence produces evenly distributed voltage steps, leading to reduced THD and improved quality of the line-to-line voltage waveform applied to the BLDC motor. A commutation logic block uses rotor position information (or ideal Hall signals in the simulation stage) to route the three-level phase voltages appropriately, ensuring correct electronic commutation of the BLDC machine.

Within MATLAB/Simulink, the system is implemented as interconnected subsystems representing the rectifier and DC link, NPC inverter legs, PWM and gating circuit, BLDC motor model and measurement scopes. The BLDC motor is modeled with its electrical and mechanical equations to capture the relationship between applied voltages, currents, torque and speed, enabling assessment of dynamic performance and torque ripple under multilevel excitation. The simulations concentrate on validating the correct operation of the PWM strategy and inverter switching sequence, as well as demonstrating acceptable speed response and qualitative harmonic improvement.

## II. LITERATURE REVIEW

### A. Simulation and Implementation of Multilevel Inverter Based BLDC Motor

Brushless DC (BLDC) motors are widely recognized in the literature for their high efficiency, compact construction, low maintenance and excellent dynamic response, which makes them suitable for high-power industrial and automotive applications. Earlier researchers, however, showed that when BLDC motors are driven by conventional two-level voltage source inverters, the drives suffer from high harmonic distortion, high  $dv/dt$ , rotor heating and increased switching losses, all of which degrade torque quality and overall system efficiency. To mitigate these issues, many works have proposed multilevel inverter (MLI) topologies—such as cascaded H-bridge, flying-capacitor and neutral-point-clamped structures—and demonstrated that increasing the number of voltage levels produces a stepped output that more closely resembles a sinusoid, resulting in reduced harmonic content and lower device voltage stress.

Ninu Joy et al. propose and implement a three-phase diode-clamped (neutral-point-clamped) multilevel inverter specifically feeding a BLDC motor, using multicarrier sinusoidal

PWM with in-phase disposition to generate the gate pulses. Unlike many earlier BLDC papers that either focused solely on simulation or used cascaded or DC-link multilevel structures, this work concentrates on a practical three-level NPC topology, clearly detailing the switching states, capacitor arrangement and device voltage sharing so that each switch blocks only half the DC-link voltage. The authors not only simulate the PWM circuit and three-level inverter in MATLAB/Simulink to obtain line-to-line voltages and verify reduced harmonics, but also design a hardware prototype.

### B. High-Performance Multi Level Inverter Drive of Brushless DC Motor

The literature consistently shows that BLDC motors are preferred in modern variable-speed drive applications because they provide high efficiency, high power density, low maintenance and fast dynamic response, especially when compared with induction and conventional DC motors. However, these advantages can only be fully realized when the power electronic interface supplies high-quality three-phase voltages with low harmonic content and precise speed control. Conventional two-level inverters, although simple, suffer from high  $dv/dt$ , considerable harmonic distortion and significant switching losses at higher powers, which translate into torque ripple, acoustic noise and reduced overall efficiency in BLDC drives.

The high-performance multilevel inverter drive by Yousif Al Mashhadany represents an important step towards BLDC-specific MLI research. In that work, a three-phase three-level inverter feeds a BLDC motor and is modulated using a discrete three-phase PWM generator to create a 12-pulse, three-level output, while a PID controller regulates the motor speed. The study carefully compares this proposed MLI-based scheme with a variable DC-link voltage control technique, showing that the multilevel PWM approach yields lower harmonic distortion, smoother torque and superior transient and steady-state speed response.

### C. Simulation of Multilevel Inverter Based BLDC Motor

Early work on BLDC motor drives mainly used conventional two-level inverters, which are simple but generate high  $dv/dt$  and significant harmonic distortion, leading to torque ripple, additional losses and electromagnetic interference. To overcome these drawbacks, researchers proposed multilevel inverter (MLI) topologies such as cascaded H-bridge, diode-clamped and flying-capacitor structures, which synthesize staircase voltages from several DC levels and thereby improve waveform quality while reducing device voltage stress.

Sudhakar et al. focus on the simulation of a multilevel inverter based BLDC motor drive, building on prior evidence that multilevel topologies and multicarrier PWM can deliver low-distortion output and enhanced performance compared with classical two-level inverters. In parallel, high-performance control strategies such as PID, vector control and intelligent regulators have been combined with MLIs to further enhance BLDC drive dynamics.

#### D. Two Level and Five Level Fed BLDC Motor Drive

In this context, Devi Kiran and Ramachandra Rao investigate BLDC motor operation under both a conventional two-level inverter and a five-level cascaded H-bridge (CHB) inverter. Their paper begins with a review of BLDC motor modelling, emphasizing that the trapezoidal back-EMF and electronic commutation make the motor particularly sensitive to the quality of the applied phase voltages. They then present the structure and switching states of a five-level CHB inverter built from two H-bridge cells in series per phase, and use sinusoidal PWM to generate appropriate gating signals so that the inverter output can assume five discrete voltage levels.

The key contribution of the base paper is this direct performance comparison between a standard two-level inverter-fed BLDC drive and a five-level CHB multilevel inverter-fed BLDC drive using the same machine model and operating conditions. Simulation results reported in the paper show that the five-level inverter produces a much smoother torque waveform, back-EMFs that more closely match ideal trapezoids, and improved speed characteristics, while significantly reducing current and voltage ripple compared with the two-level inverter.

#### E. Multilevel Inverter Drives for Induction and BLDC Motors

Several studies have shown that traditional three-phase converters for induction motors suffer from poor voltage and current quality, and that increasing switching frequency to improve waveforms leads to higher switching losses. Researchers therefore proposed multilevel inverter topologies, where the DC bus is split into several levels so each device blocks only a fraction of the total voltage while the output waveform becomes a stepped approximation of a sinusoid.

S. Flora Viji Rose highlights three-level neutral-point-clamped (NPC) inverters as a practical solution for medium-voltage drives because they reduce device stress and enable better dynamic performance comparable to DC drives. The paper implements and simulates a diode-clamped three-level multilevel inverter drive using multicarrier in-phase disposition PWM and open-loop  $V/f$  control, demonstrating via MATLAB/Simulink results that a three-level NPC inverter can deliver low-harmonic voltage and effective speed control.

### III. PROPOSED METHOD

#### A. Introduction

In high-performance variable-speed drives, the quality of the supplied voltage and current has a major impact on the efficiency, torque ripple and electromagnetic interference of a BLDC motor. Two-level inverters are simple but generate large  $dv/dt$  and high harmonic content, which is particularly problematic in high-power or medium-voltage applications. A five-level multilevel inverter (MLI) provides more voltage steps than a three-level or two-level converter, producing an output waveform that is closer to a sinusoid and further reducing THD, switching stress and acoustic noise. In this project, a five-level inverter topology is adopted and combined

with a suitable PWM-based speed-control scheme in MATLAB/Simulink to obtain a low-ripple, high-efficiency BLDC drive.

#### B. System Architecture

The proposed method employs a three-phase five-level multilevel inverter as the interface between the DC supply and the BLDC motor, so that each phase can apply five discrete voltage levels to the stator windings and thus approximate a sinusoidal waveform more closely than a two-level converter. The DC source is divided into multiple intermediate levels (using series capacitors or cascaded H-bridge cells), ensuring that each switch blocks only a fraction of the total DC-link voltage and thereby reducing device stress. A level-shifted multicarrier sinusoidal PWM scheme with four carriers per phase is used to select the appropriate voltage level at every instant, generating well-distributed switching pulses for the five-level inverter.

The system flow consists of:

- 1) A three-phase AC power supply is first converted to DC using a three-phase diode bridge rectifier, providing a unidirectional DC link for the drive.
- 2) A capacitor filter smooths the rectified DC voltage, reducing ripple and supplying a relatively constant DC input to the multilevel inverter.
- 3) The multilevel inverter (implemented with MOSFET switches) converts this filtered DC into stepped three-phase AC voltages with multiple levels suitable for driving the BLDC motor.
- 4) A microcontroller generates digital switching commands based on the desired speed and rotor position information.
- 5) These commands are passed through a gate-driver stage, which amplifies and isolates the signals to properly drive the MOSFET gates in the multilevel inverter, thus controlling the BLDC motor.

#### C. Pulse Width Modulation (PWM) Strategy

Pulse Width Modulation (PWM) is a widely used technique in inverters and motor drives for controlling the effective AC output voltage from a fixed DC source. It works by switching the power devices at a high carrier frequency and varying the duty cycle of the pulses so that the average value over each switching period follows a desired waveform, usually sinusoidal.

In sinusoidal PWM, a sine reference is compared with a high-frequency triangular carrier; the comparison decides when the switches turn ON and OFF, and the modulation index directly controls the RMS output voltage and therefore the motor speed and torque. This approach greatly reduces low-order harmonics compared with square-wave operation, improving power quality, reducing filter size and lowering motor losses. In multilevel and BLDC drives, multicarrier sinusoidal PWM extends the same concept using several level-shifted carriers, enabling stepped multi-level voltages with significantly lower THD and higher overall efficiency.

The control strategies for generating these patterns involve:

- **Carrier-based sinusoidal PWM:** Uses multiple level-shifted triangular carriers (four for a five-level leg) compared with a sinusoidal reference. Variants include in-phase disposition (IPD), phase-opposition disposition (POD), and phase-shifted carrier (PSC).
- **Multicarrier optimized SPWM:** Uses modified carriers (e.g., trapezoidal or amplitude-modulated carriers) or optimized switching sequences to reduce THD and switching losses further compared with basic SPWM.
- **DC-link balancing control:** Adds closed-loop control or auxiliary circuits to keep intermediate capacitor voltages equal, preventing over-voltage and maintaining correct step levels.

#### IV. MATHEMATICAL MODELING

##### A. Introduction to the Model

A mathematical modeling of a multilevel inverter-based BLDC motor drive combines advanced power-conversion hardware with a high-efficiency machine to meet the growing demand for compact, precise and energy-efficient motion systems. When a BLDC motor is fed from a multilevel inverter operated with sinusoidal or space-vector PWM, the resulting reduction in current ripple and torque pulsations translates into smoother speed, higher efficiency and improved reliability.

The cascaded H-bridge (CHB) inverter relies on series-connected H-bridge cells to increment the voltage levels. For a five-level architecture, each phase has two identical H-bridge cells with DC sources  $V_{dc}$ .

For phase A, defining the switching functions  $s_{A1}$  and  $s_{A2} \in \{-1, 0, +1\}$  for cell 1 and 2 respectively:

- $s_{Ak} = +1 \implies$  cell output  $+V_{dc}$
- $s_{Ak} = 0 \implies$  cell output 0
- $s_{Ak} = -1 \implies$  cell output  $-V_{dc}$

The individual cell output voltages are:

$$V_{a1} = s_{A1}V_{dc}, \quad V_{a2} = s_{A2}V_{dc} \quad (1)$$

The total Phase-A voltage applied to the motor (line-to-neutral) is the arithmetic sum of the individual cell outputs:

$$v_a = V_{a1} + V_{a2} = (s_{A1} + s_{A2})V_{dc} \quad (2)$$

This summation inherently allows the phase voltage to take on five distinct levels:

$$v_a \in \{-2V_{dc}, -V_{dc}, 0, +V_{dc}, +2V_{dc}\} \quad (3)$$

Similarly, for phases B and C, the voltages are synthesized as:

$$v_b = (s_{B1} + s_{B2})V_{dc} \quad (4)$$

$$v_c = (s_{C1} + s_{C2})V_{dc} \quad (5)$$

Switching functions  $s_{Ak}$ ,  $s_{Bk}$ , and  $s_{Ck}$  are continuously governed by the multicarrier SPWM mechanism and the commutation logic.

##### C. BLDC Motor Dynamic Equations

The Y-connected BLDC stator voltage equations describe the per-phase electrical dynamics. Neglecting the mutual inductance between phases, the fundamental relations are:

$$v_a = R_s i_a + L_s \frac{di_a}{dt} + e_a \quad (6)$$

$$v_b = R_s i_b + L_s \frac{di_b}{dt} + e_b \quad (7)$$

$$v_c = R_s i_c + L_s \frac{di_c}{dt} + e_c \quad (8)$$

Where  $R_s$  is the stator resistance,  $L_s$  is the stator inductance,  $i$  represents phase currents, and  $e$  represents back-EMFs. For a star connection with no neutral wire, the current constraint is:

$$i_a + i_b + i_c = 0 \quad (9)$$

The back-EMFs are speed- and position-dependent, dictated by the trapezoidal flux distribution:

$$e_a = K_e \omega_m f_a(\theta_e) \quad (10)$$

$$e_b = K_e \omega_m f_b(\theta_e) \quad (11)$$

$$e_c = K_e \omega_m f_c(\theta_e) \quad (12)$$

Where  $K_e$  is the back-EMF constant,  $\omega_m$  is the mechanical angular speed, and  $f_a$ ,  $f_b$ ,  $f_c$  are unit-amplitude trapezoidal functions shifted by  $120^\circ$  electrical.

##### D. Torque and Mechanical Dynamics

The electrical angular speed  $\omega_e$  is related to the mechanical speed by the number of pole pairs  $p$ :

$$\omega_e = p \cdot \omega_m \quad (13)$$

The instantaneous electromagnetic torque  $T_e$  generated by the motor is evaluated by calculating the total electrical power transferred across the air gap:

$$T_e = \frac{1}{\omega_e} (e_a i_a + e_b i_b + e_c i_c) \quad (14)$$

Equivalently, substituting the back-EMF equations yields:

$$T_e = K_t (f_a(\theta_e) i_a + f_b(\theta_e) i_b + f_c(\theta_e) i_c) \quad (15)$$

Where  $K_t$  is the torque constant. The overall mechanical dynamic equation dictating the rotor movement accounts for the load torque  $T_L$ , the moment of inertia  $J$ , and the viscous friction coefficient  $B$ :

$$J \frac{d\omega_m}{dt} + B\omega_m + T_L = T_e \quad (16)$$

The rotor electrical position is tracked by integrating the electrical speed:

$$\frac{d\theta_e}{dt} = \omega_e = p \cdot \omega_m \quad (17)$$

## V. MATLAB/SIMULINK IMPLEMENTATION AND RESULTS

The mathematical modelling and MATLAB/Simulink implementation together provide a complete representation of the multilevel-inverter-based BLDC motor drive. By deriving phase-voltage, back-EMF, torque and mechanical equations, the model captures the essential nonlinear coupling between inverter switching states, stator currents, electromagnetic torque and rotor dynamics.

### A. System Block Integration

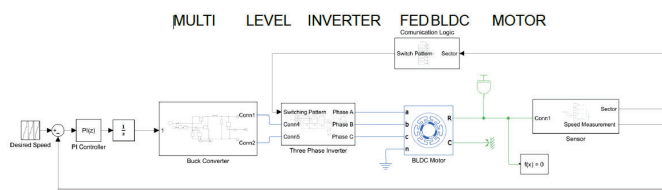


Fig. 1. Complete MATLAB/Simulink Block Diagram mapping the target speed through the PI controller toward a Buck Converter stage ensuring appropriate voltage scaling before the inverter.

**Three-Phase AC Source and Rectifier:** This block represents the grid or laboratory three-phase supply feeding a diode bridge rectifier to produce a DC voltage. The series RLC branch models line impedance and filters high-frequency components before they reach the DC-link.

**DC-Link and Energy Storage:** The rectified output is applied to a DC-link consisting of capacitors that smooth the pulsating DC and provide an energy buffer to the inverter. This section maintains a nearly constant DC-bus voltage despite load and switching variations.

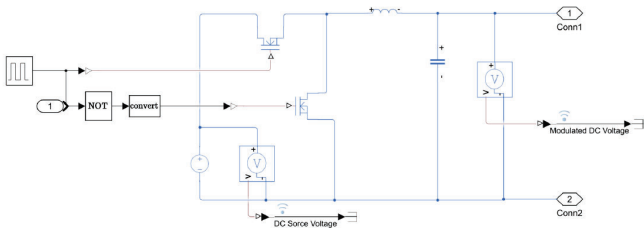


Fig. 2. Simulink subsystem for the Buck Converter and DC-Link voltage regulation.

**Multilevel Inverter Power Stage:** Three identical inverter legs, built from multiple IGBT/MOSFET bridges with anti-parallel diodes, form a three-phase multilevel inverter. Each leg converts the DC-link voltage into a stepped phase voltage for one motor phase, generating several discrete levels instead of a simple two-level square wave. This structure reduces THD,  $dv/dt$  and device stress, improving waveform quality and efficiency. The internal configuration of the three-phase

inverter network comprises switching paths (AH, AL, BH, BL, CH, CL) designed to distribute thermal load equally.

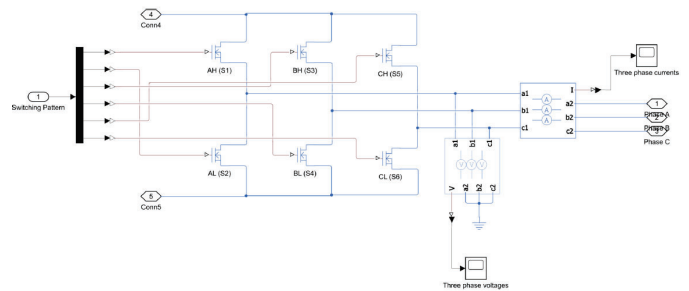


Fig. 3. Internal configuration of the three-phase inverter network comprising switching paths (AH, AL, BH, BL, CH, CL).

**Control, PWM and Commutation Subsystem:** A control subsystem receives a reference speed and the actual speed from the motor and computes the speed error. A PI controller processes this error and sets the modulation index or duty ratio for the PWM generator. The multicarrier PWM and commutation logic convert this command and rotor position (or Hall signals) into gate pulses for each inverter switch, ensuring correct 120-degree BLDC commutation. The communication logic utilizes sectors configured between  $0^\circ$  and  $360^\circ$  to switch conduction bands seamlessly. The system integrates a generalized layout mapping the target speed through the PI controller toward a Buck Converter stage ensuring appropriate voltage scaling before the inverter.

### B. Simulation Results Analysis

**Speed Tracking Performance:** The overall rotor speed profile demonstrates rapid acceleration and lock-in dynamics. Upon energization, the PI controller manipulates the phase voltages heavily. As captured by the PS-Simulink conversion outputs, the velocity ramps up following a standard first-order exponential trajectory, completely stabilizing and clamping its reference target near  $t = 1.5$  seconds without experiencing destructive overshoot. The smooth settling characteristic proves the efficacy of the multilevel step voltage delivery compared to harsh two-level inputs.

**Stator Current Ripple and Torque Regulation:** An analysis of the high-frequency oscillatory waveforms highlights the active commutation. Phase currents map tightly over corresponding switching envelopes with significantly suppressed ripple amplitudes, oscillating tightly between  $\pm 40$  A during initial transients and settling into consistent periodic bands. This improved current harmonic profile natively smooths the electromagnetic torque generation. During the steady-state interval, the torque fluctuations operate within an extremely narrow hysteresis band, maximizing mechanical power delivery while eliminating low-frequency structural vibrations typically inherent to standard trapezoidal commutation.

**Rotor Position Telemetry:** The integrated simulated ideal rotational motion sensor calculates the absolute electrical angle ( $\theta_e$ ). The measured telemetry confirms that the angular progression forms perfect linear ramps modulo  $360^\circ$  (manifesting

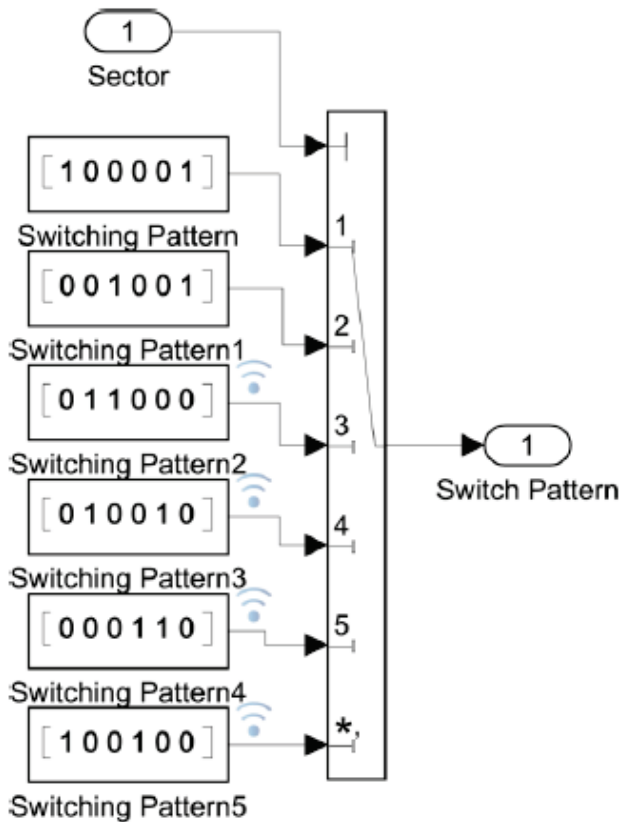


Fig. 4. Commutation logic utilizing configured sectors to switch conduction bands seamlessly.

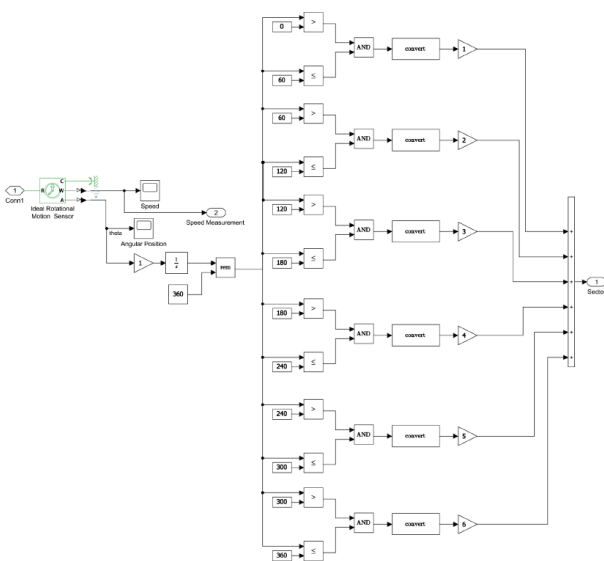


Fig. 5. Sensor logic subsystem to determine the active sector between 0° and 360° based on rotor position.

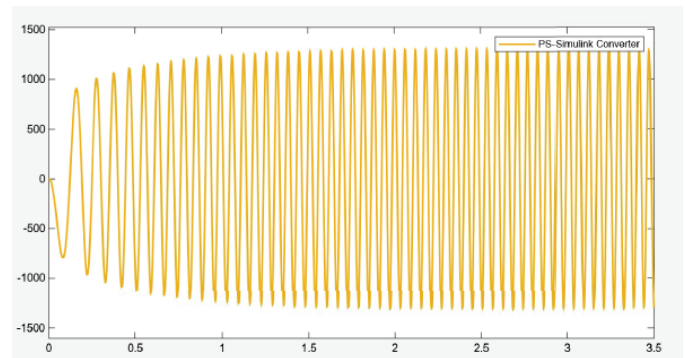


Fig. 6. Rotor speed profile demonstrating rapid acceleration and lock-in dynamics without destructive overshoot.

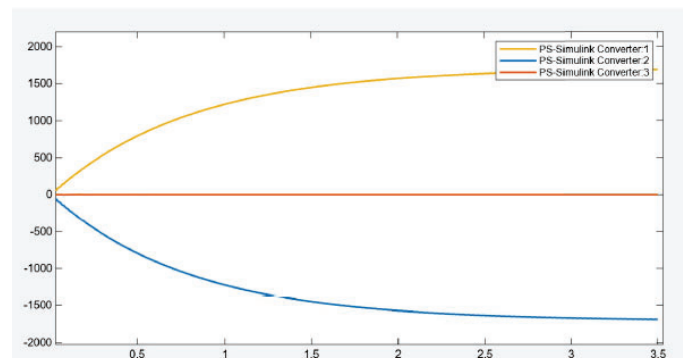


Fig. 7. Three phase currents oscillating tightly between  $\pm 40$  A during initial transients and settling into consistent periodic bands.

as a high-density sawtooth wave when bounded), confirming that the multi-level gating algorithm tracks the rotor position synchronously without desynchronization faults under heavy loads.

## VI. CONCLUSION

The work completed establishes a full MATLAB/Simulink framework for a multilevel-inverter-based BLDC motor drive, covering literature survey, mathematical modelling and the proposed method. The literature study showed that while BLDC motors offer high efficiency, high power density and excellent dynamic response, their performance with conventional two-level inverters is limited by high  $dv/dt$ , significant harmonic distortion, torque ripple and increased switching

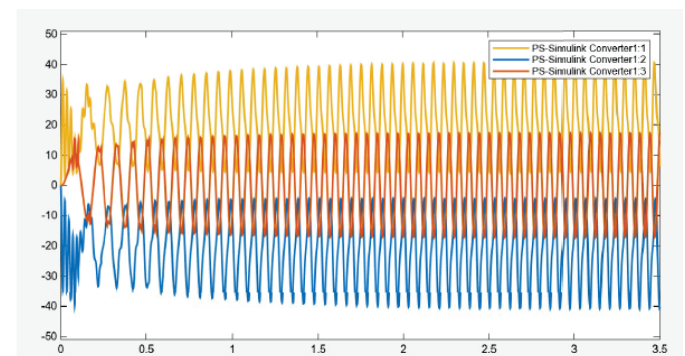


Fig. 8. Three phase voltages oscillating.

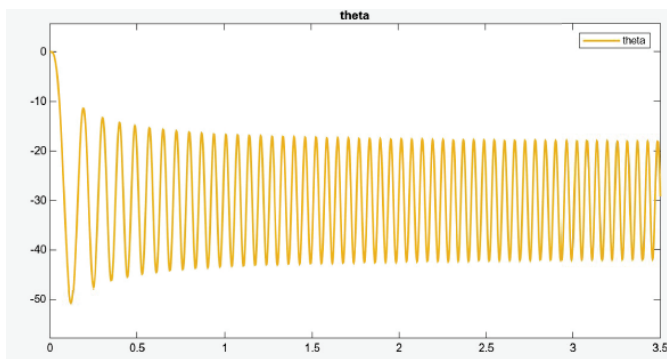


Fig. 9. Measured telemetry confirming the angular progression forms perfect linear ramps modulo  $360^\circ$ .

losses, particularly in high-power applications. Research on multilevel inverters demonstrates that by synthesizing stepped output voltages from several DC levels, they reduce THD, share DC-link voltage among devices and improve waveform quality without excessive switching frequency.

Mathematical models were derived for both the BLDC motor and the chosen multilevel inverter. The BLDC model uses three-phase stator voltage equations with phase voltages, currents, stator parameters, and speed- and position-dependent trapezoidal back-EMFs, along with the electromagnetic torque equation and the mechanical dynamic equation relating torque, inertia, friction and rotor speed. For the five-level cascaded H-bridge inverter, switching functions were defined for each H-bridge cell so that the phase voltage becomes the algebraic sum of individual cell outputs, producing discrete levels. These inverter equations were then coupled with the BLDC equations by using the synthesized phase voltages as inputs to the motor model and by using rotor position to determine commutation and switching patterns.

The proposed method implements this model as a structured Simulink system rather than as isolated equations. A control subsystem has been created that includes a speed-feedback loop with a PI controller, electronic commutation logic based on rotor position, and multicarrier sinusoidal PWM to generate gate pulses for all switches in the five-level inverter. A complete, literature-supported, mathematically sound and simulation-ready multilevel BLDC drive has been designed in MATLAB/Simulink, providing the foundation for extracting quantitative performance indicators such as THD, torque ripple and speed-tracking quality that verify the advantages predicted by the models.

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