Performance Analysis of a Multi-Channel Data Acquisition System

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Abstract:- **Data acquisition is the process of capturing the measurements and retrieving the information about any real world physical phenomenon. The data acquired by the data acquisition systems are converted into digital values by an analog to digital converter (ADC) and then processed using a digital signal processor or stored for further usage. A multi-channel data acquisition system is introduced here which can be used for acquiring various band limited physical measurements like pressure, temperature, strain, acceleration, acoustics and vibration. It is based on the mixed signal technology which combines the configurable analog cores together with customizable digital cores. The mixed signal platform here is having an ARM Cortex M3 processor, an FPGA fabric and a programmable analog part and can be tuned for various applications as required. The analog unit present here is having programmable features like ADC resolution, clock frequency, filtering unit and acquisition time which will help in improving the performance of the data acquisition system as per the requirement of the application at hand. This paper involves the modeling of a multichannel data acquisition system and its detailed performance analysis.**

Keywords: Mixed signal FPGA, Effective Number of Bits (ENOB), Analog to Digital Converter (ADC), Root Mean Square (RMS), Sampling Rate.

I. INTRODUCTION

Data acquisition is the process of acquiring the information about any real world quantity and converting the information acquired into digital value. Further this value can be used for processing there by controlling the external quantity or can be stored in a personal computer (PC) for future usage. Typically a data acquisition system consists of a PC, an external stand alone data acquisition board plugged into the PC or discrete instruments connected together.

External chassis and instruments can be typically connected to a PC using either standard communication ports or sockets or through interface board connected to the PC. The PC contains any operating system and software that supports the data acquisition and help in obtaining desired result. The personal computer can also be used for supporting functions, such as producing the graphical representation of the data acquisition or for generating report. The PC may not necessarily be in constant control of the data acquisition equipment or even remain connected to the data acquisition equipment at all times.

A multi-channel data acquisition system can measure one or more physical process at a time and control these processes using various combinations of analog input, analog output, digital I/O, or other specialized functions. The multi-channel data acquisition system here is based on the state of art mixed signal technology, which comprises an ARM CortexM3 processor as the digital core performing 32 bit processing, FPGA fabric and programmable analog unit [1]. The programmable analog is divided into Analog Front End (AFE) and Analog Compute Engine (ACE). The AFE consists of two Signal Conditioning Blocks (SCBs), two Analog to Digital Converters (ADCs) and two Digital to Analog Converters (DACs). The ADC present in the programmable analog part is multi-channel Successive Approximation Register (SAR) ADC with 32 input channels which can be multiplexed to perform multi-channel data acquisition. The ACE is having a Sample Sequencing Engine (SSE) and a Post Processing Engine (PPE). The analog signals are received and conditioned using the AFE and the parameters of the analog part are configured using the ACE. The communication between the data acquisition system and PC takes place using the UART present in the mixed-signal board. This standalone multi channel data acquisition system can be used to perform high speed and low power data acquisition in many applications.

The remainder of this paper is organized as follows, section II deals with the modeling of the multi-channel data acquisition system. There we will discuss how the data is acquired by the data acquisition board and how it is monitored and analyzed. In Section III we will see how the data acquisition rate of the ADC can be controlled using the FPGA programming. Section IV explain about the performance analysis of the data acquisition system. Here the performance is analyzed by taking the digitized output samples of the acquired signals. We conclude in section V.

II. MODELING MULTI- CHANNEL DATA ACQUISITION SYSTEM USING MIXED-SIGNAL FPGA

As mentioned earlier the data acquisition system is having a data acquisition board, which acquire the analog signal from the source and give the digitized values to a computer for storage or processing. The mixed-signal data acquisition board used here is based on the SmartFusion technology which will integrate the ARM Cortex M3 processor, FPGA fabric and programmable analog together into a single board. The figure 1 shows the setup of a multi-channel data acquisition system.
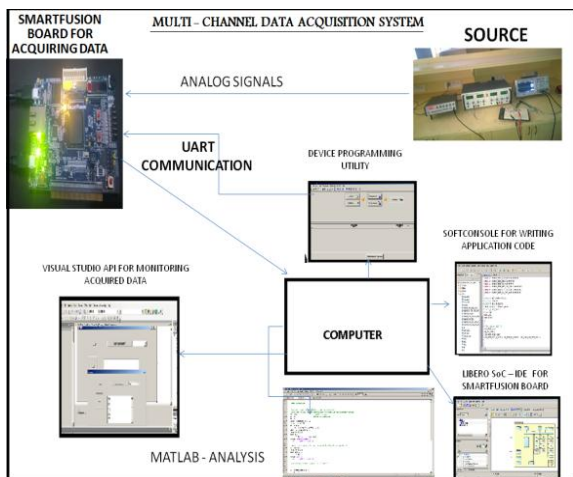
Figure 1. Modelling Multi channel data Acquisition System

The mixed-signal board will acquire the analog input through one of its external pins and give it to the input of the ADC [1] - [2]. The ADC is having configurable resolutions of 8, 10 or 12 bits. The ADC resolution, acquisition time and clock frequency can be adjusted through the ACE in the programmable analog unit. There is also provision for filtering the ADC output with various filtering factors for better performance. The ADC will digitize the input analog value against a 2.56 V reference voltage and the resulting digital value is given to the ARM processor for processing and finally given to the computer for further storage and analysis.

Inside the computer various softwares are running for controlling and configuring the data acquisition board as shown in the figure 1. The libero SoC, is the Integrated Development Environment (IDE) for the mixed-signal FPGA. It helps in setting all the parameters of the mixed-signal board and can also be used to write code for programming the FPGA fabric. Application code for the mixed-signal board is written using SoftConsole, here initialisation of all the peripherals and cores are done. The SmartFusion device is based on the flash technology hence the device is programmed using a FlashPro, which is the device programming utility of the mixed-signal data acquisition board.

The mixed-signal board is programmed to acquire various signals like the output of temperature sensor, pressure sensor, sine wave, square wave, ramp, Gaussian wave and fixed DC values. Input multiplexing is performed to analyse the sampling rate and performance of the multi-channel data acquisition system [3]. During input multiplexing each channel is monitored separately by collecting the digitized output values separately for different channels.

For monitoring the digitised samples from the data acquisition board and doing its further analysis here an Application Programming Interface (API) is created for serial port communication using Visual Studio VC#. Using the API the digitised output is seen and it is collected to a text file for further analysis. It is also possible to use the hyperterminal but collecting large amount of samples and analysing is difficult in the hyperterminal. The analysis of the digitised samples is carried out with the help of MATLAB.

III. CONTROLLING THE SIGNAL ACQUISITION RATE USING FPGA PROGRAMMING

It is possible to control the acquisition rate or sampling rate of the system using FPGA programming. Here the ADC is allowed to acquire the signal in an interrupt routine. The FPGA fabric will generate a periodic interrupt and the rate of occurrence of the interrupt will determine the sampling rate of the ADC. If the FPGA is programmed to generate an interrupt at every 1ms then the acquisition rate of the ADC is 1000 samples per second. Hence it is possible to control the acquisition rate by generating interrupt at different rates. The figure 2 shows the operations performed in the data acquisition board.
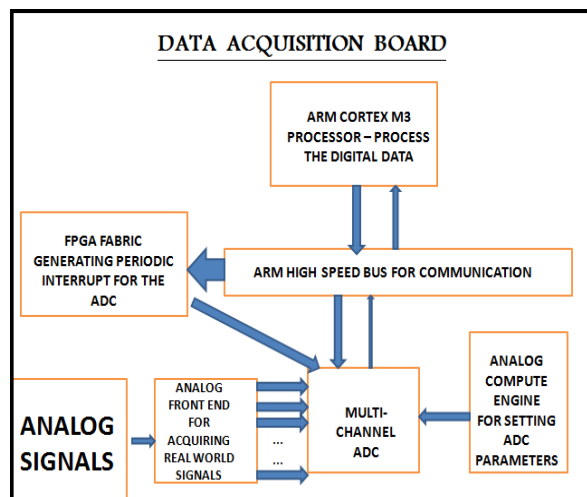

Figure 2. Operations Performed in the Data Acquisition Board

The interrupt can be generated using a simple counter design using VHDL. Different counts are chosen for varying the rate of the periodic interrupt. Figure 3 shows the simulation result of the FPGA interrupt.
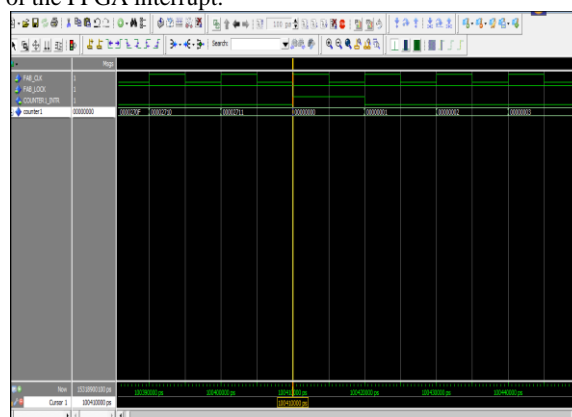

Figure 3. Simulation Result of Periodic Interrupt

IV. PERFORMANCE ANALYSIS OF THE DATA ACQUISITION SYSTEM

The accuracy of the data acquisition system is mainly characterized by the effective number of bits (ENOB) of the ADC. ENOB is the number of bits in the ADC resolution that is not affected by noise. The concept of resolution and ENOB of ADC are explained below,

A. Resolution

Resolution is the number of output levels to which an ADC can quantize a signal or the number of bits present in the ADC output. It can be also denoted as the smallest voltage change an ADC can measure.

Resolution in terms of voltage is also known as LSB.

$$1 \text{ LSB} = \text{VREF}/ 2^N$$

Where VREF is the reference voltage and N is the resolution in bits.

B. Effective Number of Bits (ENOB)

Effective number of bits is one of the parameters used for analysing the dynamic performance of the ADC [4]. If the ENOB is 6.5 bits then it means that the converter performs, as if it were an ideal 6.5 bit ADC. The effective number of bits of the ADC is defined as,

$$\text{ENOB} = N - \log2 [QA/QT]$$

Where N is the ADC resolution, QA and QT represents the actual Root Mean Square (RMS) error and theoretical RMS error of the output. The theoretical RMS error is given by,

$$QT = q/ \text{sqrt (12)}$$

Where q is the weight of one LSB bit in the ADC resolution. Hence substituting the above values the ENOB can also be written as,

$$\text{ENOB} = \log2 \text{ (Full Scale Voltage/ RMS noise *sqrt(12))}$$

If the distortion due to the harmonic content of the signal is also considered then the ENOB equation becomes,

$$\text{ENOB} = (\text{SINAD} -1.76) / 6.02$$

Where SINAD is the signal to noise and distortion ratio, expressed in dB.

For ideal case the ENOB = RESOLUTION. But in most of the cases the ENOB value is much less than that of the specified resolution.

C. ENOB Analysis

ENOB determines how much of the resolution is actually valid, irrespective of the ADC noise. The ADC noise mainly comes from the quantization error, clock jitter of the ADC, error due to unwanted harmonics and noise caused by the converter itself. For calculating the ENOB the standard deviation of a fixed number of samples are calculated [5]-[6]. The standard deviation is calculated by two methods, using the ARM processor and by offline method using MATLAB.

ENOB calculation is done for fixed DC signal and also for signals with harmonic contents like sine wave.

1. Calculating RMS Noise using ARM Processor

Here various input signals are applied to the data acquisition board and 512 samples are collected for each input. The resolution was set to 12 bits and the full scale range is 2.56V. Due to the double buffering property of ADC two buffers are used for collecting and calculating the standard deviation. The ADC will read the input inside the interrupt routine, in which both the buffers are updated. When one buffer is filled with ADC samples the standard deviation of the other buffer is calculated.

The standard deviation is calculated separately for both the buffers in two different loops. The resulting standard deviation of two buffers are observed using the visual studio API as shown in figure 4 and the standard deviation is observed in the range 0.6 to 0.79 range.
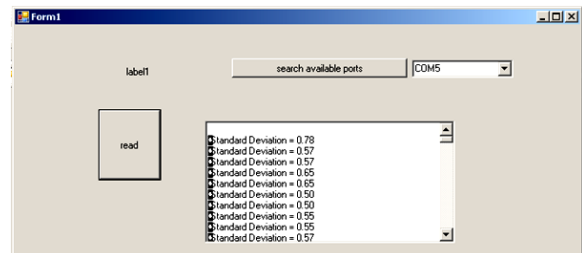

Figure 4. Standard Deviation of ADC outputs

The ENOB is obtained by substituting the value of RMS noise in the equation of ENOB.

$$\text{ENOB} = \log2 \text{ (Full Scale Range/ RMS noise *sqrt(12))}$$
$$= 10.1 \text{ bits}$$

That is out of 12 bits only 10.1 bits are accurate and rest of the bits are affected by noise.

2. Calculating RMS Noise using MATLAB

Here the digitized ADC samples of various input signals are written to a .text file using the visual studio API and the file is then exported to the MATLAB for calculating the standard deviation. The figure 5 below shows the digitized ADC samples in the solution window of the visual studio API and figure 6 shows the values written and stored in a text file for further analysis.
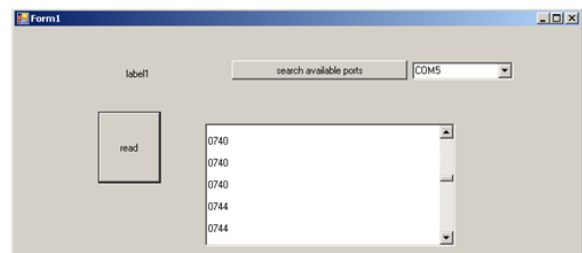

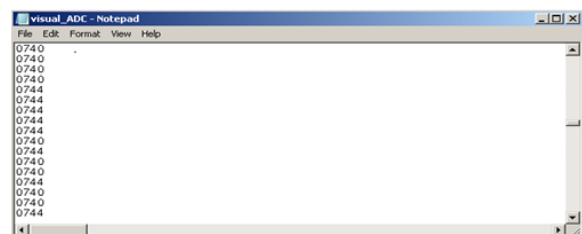Figure 5. Digitized ADC outputs in the Visual Studio API

Figure 6. Digitized ADC outputs in Text File

Standard deviation was calculated using MATLAB and the result obtained is around 1.89 bits.

This value is substituted in the equation for ENOB and the result obtained is,

$$\text{ENOB} = 9.5 \text{ bits}$$

This method is opted as more accurate one, because the noise is less when calculating ENOB offline. Hence it is observed that out of the 12 bits only around 9 bits are accurate and rest of the bits are affected by noise. Substituting the actual value of resolution in the equation of LSB it is observed that the LSB value or the smallest change in voltage the ADC can measure is increase; hence the accuracy of the ADC is reduced.

D. Improving The Performance By Filtering

The noise of the samples collected by ADC can be reduced by oversampling the signals and applying filtering to the digitized samples [7]. Filtering can be enabled through ACE and various filtering factors can be applied from 0-2048 is applied and the performance improvement can be observed as shown in. Here a filtering factor of 128 is applied and the improvement in RMS noise is shown below,
Figure 7 shows ADC output without filtering and figure 8 shows performance improvement with filtering.
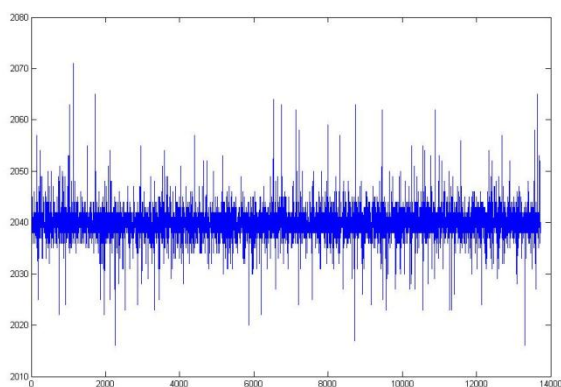

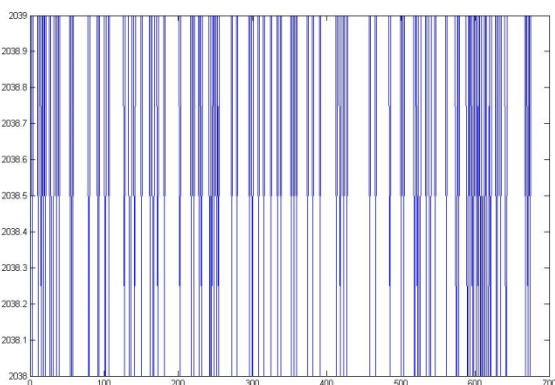Figure 7. ADC Output without Filtering

Figure 8. ADC Output with Filtering

It is observed that the ENOB is only 1 bit less than the actual resolution when filtering is applied to the ADC outputs. Hence the performance of the data acquisition is improved.

V. CONCLUSION

A multi-channel data acquisition using mixed-signal FPGA is introduced here and its various features are also discussed. This multi-channel data acquisition system can be used to acquire various signals simultaneously and there by monitoring and controlling different real world processes at the same time. The data acquisition rate of the system can be controlled as per our application requirement using a periodic interrupt generated by the FPGA. Also the performance of the data acquisition system is studied by analyzing the accuracy of the SAR ADC present in the programmable analog unit. The accuracy of the ADC is determined by calculating the ENOB of the digitized ADC output samples. It is observed that the ENOB of the ADC is improved when the output of the ADC is filtered by applying various filtering factors. Since all the data acquisition elements and digital signal processor are present on the same board this can be used as a compact, low cost and high speed data acquisition system for gathering information about different real world physical phenomenon and controlling them simultaneously

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