Parameter Optimization Of GAA Nano Wire FET Using Taguchi Method

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Abstract

As the process technology is becoming less than 32nm, the variations in Gate length, Channel width and Gate Oxide thickness affect the charge and potential distributions. These variations in turn will affect the Voltage-Current characteristics of the device. Nano wire FET devices are promising candidates to realize the high speed operation of the FET. However high access resistance, capacitances and self heating effects are challenges are for multi Gate FET architectures. Also the analysis of their behavior is complex because it is influenced by the size, shape, channel orientation and strain induced by the fabrication process. The charge distributions are to be analyzed with respect to Azimuthal co-ordinates in weak inversion region which is affected by the charge distribution. In this paper the I-V characteristics of the GAA Nano Wire FET are optimized using Taguchi method.

Keywords: FinFET, GAA, Taguchi, Nano wire, optimization.

1.0 Introduction

The advances made in the MOSFET fabrication technology has resulted in the fast growth of modern integrated circuits and computers [1]. The steps needed in fabricating the MOSFET are lesser than those needed in the case of a BJT. This translated into lesser manufacturing costs for a MOSFET. The Bipolar technology cannot be scaled down without compromising the transistor characteristics. In the case of the MOS transistor, the scaling down of the size can be done without compromising on the performance. This resulted in tremendous growth of MOSFET technology. The Moore's Law predicted that the number of components fabricated on an integrated circuit increases at a rate of roughly a factor two per year. The consequences of Moore's law are, ever increasing power while decreasing costs because of higher levels of transistor and circuit integration. The technology improvements and innovations like Strained Si channels [2], high-K dielectric [3], Metal Gates [4] are being used. Also development of new designs like Ultra-Thin Body (UTB) transistors, FinFET's and other Dual Gate Transistors [5], Tri-Gate transistors and Silicon Nano wire Gate All Around (GAA) transistors [6] has made it possible for the Moore's law to be satisfied even in the next decade.

2.0 Scaling Issues

For the past few decades there has been a steady reduction in the length of the channel, gate oxide thickness and the supply voltage. These resulted in the steady improvement in the transistor performance, smaller transistor size and reduction in the cost. The scaling down of the transistor size results in increased IC packaging density, increase in speed and low – power dissipation.

A further reduction in the size of the transistor i.e. when the device dimensions start reaching the nanometer region, new effects in the device performance arising from new physical phenomenon are seen. The performance of the device should me improved even when the device size is decreasing. This requires modification in both the device design and fabrication process. The reduction in the device dimensions results in undesirable effects

labeled as short channel effects. There are 3 main short channel effects and these are:

(a) Decrease in Threshold voltage
(b) Drain Induced Barrier Lowering and
(c) Sub Threshold slope degradation

To maintain electrostatic integrity and to control short channel effects, the gate oxide thickness is reduced. But there is a physical limit beyond which the carrier tunneling current through the gate increases dramatically. This gate-oxide tunneling current increases exponentially as the Gate-Oxide thickness decreases. Another effect of thin gate oxide is that there is a loss of inversion charge leading to smaller capacitance and smaller trans-conductance. Another effect of thin gate oxide is that the inversion layer is lost.

The shrinking of MOSFETS beyond the 50-nm technology needs additional innovations to deal with the barriers imposed by the fundamental physics. The most important issues involved are (a) Current tunneling (b) quantum mechanical tunneling (c) Threshold voltage increase due to quantum confinement and (d) Random Dopant induced fluctuations. As the gate length is reduced to around 10 nm level, gate control over the channel region is reduced and there is an increase in the Source-Drain tunneling of electrons. This significantly reduces the sub threshold slope S at gate lengths less than 10 nm, thus increasing the off state current. The quantum mechanical narrow channel effect occurs because of the electrons in the inversion layer are not only located away from the surface but also occupy discrete levels in the channel. Now a larger threshold voltage is needed to populate the inversion layer.

3.0 New Devices

As the MOSFET is scaled down in size, it requires new materials and newer device concepts. The new devices that are being used are UTB FET, Dual Gate FET, FinFET, Tri Gate FET and Gate All Around (GAA) FET. These new devices help to continue scaling as they provide reduced short channel effects, sharper sub threshold slope and improvement in carrier transport.

In the UTB MOS device a thin silicon channel with an underlying insulation oxide is used. This is to remove the leakage current paths through the substrate and to reduce parasitic capacitances. This increases the device speed. Here the semiconductor substrate can be replaced with an insulating dielectric.

The Dual gate FET allows for more device scaling as it further suppresses the short channel effects. This is due to the presence of two gates- doubling the effective gate control. The FinFET is the most popular dual gate FET. Here the channel consists of a thin vertical fin around which the Gate is wrapped around on three sides. The fin width is an important parameter because it determines the body thickness and short channel effects. The vertical nature of the FinFET channel has (110) oriented surfaces on a standard (100) wafer.

The Tri-Gate and Omega-Gate FET are examples of multi-gate transistors having three sided gate structures. In the Omega-gate FET, the gate extends into the substrate on both sides creating an effective fourth gate which provides better gate control than the Tri-Gate FET. The Figure 1 shows the TEM image of the GAA FET. [7].

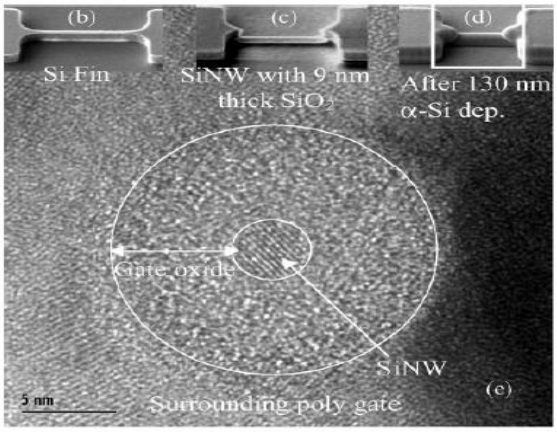

Fig 1: TEM Image of the fabricated GAA

The Silicon Nano wire Technology uses semiconductor Nano wires which are cylindrical single crystal structures. The diameters of these are in few Nano meters and they exhibit several interesting properties. The ultimate scaling of MOSFET is done for GAA-FET using the Nano wire approach.

4.0 GAA Nanowire FET & its Electrical Characteristics

As the scaling of classical CMOS is approaching its limit, new device architectures are being developed. The GAA structure is reported to lead to better gate control and better short channel performance. The Figure 1 shows the TEM image of a reported 200 nm long wire Nano wire with 4 nm diameter and 9 nm thick oxide. The fabrication process started with a p-type silicon-on-insulator (SOI) wafer. Active areas were etched out down to the buried oxide to form a silicon fin structure.

The patterned silicon was then oxidized in dry O_2 which resulted in two Nano wire cores, one at the bottom and another at the top fin. The top nanowire was etched out and bottom one was released from the underlying oxide using wet etch process. The release was followed by a 9 nm gate oxide and 130 nm **α-Si** deposition to form the gate dielectric and polysilicon gate electrode.

The Figure 2 shows the device geometry of GAA Nanowire FET.

The Figure 3 and 4 show the I_d vs. V_d and I_d vs. V_{gs} characteristics of GAA Nanowire FET [8]. The device is fabricated for 5nm diameter and 180 nm channel length SiNW FET shows ON-state currents of 1.5 mA/µm and 1 mA/µm for n and p-FETs respectively. The OFF is state current less than 1nA/ µm at 1.2 V of operating voltage. The electron and hole mobilities were estimated to be ~750cm^2/V-S and ~325 cm^2/V-S, for holes and electrons which are lower than the other reported Nano wires. However the sub threshold characteristics of n-FET were nearly ideal with SS~63 mV/dec and the DIBL was also good.

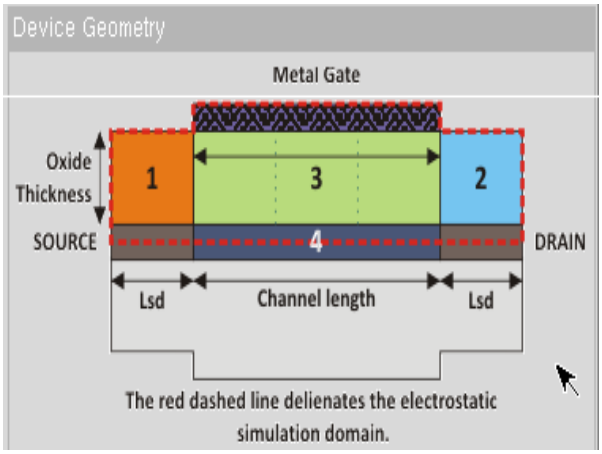

Fig 2: Device Geometry of GAA Nanowire FET

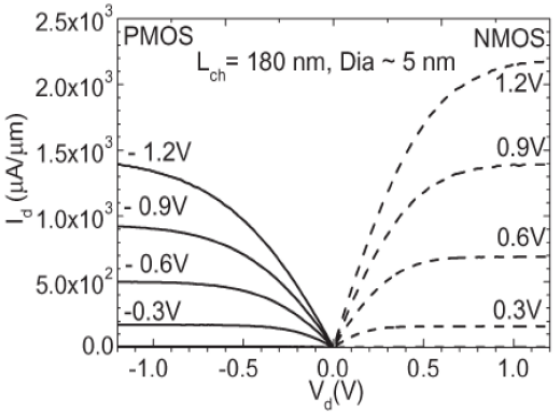

Fig 3: I_d-V_d curves for a 5 nm diameter GAA Silicon Nanowire transistor

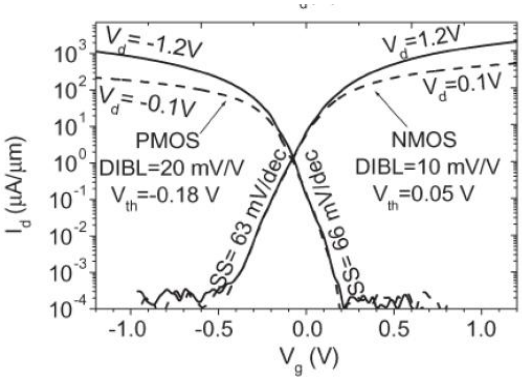

Fig 4: I_d-V_{gs} curves for a 5 nm diameter GAA Silicon Nanowire transistor

5.0 Taguchi Method of Optimization

The Taguchi method is based on the Orthogonal Array experiments which give a much better variance with optimum settings of control parameters. The combination of design of experiments with the optimization of control parameters will achieve best results.

The Taguchi method breaks the optimization problem in two categories. These are:

(1) Static Problems and

(2) Dynamic Problems

A process to be optimized has several control factors which directly decide the target or the desired value of the output. If the optimization is done using the best control factors, it is called Static problem. This ensures that the output is the target value. The important characteristic of the Taguchi method is to minimize variations in the output even in the presence of noise.

The dynamic problem is applicable to those systems which have a signal input that directly decides the output. Here the optimization involves determining the best control factor levels, to get the input output ratio as close to the desired target as possible.

The orthogonal arrays allow for significant reduction in the number of experimental runs to find the optimal solution. The orthogonal array allows for the evaluation of each level of a factor independent of the values of other factors. This property leads to reduction in the number of test runs needed to cover all the combination of factors and their level resulting in quicker testing to achieve optimal solutions.

6.0 Results and Conclusions

The Taguchi method was applied to optimize the I-V characteristics of the GAA Nanowire FET. The issues considered during the optimization are:

NEGF solved for Poisson and Schrödinger equations

Suitable bias set and Hamiltonian Matrices are chosen for an isolated channel

The self consistent potential is considered

Self energy matrices were considered

Ballistic channel coupling to Source-Drain contacts and scattering process is considered.

Retarded GF has been calculated.

Neumann boundary conditions are considered

The V-I characteristics of the GAA Nano wire FET is shown in Figure 5.

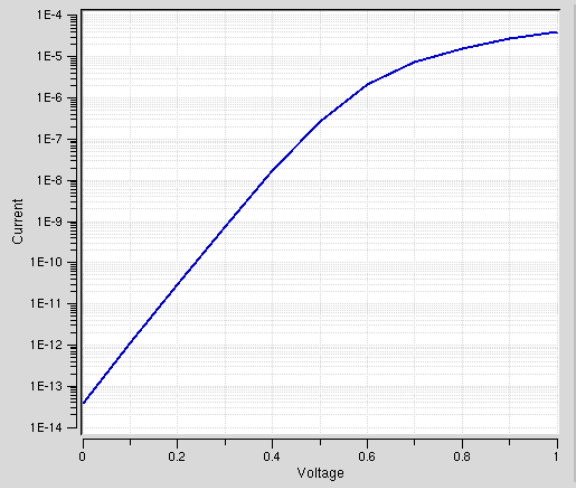

Fig 5: V-I Characteristics

The Figure 6 shows the mid channel charge density profile for the Omega-Gate FET. As seen, most of the charge density is located in the range of 10-20 nm.

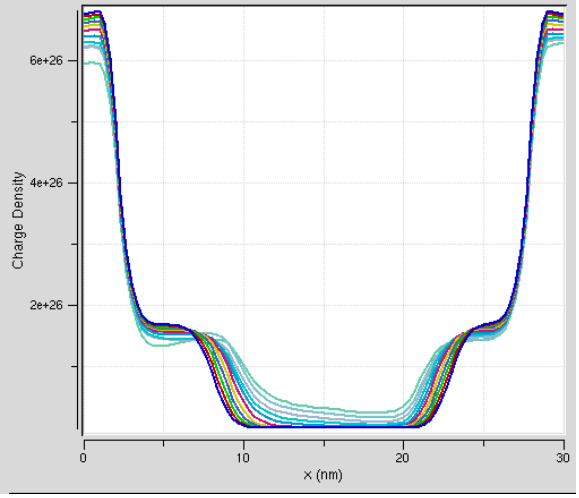

Fig 6: Mid Channel Charge Density Profile

The Figure 7 shows the conduction band profile in the mid channel range.

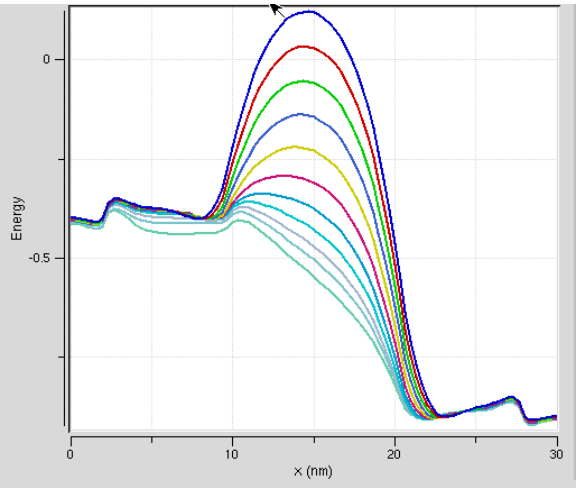

Fig7: Mid Channel Conduction Band Profile

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