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Overview of Differential - ended I/O Logic Families

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Abstract- **I undertook in-depth technical survey to bring out this survey paper covering-Differential logic families including Low-Voltage Differential Signaling(LVDS), Low-Voltage Positive Emitter-Coupled Logic, Bus LVDS, Gunning Transceiver Logic, Gunning Transceiver logic plus, Centre Tapped Terminated Logic, Pseudo Current Mode Logic, Point-to-Point Differential signaling, Reduced Swing differential signaling, Quad Rambus Signaling Levels, Transition-minimized differential signaling, Differential Rambus Signaling Level, I/O design parameters, GPIO, SPIO.**

Keywords- IO logic families, Differential ended, LVDS, GPIO, SPIO, IO design parameters, differential signaling.

I. INTRODUCTION

Dramatic increases in processing power, fueled by a combination of integrated circuit scaling and shifts in computer architectures from single-core to future many-core systems, has rapidly scaled on-chip aggregate bandwidths into the Tb/s range [1], necessitating a corresponding increase in the amount of data communicated between chips to not limit overall system performance. Due to the limited I/O pin count in chip packages and printed circuit board (PCB) wiring constraints, high-speed serial link technology is employed for this inter-chip.

Input/output (I/O) has always played a crucial role in computer and industrial applications. But as signal processing became more sophisticated, problems arose that prevented reliable I/O communication. In early parallel I/O buses, interface alignment problems prevented effective communication with outside devices. And as higher speeds became prevalent in digital design, managing signal delays became problematic.

Differential Logic Families

Differential logic families use differential voltage levels to measure the voltage difference between a pair of wires [1].

Low-Voltage Differential Signaling (LVDS)

LVDS is a low-noise, low-power, low-amplitude differential method for high-speed data transfer.

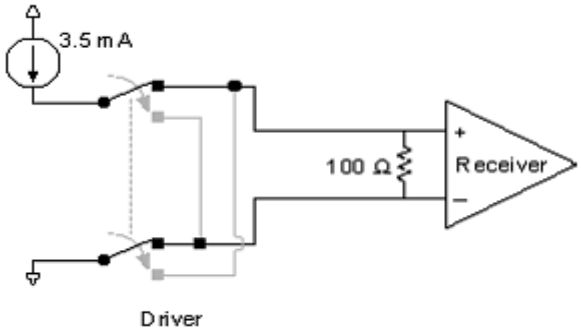

Fig.1 LVDS circuit

A current source at the driver provides approximately 3.5 mA of current. When the current reaches the receiver, a 100 Ω terminating resistor connects the two ends of the differential transmission line which provides a return path for the current and a voltage of approximately 350 mV is established across the two input terminals of the receiver. The differential voltage is either positive or negative at the receiver, based on the direction of the current.

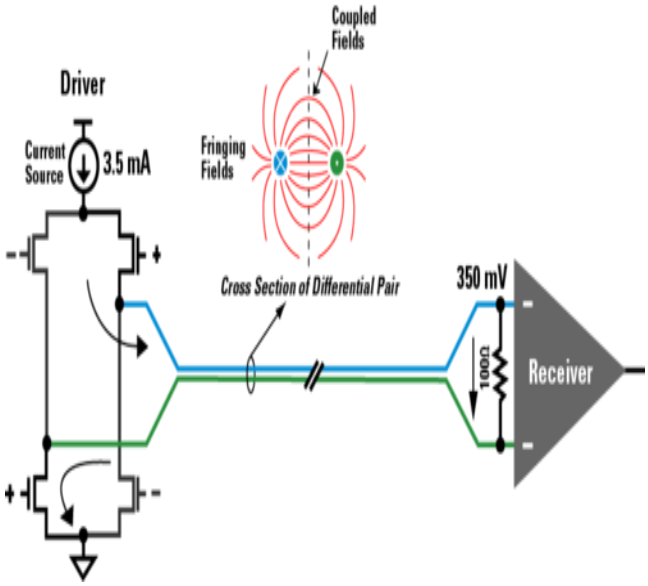

Fig.2 LVDS Circuit

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DC Parameter	Conditions	MIN	TYP	MAX	Units
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	-	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.90	1.03	-	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage (Q + $\overline{Q}$) / 2	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
Input Common-Mode Voltage (Q + $\overline{Q}$) / 2	Differential input voltage = ±350 mV	0.25	1.25	2.25	V

Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

Emitter-Coupled Logic circuit consists of transistors which steer current through gates which performs logical functions. The transistors operate in the active region; hence they can change the state rapidly, so ECL circuits operate at very high speeds. LVPECL circuits are designed for use with VCC = 3 V or 3.3 V.

Bus LVDS (BLVDS)

Multipoint BLVDS system consists of transmitter and receiver pairs (transceiver) that are connected to the bus.

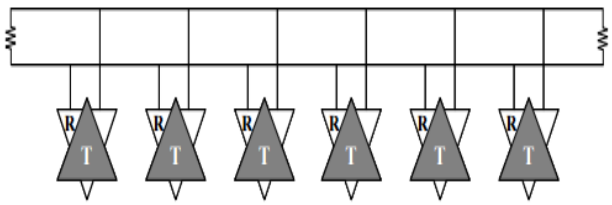

Fig.3 Multi point BLVDS

- The above configuration provides bidirectional half duplex communication while minimizing the interconnect density.
- Few transceiver acts as a transmitter, with the remaining transceivers acting as receivers.
- The performance of a multipoint BLVDS is affected by the capacitive loading and termination on the bus.

Use different input or output buffers depending on the application type:

- Multi-drop application—uses the input or output buffer depending on whether the device is intended for driver or receiver operation.
- Multipoint application—the output and input buffer shares the same I/O pins. An output enable (OE) signal is used to tri-state the LVDS output buffer when it is not sending signals.
- External resistors are used at the output buffers to provide impedance matching to the stub on the plug-in card.

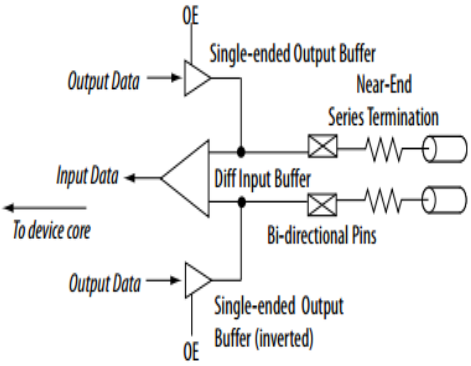

Fig.4 BLVDS I/O Buffers

Gunning Transceiver Logic - GTL

GTL standard is a high speed bus standard invented by Xerox.

Gunning Transceiver logic plus (GTL+)

- The GTL+ I/O standard is used for high-speed back plane drivers and Pentium processor interfaces.
- The GTL+ standard defines the DC interface parameters for digital circuits operating at 2.5, 3.3, and 5.0V.
- The GTL+ standard is an open-drain standard, and Stratix and Stratix GX devices support a 2.5- or 3.3-V VCCIO.
- GTL+ requires a 1.0-V VREF and open-drain outputs with a 1.5- V VTT to which the reference voltage tracks.
- Stratix and Stratix GX devices support both input and output levels.

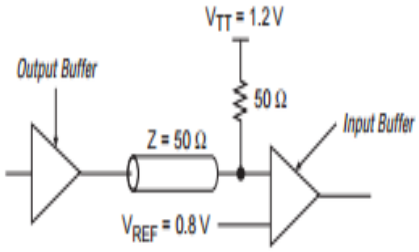

Fig.5 GTL Termination

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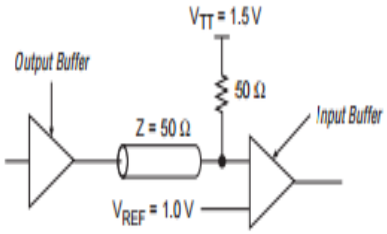

Fig.6 GTL+ Termination

Centre Tapped Terminated Logic (CTT)

CTT - EIA/JEDEC Standard JESD8-4

- The CTT I/O standard is used for backplanes and memory bus interfaces.
- The CTT standard defines the DC interface parameters for digital circuits operating from 2.5- and 3.3-V power supplies.
- The CTT standard does not require special circuitry to interface with LVTTL or LVCMOS devices when the CTT driver is not terminated.
- The CTT standard requires a 1.5-V VREF and a 1.5-V VTT.
- Stratix and Stratix GX devices support both input and output levels.

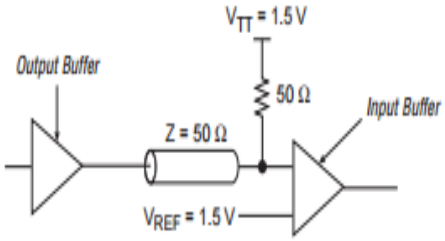

Fig.7 CTT Termination

Pseudo Current Mode Logic (PCML)

- The PCML I/O standard is a differential high-speed, low-power I/O used in networking and telecommunication field.
- This standard requires a 3.3-V VCCIO.
- The PCML I/O consumes less power than the LVPECL I/O standard. PCML has a reduced voltage swing, which allows for a faster switching time and lower power consumption.
- The PCML standard uses open drain outputs and requires a differential output signal. Stratix and Stratix GX devices support both input and output levels.

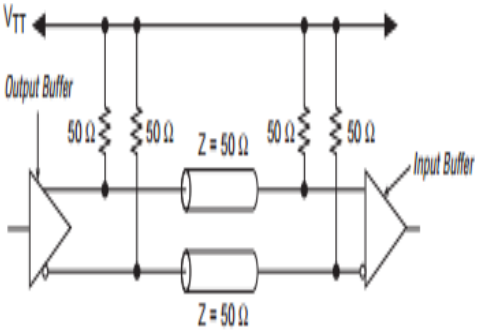

Fig.8 PCML Termination

Point-to-Point Differential signaling (PPDS)

- Point-to-Point differential signaling (PPDS') ensures reliable data transmission to the column driver (CD) from the timing controller (T-con) using few data lines compared with the traditional multi-drop architecture.

Below figure shows the benefits of PPDS. As data output pins and other control lines are reduced, the T-con becomes smaller.

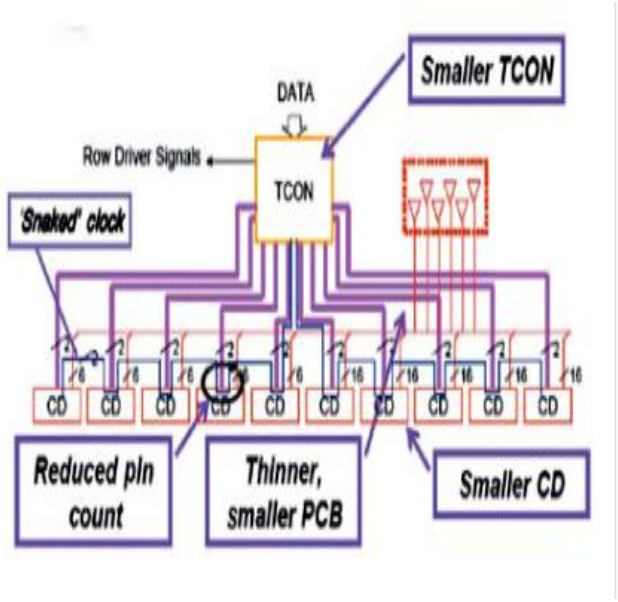

Fig.9 Point-to-Point Differential signaling

A thin PCB design is possible due to fewer data lines and less gamma reference voltages.

Reduced Swing differential signaling (RSDS)

It is an intra panel interface bus standard. It defines the characteristics of transmitter and receiver along with the protocol for a chip to chip interface [5].

The RSDS provides many benefits to the applications that include the following

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- Reduced bus width- enables smaller thinner column driver boards
- Low dynamic power dissipation-extends system run time
- Low EMI generation-eliminates EMI suppression components and shielding
- High noise rejection-maintains signal image
- High throughput-enables high resolution displays

RSDS is used in flat-panel displays to transfer the data between the timing controller and the column drivers.

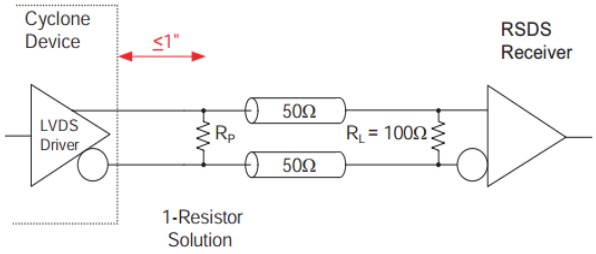

Fig.10 RSDS resistor network

Quad Rambus Signaling Levels (QRSL)

QRSL doubles the data rate by using four voltages to represent two bits of information. This multi-level signaling allows higher data bandwidth, twice that of RSL (>2 GB/s) while it does not increase the frequency of operation of the Channel [4].

Major features of QRSL are:

- Low voltage swing (800 mV p-p, ~267 mV per step)
- Current mode output drivers
- Automatic output current control
- Controlled impedance design typically 40 Ohm systems
- Low parasitic packages
- Double data rate and multi-level signaling, providing four bits of information per clock cycle
- Gray coded logic levels
- Bi-directional Channel
- Pseudo-differential receivers, with three Vref inputs
- New driver and receiver circuits, including integrating receivers
- Common differential clock, which travels with the data, and is the same frequency as RSL
- Terminated at one end

Transition-minimized differential signaling (TMDS)

- TDMS is used for transmitting high speed serial data used by DVI and HDMI video interfaces [6].
- The TDMS standard requires external 50 ohm resistor pull-ups to 3.3V on inputs.
- TMDS inputs standard do not require parallel input termination resistors, and can be placed on any I/O bank, while PPDS outputs are available on I/O banks 0 and 2

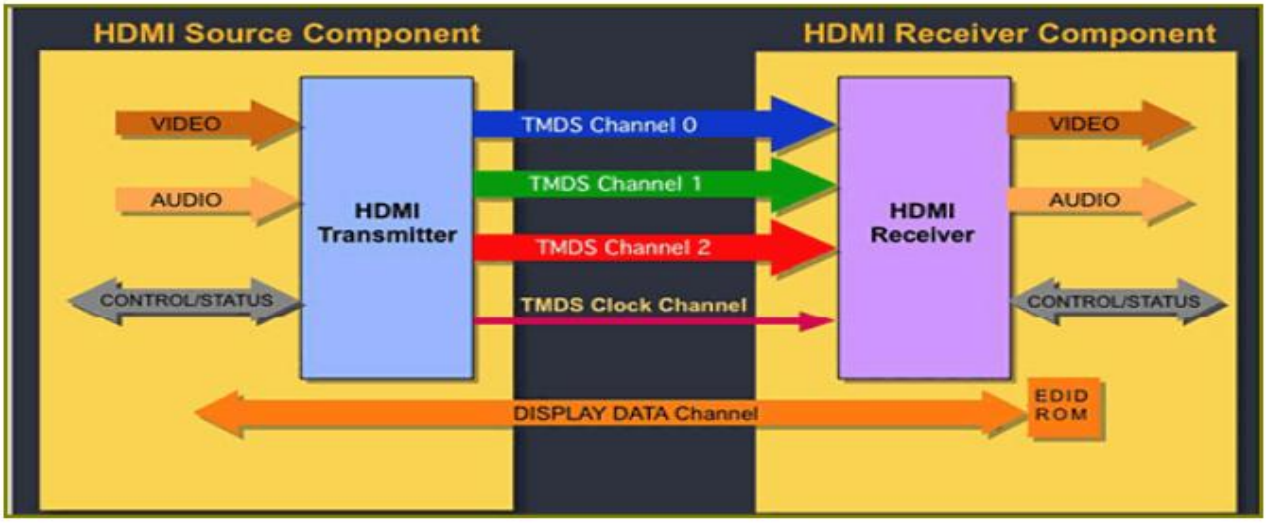

Fig.11 TDMS

Differential Rambus Signaling Level (DRSL)

- DRSL is a bi-directional, differential signaling standard which provides high-performance, low-power, and cost-effective solution for getting bandwidth on and off chip.
- DRSL signals are point-to-point and use an ultra-low 200mV signal swing (1.0 to 1.2 V).
- DRSL also enables low power operation and scalability for future reductions in voltage swing.

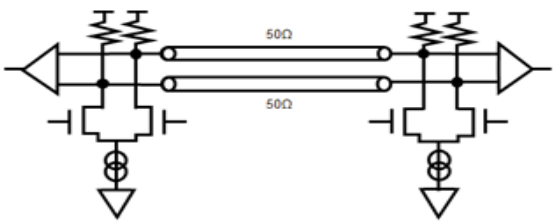

Fig.12 Bidirectional differential signaling

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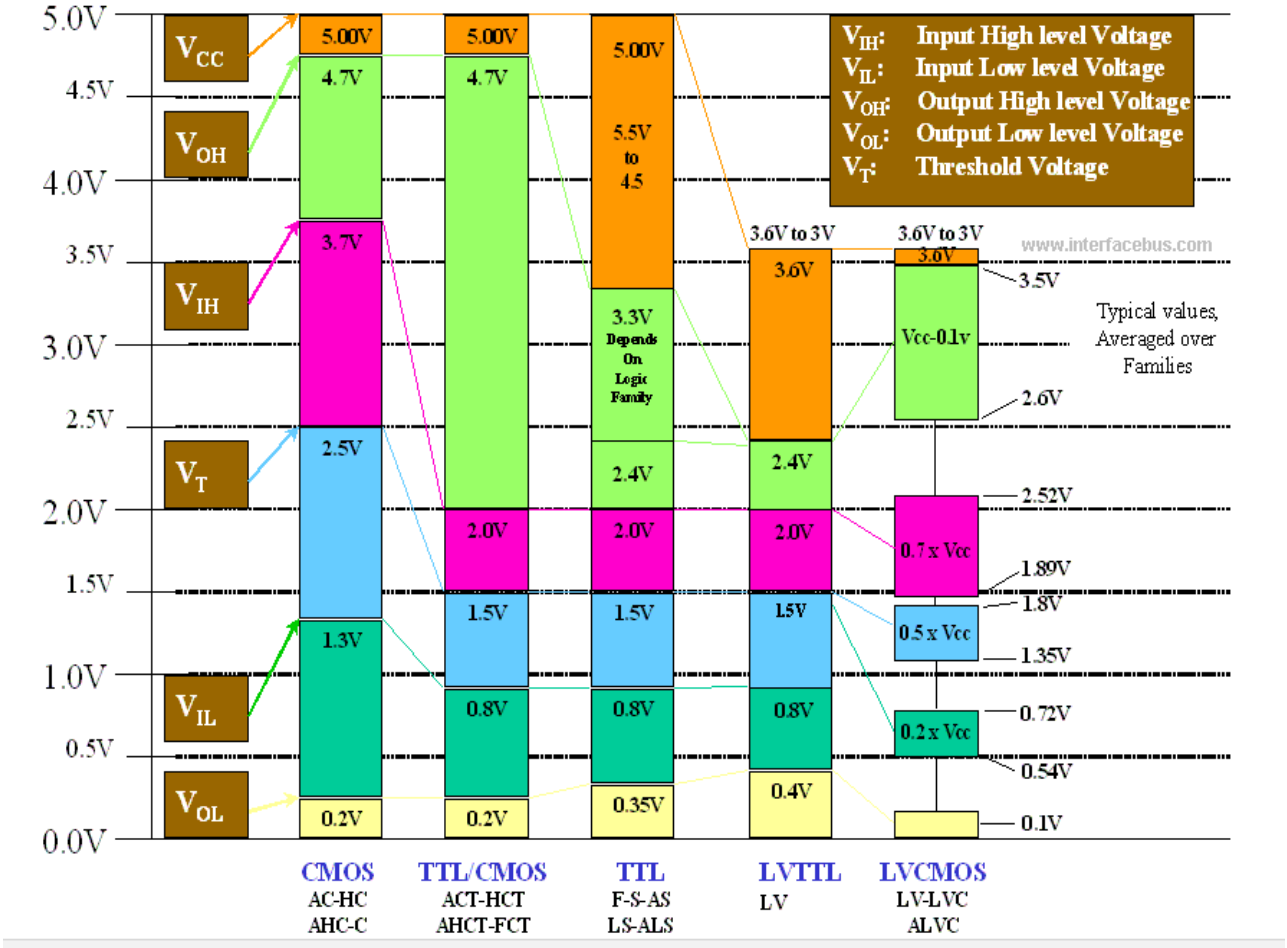
Signaling Technology Differences

	RSL	QRSL	Quad SerDes
Application Areas	Main-Memory	Small memories, chip-to-chip	Chip-to-chip across backplanes
Type	Multi-drop, bidirectional bus	Multi-drop, bidirectional bus	Point-to-point, unidirectional link
Data rate per link	1066 MHz	> 2 Gb/s	3.125 Gb/s
Number of devices	Up to 32 slaves	Up to 4 slaves	2 devices
Length of interconnect	-20 in	-4 in	-30 in
Connectors	Yes	Not initially	Backplane connectors
Voltage swing	800 mV	800 mV	±500 mV differential
Voltage levels	2	4	2
Clock frequency	533 MHz	>500 MHz	Embedded clock
Separate clocks	Yes	Yes	No

Low Voltage Logic Threshold Levels



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Differential I/O signaling

Standard	Description	Industry specification	Use and sponsor	Input buffer	Output buffer
LVDS25 LVDS33	Low voltage differential signaling	ANSI/TIA/EIA-644-A	High speed interface, backplane, video; National ,TI	Differential pair	Differential pair
BLVDS	Bus LVDS	ANSI/TIA/EIA-644-A	Bidirectional, multipoint LVDS	Differential pair	Pseudo Differential pair
DISPLAY PORT	Auxiliary channel interface for DISPLAY PORT	www.vesa.org	Flat panel displays	Differential pair	Pseudo Differential pair
LVPECL	Low voltage positive ECL	Free scale semiconductor(former Motorola)	High speed clocks	Differential pair	N/A
MINI_LVDS	Mini-LVDS	TI, Display panel interface	Flat panel displays	Differential pair	Differential pair
RSDS	Reduced swing differential signaling	National semiconductor	Flat panel displays	Differential pair	Differential pair
TMDS	Transition minimized differential signaling	National, display panel interface	Silicon image; DVI/HDMI	Differential pair	Differential pair
PPDS	Point to point differential signaling	National, display panel interface	LCDs	Differential pair	Differential pair
Differential mobile DDR	Differential LPDDR for CK/CK#	JESD209A		Differential pair	Pseudo Differential pair

B. GPIO

General-purpose input/output (GPIO) is a generic pin on an integrated circuit or computer board whose behavior is controllable by the user at run time [2].

Uses of GPIOs

- Devices with pin scarcity: Integrated circuits such as system-on-chip, embedded and custom hardware, and programmable logic devices.
- Multifunction chips: power managers, audio codecs, and video cards
- Embedded applications (Arduino, PSoC kits, Raspberry Pi etc.) use GPIO for reading the input from various environmental sensors and writing output to DC motors (via PWM), audio, LCD or LEDs for status.

C. SPIO

Special input/outputs are inputs and outputs of a microcontroller that perform specialized functions [3].

Specialized functions include:

- Hardware interrupts
- Analog input or output
- PWM output
- Serial communication

D. I/O design parameters:

- V_{DD}- supply voltage
- I_{IL}-low level input current
- I_{IH}-high level input current
- I_{OZ}-OFF state output current
- I_{LATCH}-I/O latch up current
- V_I-input voltage
- V_O-output voltage
- V_{IH}-high level input voltage
- V_{IL}-low level input voltage
- V_{hys}-hystersis voltage
- V_{OH}-high level output voltage
- V_{OL}-low level output voltage
- I_{OHS}-high level short circuit current
- $I_{DD(act)}$-active mode supply current
- $I_{DD(pd)}$-power down supply current
- T-temperature
- I_{OLS}-low level short circuit current
- I_{pd}-pull down current
- I_{pu}-pull up current

CONCLUSION

I/O technologies are classified into single ended and differential ended. In this survey paper I have summarized ended I/O. As a part of my ongoing research on design and development of futuristic and next generation high speed I/O, it is important to study and understand technology, specification, and key performance parameters all the popular and contemporary I/O technologies. All these functionalities needs to be experimented and further improved.

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