Optimization of Delay and Leakage using Body Bias

Pandit Nad [1] , Dhananjaya A[2]
Student IETE Member, Mtech VLSI Design and Embedded System
Ms.Suma M S[3]
Professor.Dept of ECE
RVCE Bengaluru, INDIA

ABSTRACT

Power dissipation and speed (timing) are noticeable issues should be controlled in VLSI design. Due to constraints on the threshold voltage V^{th} of the transistors it's very difficult for the designer to scale down the power supply while maintaining the speed. Also V^{th} is not lowered to avoid the static leakage powers due to large leakage currents under small V^{th} operation. Body Bias is one design techniquecan be used to the delay and leakage to large extent.The forward body bias(FBB) improves the delay by reducing the threshold voltageV^{th} and the reverse body bias (RBB) decreases the leakage current by increasing the threshold voltageV^{th}.Thus one can reduce the V^{th} keeping the VDD constant. Hence improving the performance parameters of the design. The Body Bias (BB) can be Fixed, Adaptive and Dynamic. In this paper howAdaptive body bias can be used to reduce the delay and leakage is presented. Fixed forward body bias is applied during the ON state of the design to reduce the V^{th} of the transistors thus increasing the performance and Fixed reverse body bias is applied during the off state of designto reduce the leakage currents. Using FBB a decrease of 35% and 55% delay is observed for an Inverter and 3-bit ripple counter respectively and by RBB a decrease of leakage current up to 90% is achieved using 90nm CMOS technology.

Keywords:-Body Bias, Fixed Bias, Adaptive body bias, Dynamic Bias, BBG (Body bias generator), Logic Cell, FBB, RBB, delay, CMOS.

I. INTRODUCTION

In an electronic device design power and performance are the most concern parameters. The user is not comfortable neither only with lowest power design since it limits in handling range of applications and high performance design since it consumes more power.The present day requirement is the High Performance with low power consumption. But this achievement is a difficult task with technology scaling.In CMOS technology over the last ten yearsit has been impossible to scale the power supplyvoltage while maintaining speed because of the constraints on the thresholdvoltageof the transistors[1]. Also V^{th} is not lowered to avoid the static leakage powers due to large leakage currents under small V^{th} operation**.** With the technology scaling from 130nm and downwards VDD and V^{th} scaling achieved is very small[1].Due to this limitation performance improvement design possibilities with the power concern are very difficult and these introduce a many second order effects.

Body bias method can be used to overcome the above said problems. Body biasing is a method of applying the voltages to the substrate terminals(VBN,VBP) of MOSFETs. Body biasing scales the V^{th} of a device without varying the power supply. Forward body bias scales down the threshold voltage and reverse body bias increases the threshold voltage. Thus by wisely applying the FBB and RBB we can reduce the delay and leakage of the design.

II. V^{TH} SCALING IN MOSFETS

The threshold voltage of a transistor depends upon the transistors body voltage. Changing the body voltage applied to transistors bulk terminal changes the V^{th} of a transistor. When FBB body bias is applied V^{th} decreases and for RBB V^{th} increases. Table 1 tabulates the different values V^{th}observed for different values of VBS for both NMOS & PMOS.Fig1 shows the plots of the variation of V^{th}Vs VBS for NMOS & PMOS. For positive bias voltage NMOS substrate is forward body biased (V^{th}decreases)and PMOS substrate is reverse biased (Vth increases). For negative bias voltage NMOS substrate is reverse biased (V^{th} increases) and PMOS substrate is forward biased(V^{th} decreases). These cases can be observed in Table 1 and the plot drawn in Fig 1. This observation motivates the designer to implement the designs by modeling the transistors for body bias.

VBS(V)	V^{th}_N(V)	V^{th}_P(V)
-0.4	0.337154	0.20605
-0.3	0.31956	0.21695
-0.2	0.302145	0.22806
-0.1	0.28334	0.24397
0	0.26372	0.26372
0.1	0.24397	0.28354
0.2	0.22806	0.30345
0.3	0.21695	0.32056
0.4	0.20605	0.3384

Table 1: Threshold Voltage values for different body bias voltages

III. BODY BIAS DESIGN

The transistorssubstrate bias pins can be modeled to optimize the delay and leakage. The substrate bias modeling is of three types: Fixed Body Bias, Adaptive Body Bias and Dynamic Body Bias.In fixed body bias a fixed forward or

reverse bias is applied to the substrate pin of the transistor.In adaptive body bias different body bias voltages are applied according to the operating mode of the design.This avoids the overhead of leakage or delay due to fixed bias voltage.

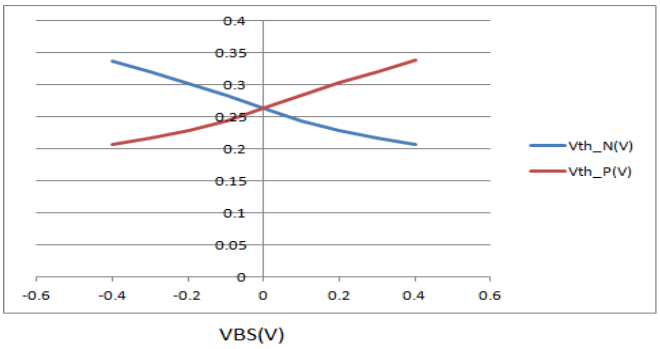

Figure 1: V^{th} scaling wrt body bias voltage for NMOS(Vth_N)& PMOS(Vth_P)

In Dynamic body bias different bias voltages are applied during the on state of the design unlike a single fixed bias voltage used in fixed and adaptive techniques.The adaptive and dynamic body bias based designs requires an extra control circuitry to generate the body bias voltages called Body Bias Generator (BBG).This paper presents an Adaptive BBG design.Many researchers have used adaptive body biasing control on different parameters.The FBB scheme on row-based standardcell layout style that enables selective forward body biasing of only of the rows that contain most timing critical gatesreduces delay of the critical path[3].By generating the probability distribution of dies post-silicon ideal body bias voltage using an efficient sampling method is used for adaptive body biasing [4].Different body bias voltages are generated according the ON or OFF state of the design for adaptive body biasing [5].

In all microprocessor and microcontroller level designs there are control circuits to switch the operating mode of the design from Active mode to different low power modes. Each low power mode turns ON or turns OFF some logic blocks of the processor in order to save the power.The turned OFF blocks power dissipation is only due tostatic leakage contributed by sub threshold current.The frequency of operation will be different in different operating modes. The intelligence required here is to find the different low power modes with respect to the operating frequency change and generate the different body bias voltages adaptively.In this fixed oscillator frequency is used as a reference to compare with operating frequency to find the operating mode of the design. During active mode the concern is about the critical path delaythis delay can be reduced by forward body biasing the design, so for active mode (high frequency) VBias is generated for forward body bias. In low power modes VBias is generated for reverse body bias, to decrease the leakage power.This method uses the changing operating frequency as a parameter to generate the body bias voltages adaptively.

Fig 2 shows the schematic of the adaptive body bias generator.It consists of 3-bit counter and 3-bit shift register to find the operating mode of the design and 8:1 mux to choose the body bias voltage corresponding to the operating mode latched by the shift register.In this ripple counter counts the number of pulses of crystal oscillator frequency in off cycle of an Operating Frequency. The count value of the ripple counter increases with decreasing operating frequency and decreases with increasing the operating frequency. This count value is latched by shift register at every posedge of an operating frequency clock signal.The Inverter is used for this purpose in the design. This will make sure applying body bias as soon as operating mode is changed.

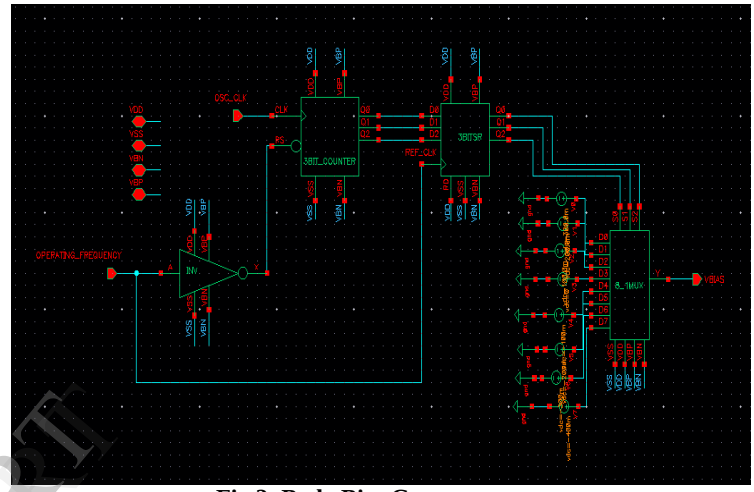

Fig 2: Body Bias Generator

Once the count value is latched by the shift register, the combinational circuit with Mux selects the body bias voltage VBias. This Vbias is applied to the substrate bias pins of the actual design. Using this design and assuming that for high operating frequency select the FBB and for low operating frequency select the RBB resulted in optimization of delay and leakage values for Inverter and 3-bit ripple counter. In both the cases body bias is applied only to NMOS transistors.

Fig 3 shows the schematic of BBG and test circuit of Inverter. The output of BBG is VBias which applied to the VBN pin of the test circuit. The simulations are done with respect to different operating frequency to calculate the leakage and power. The results are documented in the next section.

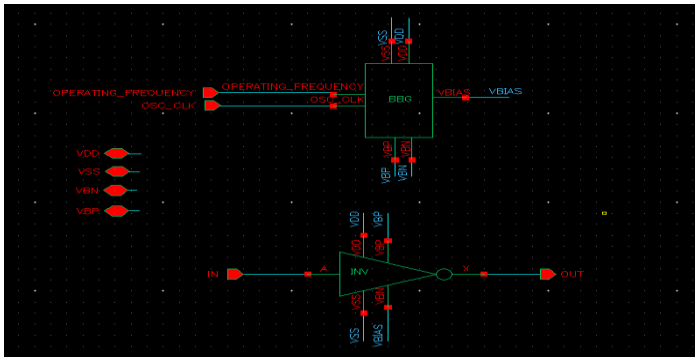

Fig 3: Adaptive Body Biasing on Inverter

Similarly Fig 4 shows the schematic of BBG and test circuit of 3-bit ripple counter. The simulations are also done like Inverter and results are added in the next section. Also it'sproved that performance parameters of BBG are not changed when used for different designs for body biasing.

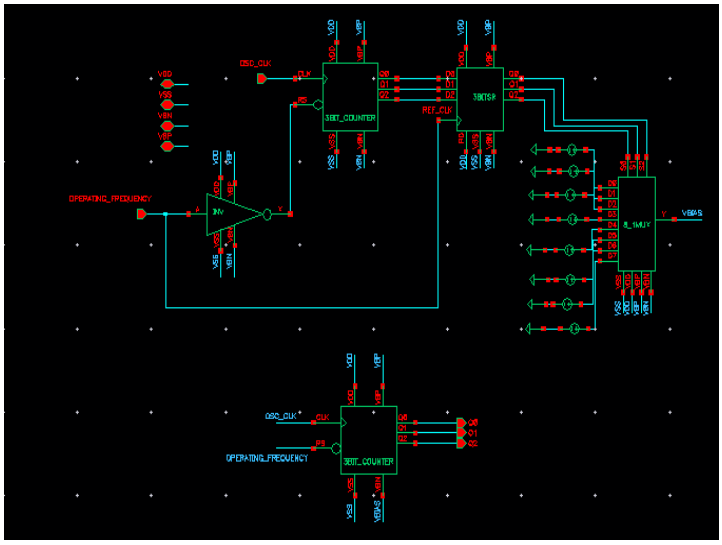

Fig 4: Adaptive Body Biasing on3-bit ripple counter

IV. RESULTS

Simulations are done by choosing a fixed oscillator clock period of 20ns and Operating frequency clock period in multiples of oscillator clock period. The number of counts chooses the VBias voltage.

A: Inverter

Table 2 shows the performance increase of an Inverter by forward body biasing the design during high frequency operation, a maximum of 61% decrease in delay is observed and Table 3 shows the leakage reduction observed by reverse body biasing the design during low frequency operation and decrease of 57% in leakage power is observed.

Table 2: Inverter delay values for different VBias (FBB) values

Vbias	Delay_Inv
0	1.91E-10
0.1	1.73E-10
0.2	1.54E-10
0.3	1.35E-10
0.4	1.12E-10
0.5	9.07E-11
0.6	6.59E-11

Fig 5 plots the VBias Vs Delay of an Inverter.

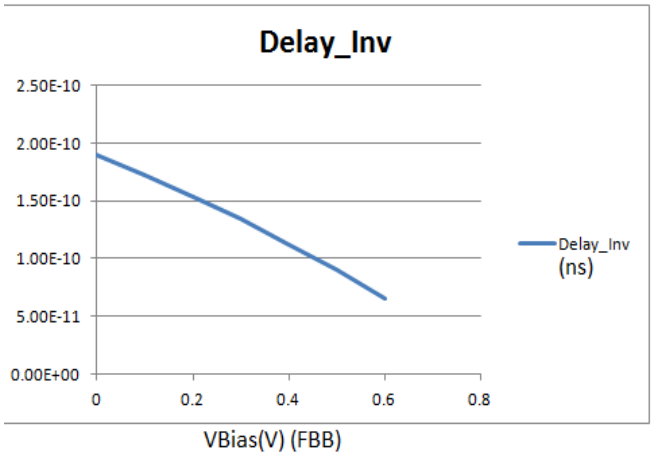

Fig 5. VBias VsDelay_Inv

Table 3: Inverter Leakage valuesfor different VBias (RBB) values

Vbias	Leakage_Inv
0	2.33E-11
-0.1	1.66E-11
-0.2	1.29E-11
-0.3	1.09E-11
-0.4	9.93E-12

Fig 6 plots the VBias VsLeakage of an Inverter. Maximum performance is calculated with respect no BB, VBias=0v.

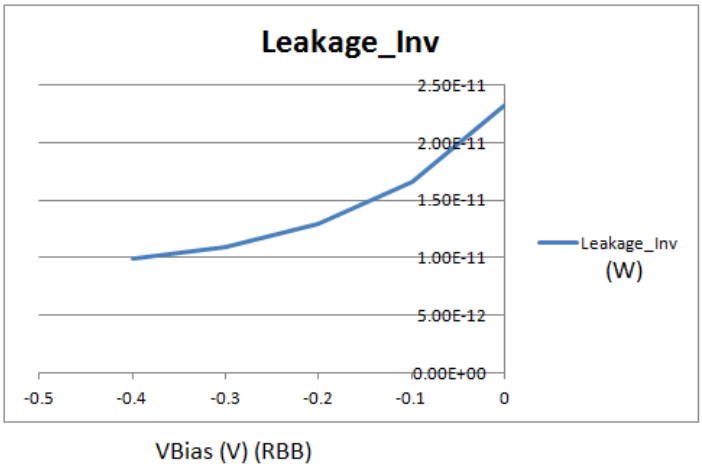

Fig 6. VBias VsLeakge_Inv

B. 3-bit Ripple Counter (RC)

Table 4 shows the performance increase of aripple counter by forward body biasing the design during high frequency operation, a maximum of 55% decrease in delay is observed and Table 5 shows the leakage reduction observed by reverse body

biasing the design during low frequency operation and decrease of 70-90%in leakage power is observed for different constant dc voltages.

Table 4:Ripple Counter delay values for different VBias (FBB) values

Vbias	Delay_RC
0	3.85E-10
0.1	3.62E-10
0.2	3.37E-10
0.3	3.11E-10
0.4	2.85E-10
0.5	2.57E-10
0.6	2.30E-10
0.8	1.71E-10

Fig 6 plots the VBias VsDelay_RC from the Table 4 data, showing decreasing delay with FBB.The leakage values of ripple counter are simulated for different dc values for the clock and reset signal. The simulated values are in Table 5 & 6.

Fig 8 & 9 plots the Table 5&6 showing decreasing leakage power with RBB.

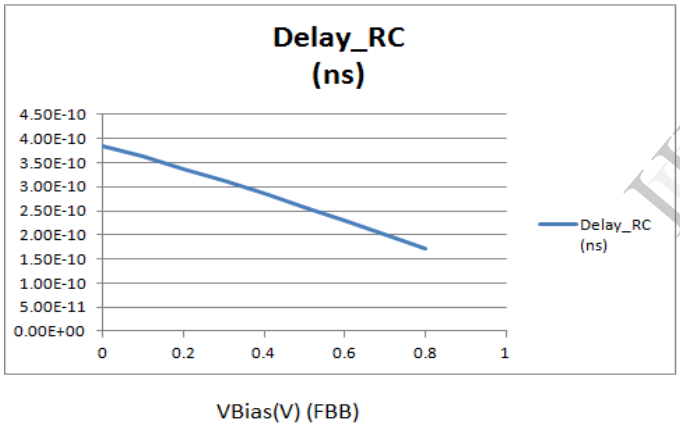

Fig 7. VBias VsDelay_RC

Table 5: Ripple Counter Leakage values for different VBias (RBB) values

RS	1.2v
CK	1.2v
Vbias	Leakage_RC (W)
0	9.14E-05
-0.1	8.35E-05
-0.2	4.19E-05
-0.3	2.36E-05
-0.4	3.64E-10

Table 6: Ripple Counter Leakage values for different VBias (RBB) values

RS	1.2v
CK	0v
Vbias	Leakage_RC (W)
0	1.62E-05
-0.1	4.36E-10
-0.2	4.08E-10
-0.3	3.93E-10
-0.4	3.85E-10

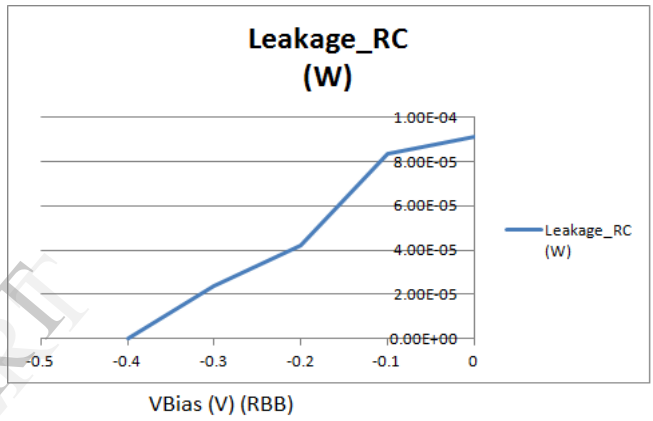

Fig 8. VBias VsLeakage_RC

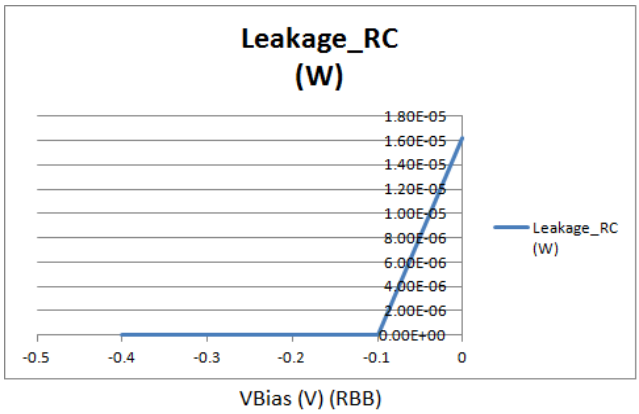

Fig 9. VBias Vs Leakage_RC

Under the above two simulations using BBG the performance parameters of the BBG should not vary. To prove this the performance parameter delay of BBG is observed for both the cases.Table 7 shows the delay values of Inverter, ripple counter and BBG for both the cases.

Fig 9 plots the Table 7 to show that delay of BBG for both the cases same. In the plot we can see the graph of BBGDelay_Inv and BBGDelay_RC are overlapped.

Table 7: BBG, Inv& RC delay values for different VBias

Vbias	BBG Delay_Inv	Delay_Inv	BBG Delay_RC	Delay_RC
-0.3	0.38723	1.76E-01	0.38724	0.4366
-0.2	0.387	1.62E-01	0.38724	0.42
-0.1	0.387	1.49E-01	0.38724	0.40015
0	0.38724	1.35E-01	0.38724	0.38197
0.1	0.38707	1.20E-01	0.38701	0.35675
0.2	0.38707	1.03E-01	0.38724	0.3328

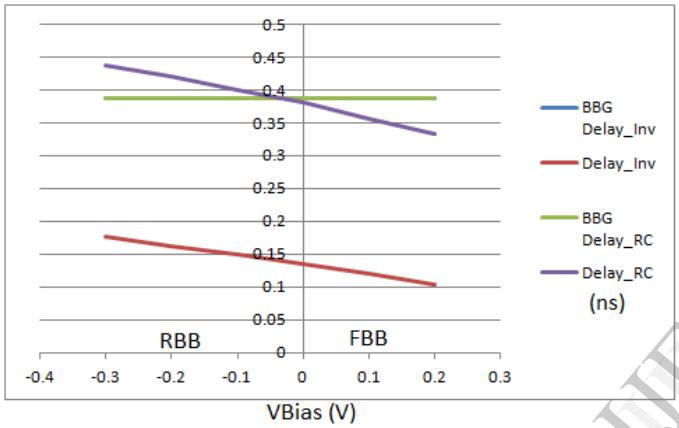

Fig 10. BBG delay VsInv& RC wrtVbias

V. CONCLUSION AND FUTURE WORK

The Adaptive Body Biasing technique has been shown to reduce the Leakage and Delay of the design in Low Power Mode and Active Mode respectively. Also it's proved that the BBG doesn't add any overhead in performance of the design except the area overhead.There's still lot of research work required in this domain. This work needs to extend it by using this concept of body biasing in processor designs and achieve decrease in the leakage powers in Low Power Mode and decrease in the critical path delays in Active Mode of Operations.

REFERENCES

[1]. Rinze Ida Mechtildis Peter Meijer," Body Bias Aware Digital Design"Eindhoven: Technische Universiteit Eindhoven, 2011.ISBN : 978-90-386-2920-9 NUR : 959

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[2]. ASHOK SRIVASTAVA and CHUANG ZHANG, "An Adaptive Body-Bias Generator for Low VoltageCMOS VLSI Circuits", ISSN: 1550-1329 print / 1550-1477 International Journal of Distributed Sensor Networks, 4: 213–222, 2008**.**

[3]. AshokaSathanuretal.,"Physically Clustered Forward Body Biasing for Variability Compensation in Nanometer CMOS design", 978-3-9810801-5-5/DATE0 2009 EDAA.

[4]. Sarvesh H. Kulkarni, Dennis M. Sylvester, Senior Member, IEEE, and David T. Blaauw,"Design-Time Optimization of Post-Silicon Tuned Circuits Using Adaptive Body Bias",IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 27, NO. 3, MARCH 2008

[5].B. Choi et al.,"Lookup table-based adaptive body biasing of multiple macros," in ISQED'07.

[6] T. Chen and, S. Naffziger, "Comparison of Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV) for Improving Delay and Leakage Under the Presence of Process Variation," *IEEE Transactions on VLSI Systems*, Vol.11, No.5, October 2003,pp.888-899.

[7] T. Kuroda, T. Fujita, S. Mita, T. Nagamatsu, S. Yoshioka, K. Suzuki, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu, and T. Sakurai, "A 0.9-V, 150-MHz, 10-mW, 4 mm2, 2-D Discrete Cosine Transform Core Processor withVariable Threshold-Voltage (VT) Scheme," *IEEE Journal of Solid-State Circuits*,Vol.31, No.11, November 1996, pp. 1770-1779.

[8] M. Miyazaki, H. Mizuno, and K. Ischibashi, "A Delay Distribution Squeezing Scheme with Speed-Adaptive Threshold-Voltage CMOS (SA-Vt CMOS) for Low Voltage LSIs," *Proceedings of ISLPED*, Monterey, CA, USA, August 1998, pp. 48-53.

[9] J. Tschanz, J. Kao, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De,"Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die ParameterVariations on Microprocessor Frequency and Leakage," *ISSCC Digest of TechnicalPapers*, San Francisco, CA, USA, February 2002, pp. 344-345.