

Optimised design for accumulator based 3 -weight pattern generation

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Abstract-In VLSI system, the largest research is mainly based on the efficient design of area, power, and speed. The accumulators used in current VLSI design saves the additional gates that are needed to implement the test registers and it avoids performance degradation. The accumulator can efficiently use to drive down the weight pattern generation for BIST applications. DDFS plays an important role in modern communication systems, especially for its interesting features such as high speed and fast frequency channel switching. The accumulator is the key element of DDFS system. The adder is the key element of accumulator. The optimization here is mainly based on the carry skip adder; a fast adder provides good compromise in terms of area and delay along with a simple and regular layout.

Keywords- Built-in-self-test schemes (BIST), Benchmark circuits, DDFS (direct digital frequency synthesis), pseudo random generators, weighted test pattern generation

I.INTRODUCTION

Pseudo random BIST generators have been successfully utilized for testing the integrated circuits and systems. The pseudo random generators include linear LFSR, cellular automata and accumulators accumulating a constant value. For achieving high fault coverage, large number of random patterns has to be generated for certain fault containing circuits. Therefore weighted pseudo random techniques have to be taken into account. In weighted pseudo random techniques, inputs are biased by changing the probability of a 0 or 1 on a given input from 0.5(for pure pseudo random tests) to some other value.

Weighted random pattern generations depending on a single weight assignment fails to achieve the complete coverage.in certain cases ,some faults may requires long test sequences to be detected.in order to overcome the drawbacks multiple weight assignments have been suggested, where different faults require different biases of the input condition applied to the circuit.To ensure that are relatively small

number of patterns can detect all faults [4].the methods for deriving the weight assignments for a given deterministic tests can allow complete fault coverage with small number of patterns.

In order to minimize the hardware implementation cost, the schemes based on multiple weight assignments utilizes the weights of 0, 1 and 0.5. This approach apart from reducing the hardware overhead, it has some beneficial effects on consumed power. Current VLSI circuits, e.g., data path architectures, or digital signal processing chips commonly contain arithmetic modules [accumulators or arithmetic logic units].this has fired the idea of arithmetic BIST(ABIST).the basic idea of ABIST is to utilize the accumulators for BIST schemes(especially for generation of test patterns).in [7] ,it was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudo random characteristics, if the input is properly selected. However, modules containing hard to detect faults require extra test hardware either by storing additional deterministic test patterns or by inserting test points into the mission logic.

II.WEIGHT GENERATION

The weights may be computed either by structural analysis or by extracting the required information from a recomputed deterministic test set. Methods based on structural analysis uses testability measures or heuristic to determine weights. The advantage of this method is the generation of very efficient weight sets in terms of the number of weight sets and number of patterns.

The first step in weight generation is to generate and simulate pseudo random patterns.

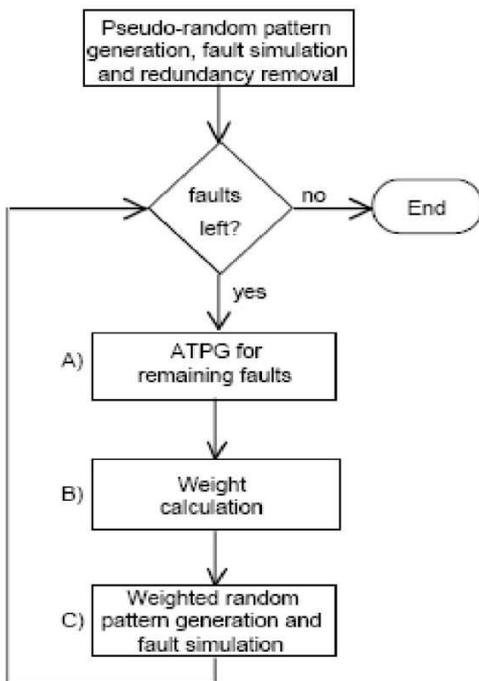


Fig.1 (a): Weight pattern generation.

The detected faults are highly random pattern testable and can be removed from the fault list for the remaining faults; redundancies are identified by a preliminary ATPG step. The redundant faults are removed from the fault list F and finally weight calculation is done for the remaining faults.

III. ACCUMULATOR BASED 3- WEIGHT PATTERN GENERATION

The accumulator based 3 weight pattern generations are given by an example. Let us consider the test set for the c17 benchmark circuit. According to this scheme, a weight assignment procedure would involve separating the test into two subsets S1 and S2 as follows: $S1=\{T1,T4\}$ and $S2=\{T2,T3\}$. the weight assignments for these subsets is $W(S1)={-, -, 1, -, 1}$ and $W(S2)={-, -, 0, 1, 0}$, where „-“ denotes a weight assignment of 0.5 ,a “1” indicates that the input is constantly driven by the logic “1” value, and “0” indicates that the input is driven by the logic “0” value. in the first assignment the inputs A[2] and A[0] are constantly driven by “1”, while inputs A[3] and A[4] are pseudo randomly generated (i.e. have weights 0.5). similarly ,in the second weight assignment (subset S2), inputs A[2] and A[0] are constantly driven by “0”, input A[1] is driven by “1” and inputs A[4] and A[3] are pseudo randomly generated.

Table1. Test set for c17 benchmark Circuit

Test vector	Inputs a[4:0]
T1	00101
T2	01010
T3	10010
T4	11111

The configuration of accumulator is given based on the following conditions: 1) an accumulator output can be constantly driven by “1” or “0” and 2) an accumulator cell with its output constantly driven to “1” or “0” allows the carry input of the stage to transfer to its carry output unchanged. This condition mainly leads to effectively generate the pseudo random patterns in the accumulator outputs whose weight assignment is “-”.

IV. DESIGN METHODOLOGY

The implementation of the weighted pattern generation scheme is based on the accumulator cell. it consists of full adder (FA) and D-type flip flop with asynchronous set and reset inputs whose output is also given to one of the full adder inputs. The set and reset are active high signals.

The session counter is used to alter the different weight sessions; the session counter consists of $\log_2 k$ bits, where k is the number of test sessions (i.e. weight assignments) of the weighted test set. The implementation of this scheme does not rely on a specific adder design.

The logic module provides the set [n-1:0] and reset [n-1:0] signals that drive the S and R inputs of the register A and register B inputs. The signals that drive the S inputs of the flip flops of register A, also drive the R inputs of the flip flops of register B and vice versa.

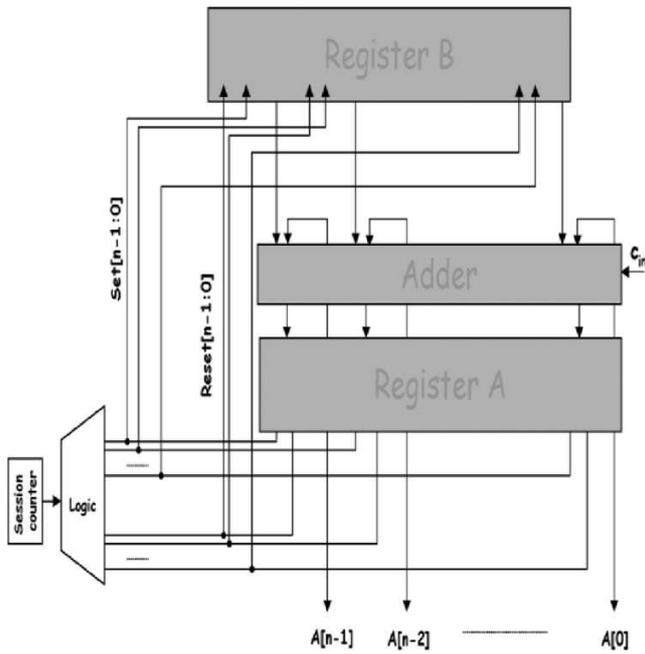


Fig3 (a): Accumulator Scheme

The accumulator was modeled using vhdl and simulated using modelsim 6.5b.

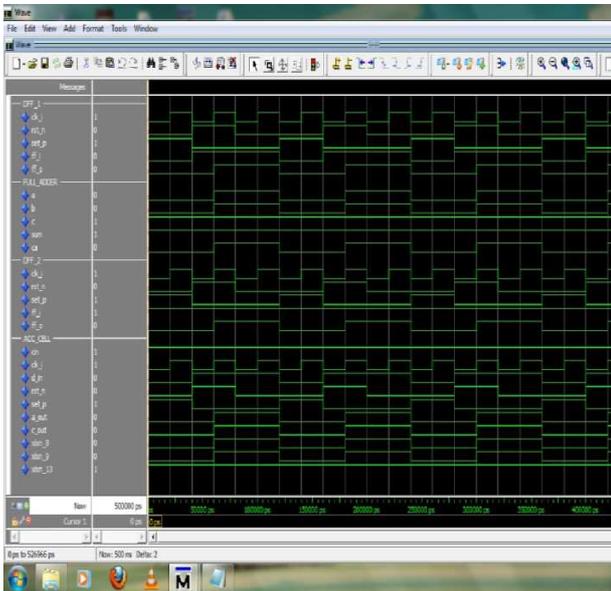


Fig: 4(a) simulation result of accumulator cell

V.DDFS USING ACCUMULATOR

Direct digital frequency synthesis (DDFS) have been widely used in software denied radios,Bluetooth and wireless transceivers. It can provide fast switching and high frequency resolution, over a wide band of frequency .DDS provides many advantages over PLL, such as fast settling time, frequency resolution and low phase noise .the architecture of high speed DDFS using accumulator is given below.

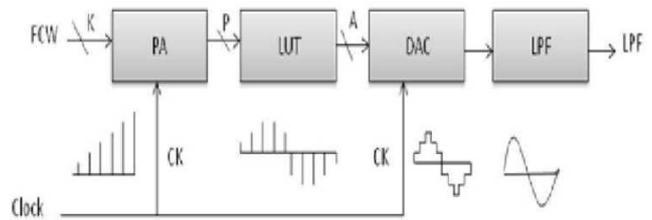


Fig: 5(a) Architecture of DDFS

The frequency control word (binary number) is loaded to accumulator. The accumulator is triggered by the system clock. The output frequency of the DDFS mainly depends on the following parameters, they are: f_{clk} (clock frequency), FCW (frequency control word), n (bit of the accumulator).the accumulator consists of a frequency register, adder and phase register.

The binary number in the phase register provides the main input to accumulator. The adder is the key element in accumulator; therefore it was necessary to improve the performance of adder. The look up table converts the discreet phase into amplitude of sinusoidal waveform. The DAC (digital to analog converter) transforms the digital representation of the sinusoidal signal waveform to analog. The filter is used to remove the unwanted signals.

To achieve the high speed in DDFS, the following criteria"s have to be taken into account: high speed operation is one of the important requirements in a DDFS system. The accumulator is a key element of the DDFS system and adder is the core of the accumulator. Therefore, the improvement of the adder design can lead to the increasing speed of the accumulator for DDFS. The speed can be achieved by using the carry skip adder, which is a fastest adder.

VI.CONCLUSION

Weighted pseudo random test generation methods that uses three weights namely 0, 0.5 and 1 have been efficiently utilized in BIST circuits to achieve complete fault coverage. Since accumulators are commonly found in current VLSI circuits e.g. data path architectures, or Digital Signal Processing chips, the utilization of accumulators for the purposes of BIST, including the generation of test patterns. An accumulator using full adder circuits has been designed. Here the accumulators of adder circuits need not to be redesigned. Hence results in the significant reduction of hardware, thereby increasing the operational speed of the circuit. The design of carry skip adder in accumulator of DDFS will increase the speed and performance. These adders are suitable for highly parallel and low cost applications.

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