International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 03, March-2015

Operation of Parallel Inverters for Power Quality Enhancement and Interfacing Distributed Energy Resources

B. Uday kumar
Electrical & Electronics Engineering
SVU College of Engineering
Tirupathi, India

Prof. A. Lakshmi Devi
Electrical & Electronics Engineering
SVU College of Engineering
Tirupathi, India

***Abstract*—The work done in this paper is mainly focused on integration of renewable energy sources to utility grid simultaneously with enhanced power quality using parallel inverters. Two voltage source inverters (VSI) are connected in parallel at load point i.e., point of common coupling (PCC) for power quality enhancement and interfacing renewable energy source to utility grid. One VSI is operated in voltage control mode (VCM) and the other one is operated in current control mode (CCM). Load terminal voltage at desired magnitude is regulated by VSI operating in VCM, whereas VSI operating in CCM connects distributed energy resource to utility grid. Switching algorithm for VSI is derived using dead beat control.**

Keywords*—Voltage source inverter, Voltage control mode, Current control Mode, Voltage regulation.

I. INTRODUCTION

The load system connected to the utility grid system are mainly unbalanced inductive and nonlinear loads. Such a load profile not only increases the energy loss but also corrupt the current waveforms deteriorating the quality of power. Moreover excessive dependence on fossil fuel and ever increasing demand for energy has widened the demand supply gap subject to the fact that rate of consumption of fossil fuels is far more than the rate at which they get replenished. Fossil fuels like coal, natural gas and oil are not only exhaustible but are also known to have disastrous environmental and health consequences. This has diverted the attention from fossil fuels to renewable sources of energy like the sun, wind, tidal energy etc. Most renewable source are distributed in nature, there-by eliminating the necessity for transmitting energy over long distance, these distributed energy resource (DER) will reduce the stress on conventional power system network. Available renewable energy sources can be grouped to from microgrid. Energy available can be pumped to utility grid by synchronizing microgrid to it.

This paper presents a power electronic interface which brings the solution to both the power quality and renewable energy source. Customary approach is [6] adopted to address power quality issues which are mainly due to harmonic currents is either bypass harmonic currents, block them from entering into power system, or to compensate them by locally supplying harmonic currents. Active filtering is done in [2] using custom power devices to inject current/voltage or both into system such that undesired harmonic components gets compensated. In order to address power quality issues and to inject real power, two inverters are connected in parallel shown in fig. 1. One inverter operates in voltage control mode (VCM) and second inverter operates in current control mode (CCM).

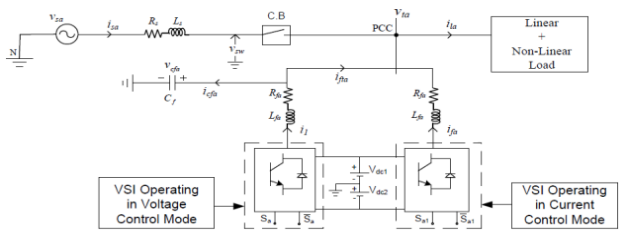


Fig 1. Single line diagram of suggested scheme

Though solution for same problem are suggested by extending the series-shunt compensation techniques usually employed by using custom power devices in [10] these suggested solutions employs an injection transformer to take care of series compensation which results in more losses compared to shunt compensation technique alone.

The operating algorithm of the VSI operating in VCM ensures that irrespective of the distortion or unbalance in the source voltage and non-linearity in load currents balanced fundamental sinusoidal voltages are maintained at point of common coupling (PCC). The VSI operating in CCM used only for interfacing DER to utility grid. CCM inverter injects real power at PCC. The common DC-link voltage can be derived from the renewable energy source in microgrid. VSI operated in VCM is rated for reactive power, whereas inverter operated in CCM has rated for active power.

II. MODELING OF VOLTAGE SOURCE INVERTER

A. VSI In Voltage Control Mode

In this section operation of VSI in voltage control mode is explained. A conventional power system is mostly interconnected. Hence there are more chances that voltage profile at particular bus get unbalanced or distorted due to nature of load at that particular bus or also due to disturbances at any part of the system. VSI can be used to maintain voltage at PCC at a pre-specified value. VSI is realized by two level neutral-clamped voltage source converter (VSC) and connected at PCC shown in Fig. 2. Here PCC may referred as terminal. A filter capacitor (C_f) is used in parallel with the VSC

circuit to provide a path for the high-frequency components. Here v_{si}, R_{si}, L_{si} are thevenin's equivalent, where i is phase a, b, c. By controlling injected currents i_{fia}, i_{fib}, i_{fic} VSI achieves its objective.

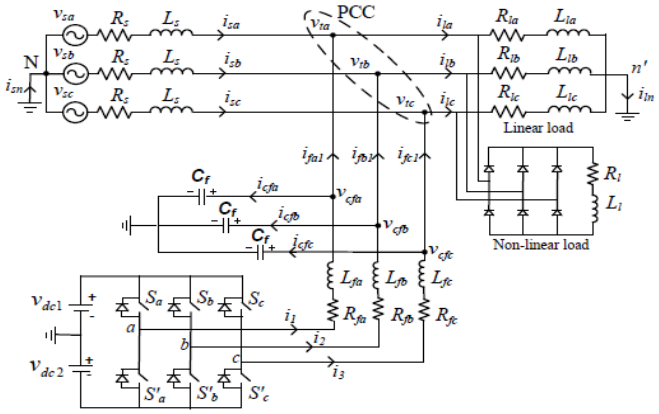


Fig 2. Voltage source inverter circuit connected at PCC

This scheme facilitates independent control on VSI each leg. Therefore single-phase modeling of VSI is sufficient to realize the operation. A single phase equivalent of VSI connected at PCC is shown in fig. 3. A detailed state space model of VSI in VCM mode is obtained and used to derive control signals.

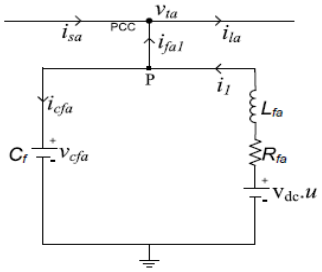


Figure 3. Single phase equivalent of VSI connected at PCC

It is considered that VSI and L-C filter can regulate voltage and injects currents at PCC. Here V_{dc1}=V_{dc2}=V_{dc}. u, a control variable, is considered as u_{cv}. Control variable can be either -1 or +1 depends on switching state. Both switches in one leg is operated in complementary manner, i.e. if upper switch is in ON then lower switch is OFF state, control signal u = +1 and vice versa. Current through inductor and voltage across capacitor are taken as state variables, therefore two state variables are v_{fc} and i_{fi}. State space equations given as follows:

$$\frac{dv_{fc}}{dt} = \frac{1}{C_{fc}} i_{fi} - \frac{1}{C_{fc}} i_{ft} \quad (1)$$

$$\frac{di_{fi}}{dt} = -\frac{1}{L_f} v_{fc} - \frac{R_f}{L_f} i_{fi} + \frac{V_{dc}}{L_f} u_{cv} \quad (2)$$

Above (1) and (2) equations are combined in standard state space equations as

$$\dot{x} = Ax + Bz \quad (3)$$

where,

$$A = \begin{bmatrix} 0 & 1/C_{fc} \\ -1/L_f & -R_f/L_f \end{bmatrix}, B = \begin{bmatrix} 0 & -1/C_{fc} \\ V_{dc} & 0 \end{bmatrix}$$

$$x = [v_{fc} \quad i_{fi}]^t, z = [u_{cv} \quad i_{ft}]^t$$

Equation (3) given continuous form, represented in discrete time form as follows:

$$x(k+1) = Gx(k) + Hz(k) \quad (4)$$

where, G and H matrix are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}, H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$$

From (4), capacitor voltage given as

$$v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11} u_{cv}(k) + H_{12} i_{ft}(k) \quad (5)$$

Let v_{tref} be the reference (nominal) voltage to be maintained at the PCC. So the cost function is chosen as

$$J = \left[v_{tref}(k+1) - v_{fc}(k+1)\right]^2 \quad (6)$$

Condition for minimum cost function is

$$v_{fc}(k+1) = v_{tref}(k+1) \quad (7)$$

Finally from (5) and (7) reference control law can be given as

$$u_{cv}^*(k) = \frac{v_{tref}(k+1) - G_{11} v_{fc}(k) - G_{12} i_{fi}(k) - H_{12} i_{ft}(k)}{H_{11}} \quad (8)$$

Expression for reference voltage to be obtained to implement above equation (8). v_{tref} magnitude can be chosen arbitrary. Here we chosen equal magnitude that of source voltage, but phase difference must be present between source and terminal voltage to ensure compensation of power losses in inverter done by source. Instantaneous power loss in inverter (p_{sh}) is given as

$$p_{sh} = v_{fca} i_{fta} + v_{fcb} i_{ftb} + v_{fcc} i_{ftc} \quad (9)$$

Reference voltages given as

$$\begin{aligned} v_{trefa} &= v_m \sin(\omega t - \delta) \\ v_{trefb} &= v_m \sin(\omega t - 2\pi/3 - \delta) \\ v_{trefa} &= v_m \sin(\omega t + 2\pi/3 - \delta) \end{aligned} \quad (10)$$

Where, v_m is required terminal voltage ω is system frequency.

Average value of inverter power losses can be calculated using a moving average filter. This power loss is passed through PI controller, which gives output phase angle delta δ.

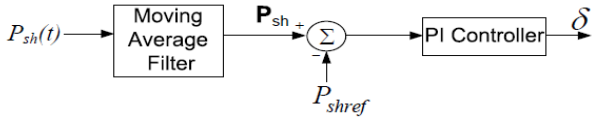


Fig. 4. Block diagram of voltage control

Control action mathematically represented as

$$\delta = K_p(p_{sh} - p_{shref}) + K_i \int (p_{sh} - p_{shref}) dt \quad (11)$$

Here it is to be noted in this case DC-link voltage obtained through renewable energy is assumed constant, hence there is no voltage loop to generate P_{shref}.

B. VSI in Current Control Mode

It is customary practice to connect Voltage Source Inverters (VSI) operating in current control mode (CCM) at PCC in parallel with load to cancel the distortion caused by the load, such that current drawn by the compensated load is pure balanced sinusoidal. This compensation is known as shunt compensation. Usually the main objectives in a 3 phase 4-wire system by operating VSI in CCM are:

1. Provide balanced supply current such that its zero sequence component is zero.
2. To have a predefined power factor from source.
3. Power supplied from source must be equal to average load power.

With a VSI operating in VCM connected at PCC as discussed in previous section, ensures that the objective no.1 enumerated above is met. Since one of the VSI's connected at PCC is operating in VCM pre-defined power factor from source can't be achieved. In case of grid-connected inverters the primary objective is to inject power. Hence the main purpose of connecting a VSI operating in CCM at PCC is to inject only real power. The circuit diagram of the system with two inverters connected in parallel is shown in the Fig. 5.

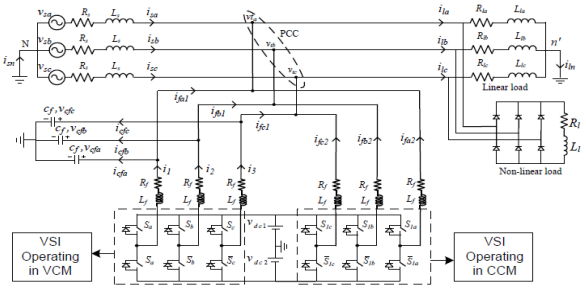


Fig. 5. Circuit diagram of parallel grid connected inverters

Above figure VSI operating in CCM injects real power to PCC. Whereas another VSI maintains voltage magnitude at desired value at PCC. This helps VSI in CCM to inject real power at PCC to load. The excess active power from VSI operating in CCM pumps back to source after meeting local load connected PCC.

III. SWITCHING CONTROL

As stated earlier, the switching variable u can take values either ±1 depending on the switching state of the top switch and bottom switch of a leg in the inverter. The voltage across each battery unit is maintained at V_{dc}. In Fig.2 S is the status of the top switch, and its complementary being the status of bottom switch in the same leg and the subscript represents the phase of the inverter. Therefore, through switching the inverter supplies a voltage $\pm V_{dc}$. This is represented as $V_{dc}u$ in Fig. 3, the Variable u controls the status of the inverter switches through gate drive circuits. The switching variable u is obtained from the continuous signal u_c by a hysteresis action around zero.

if $u_c(k) \geq h$, then $u = 1$
else if $u_c(k) \leq -h$, then $u = -1$

where h is hysteresis band prespecified. The value of h determines the frequency of switching.

As explained earlier the switching logic for VSI operating in VCM is derived using dead beat control action such that irrespective of the disturbances in the load or in the grid/source voltages, a balanced sinusoidal voltage of 1.0 p.u is maintained at PCC. In order to inject only real power at PCC with VSI operating in CCM, the switching logic for this inverter must be such that the currents injected are in phase with terminal voltage v_t.

In order to inject 1.0 p.u real power at PCC in phase a with v_{ta} being maintained at $1.0\angle -\delta$ by voltage control mode inverter, the reference current to be tracked by the VSI operating in CCM must be $1.0\angle -\delta$. For a 3 phase system reference currents to be tracked by current control mode inverter to inject 3.0 p.u real power are:

$$\begin{aligned} i_{faref} &= \sqrt{2}.(1.0)\sin(\omega t - \delta) \\ i_{fbref} &= \sqrt{2}.(1.0)\sin(\omega t - 2\pi/3 - \delta) \\ i_{fcref} &= \sqrt{2}.(1.0)\sin(\omega t + 2\pi/3 - \delta) \end{aligned} \quad (12)$$

The reference currents are tracked using a hysteresis controller

if $(i_{fa} - i_{fraef}) \geq h$ then $S_{1a} = 0$ and $\bar{S}_{1a} = 1$
else if $(i_{fa} - i_{fraef}) \leq -h$ then $S_{1a} = 1$ and $\bar{S}_{1a} = 0$

Similarly i_{fb} and i_{fc} are tracked.

IV. SIMULATION RESULTS

The system shown in fig. 5 where two inverters are connected in parallel at PCC, has been simulated in Matlab/SIMULINK. The simulation results which corroborate the analysis made for voltage control mode and current control mode. The physical parameters for the system are tabulated in table 1 taken from [2].

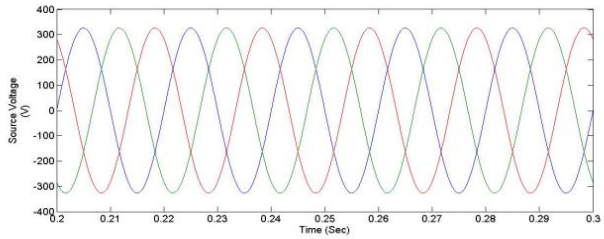
Table 1 System Parameters

System Quantities	Values
Nominal Source/grid voltage	326.26V ±10% (peak), sinusoidal and may exhibit swell, sag
PCC/Load bus voltage	326.26V(Peak), sinusoidal and balanced
Feeder impedance	1Ω, 10mH
Load parameters	40Ω, 0.2 H in each phase and a 3-ø diode bridge rectifier feeding R-L load of 100 Ω, 0.2 mH
Interfacing inductors (R_f, L_f)	0.2 Ω, 20mH connected to each leg of both VSI
Filter capacitors (C_f)	20 µF Across each phase of VSI operating in VCM
PI controller gains	$K_p = 9e^{-6}$, $K_i = 11e^{-6}$
Hysteresis band (h_1, h_2)	1 V, 0.5 A
DC link Voltage	$V_{dc1} = V_{dc2} = 600$ V

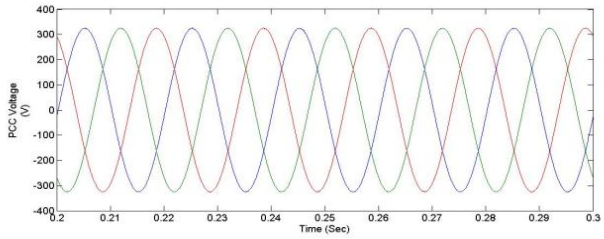
Detailed simulation results are presented in this section. Here demonstrated that VSI is able to maintain the PCC voltage at the nominal value irrespective of voltage variations in source and load changes.

Results shown in fig. 6 are only with VSI operating in VCM connected PCC. From fig. 6((a), (b), (c), (d), (e)) it can be concluded that when are at nominal value (326.26 V peak) and load current are non-sinusoidal the VSI injects filter currents filter currents as shown, to maintain voltage at PCC

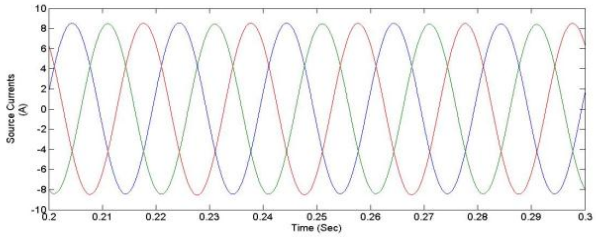
balanced 1 p.u. pure sinusoidal currents are drawn from source. It can also observed that source currents lead respective source voltages, since reactive power is supplied by compensator/VSI to source also in addition to load.



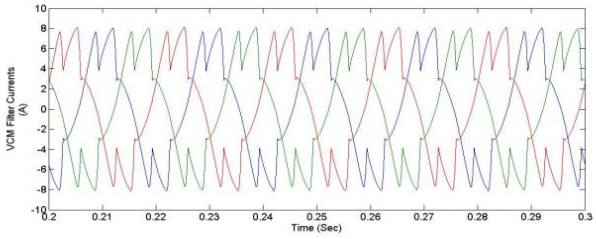
(a)



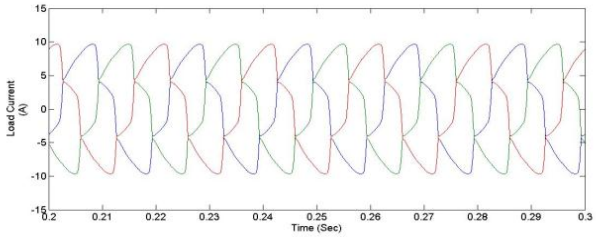
(b)



(c)

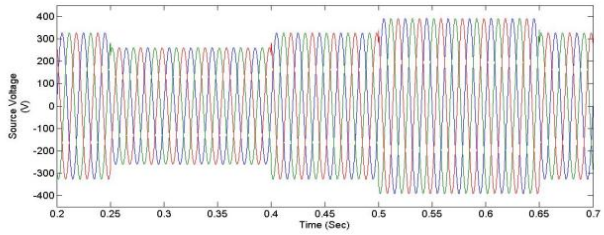


(d)

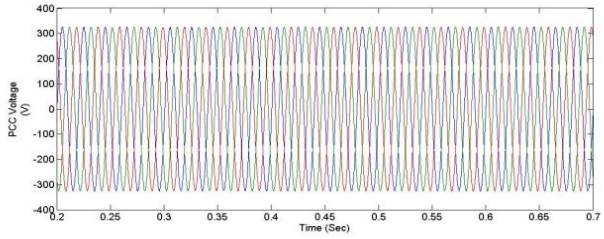


(e)

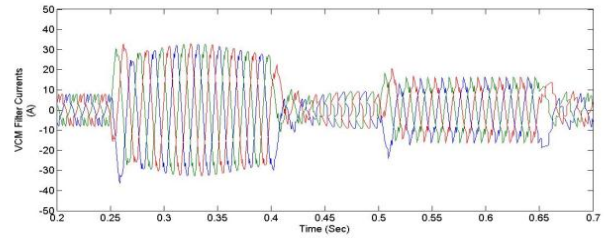
When there is sag in the source voltage in order to maintain PCC voltage at nominal value the VSI has to inject more current compared to the situation when source voltage at nominal value. Fig. 6((f) (g) (h)) shows source voltage, PCC voltage and filter currents with 20% sag and 20% swell in source voltage. It is clearly shown that during sag and swell filter injects more current to PCC to maintain voltage at nominal value 1 p.u. filter currents depending on the situation maintains PCC voltage at 1 p.u. (326.26 V) which is shown in fig. 6 (h).



(f)



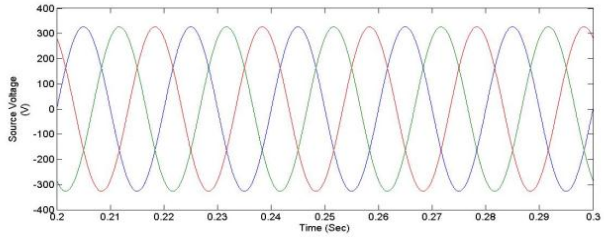
(g)



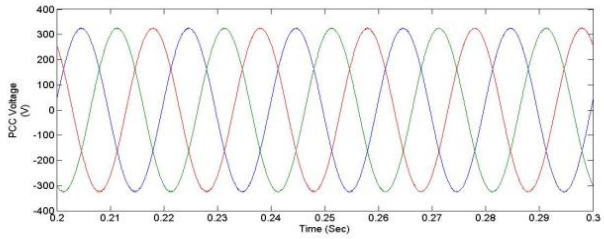
(h)

Fig.6 (a) Source Voltage (b) PCC Voltage (c) Source Currents (d) Filter currents (e) Load Currents (f) Source Voltage with Sag and Swell (g) PCC voltage during (h) Filter Current during Sag and Swell, with only one VSI operating in VCM mode connected at PCC

When both VSI are connected at PCC, the source voltage at nominal value, with non-linearity in the load currents. So, in order to maintain 1.0 p.u. balanced sinusoidal voltage at PCC, currents i_{fa1}, i_{fb1}, i_{fc1} are injected by VSI operating in VCM as shown in fig 7(d). Hence current drawn from source are pure sinusoidal shown in (c). i_{fa2}, i_{fb2}, i_{fc2} are the currents injected by VSI operating in CCM to inject active power shown in fig 7 (e).



(a)



(b)

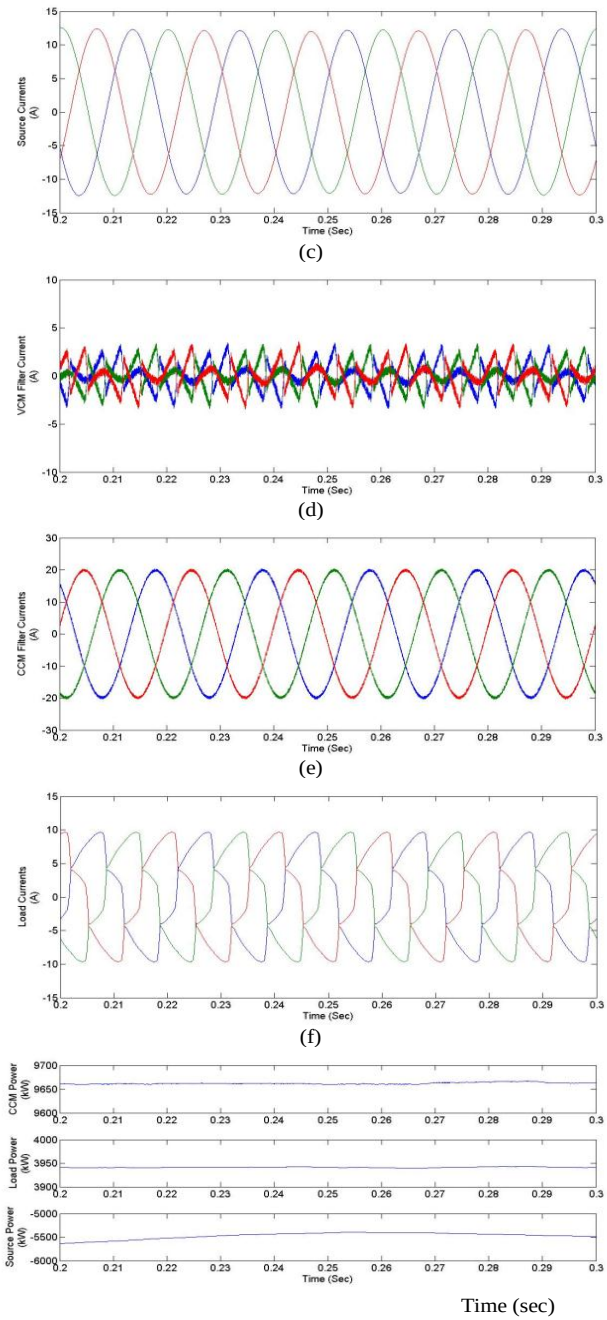


Fig.7 (a) Source Voltage (b) PCC Voltage (c) Source Currents (d) VCM Filter currents (e) CCM Filter Currents (f) Load Currents (g) Active Source, Load and CCM powers when both VSI connected at PCC

As a consequence of which δ is negative to pump remaining active power to source after meeting the local load connected at PCC. Which can be clearly observed from the above fig. 7 (g).

When source exhibits sag and swell as shown in fig.8 (a) even though load currents are non-sinusoidal, the VSI operating in VCM injects i_{fa1}, i_{fb1}, i_{fc1} to ensure that PCC voltage are pure sinusoidal and maintained 1.0 p.u. subsequently source currents are sinusoidal.

VSI in CCM mode injects i_{fa2}, i_{fb2}, i_{fc2} to inject active power at PCC. Both Filter currents VSI operating in VCM mode and VSI operating in CCM mode are shown in fig.8 (c) and (d) respectively.

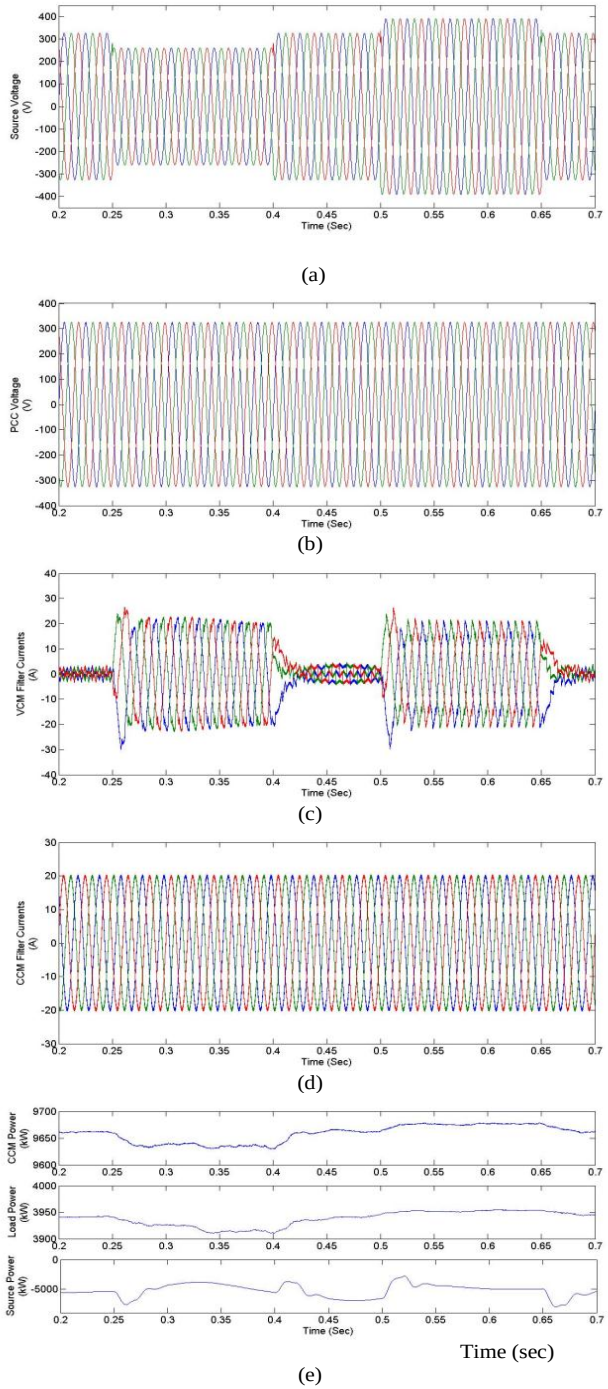


Fig.8 (a) Source Voltage, (b) PCC Voltage, (c) VCM Filter Current, (d) CCM Filter Current, (e) Source, Load and CCM power when both VSI are connected at PCC.

In fig.8 (e) shows source, load and CCM active powers from figure it clearly depicts that VSI in CCM pumps excessive power to source after meeting the local load demand.

V. CONCLUSIONS

In this work, a detailed study has be done for integration of distributed energy resources to utility grid to inject real power. Simultaneously enhancement of power quality is done. To achieve above two objectives the scheme of connecting two inverters in parallel at load bus with two modes of operation is suggested. It has been shown that VSI operating in VCM able to maintain PCC voltage against load and source disturbances. Inverter operating in CCM injects only real power at PCC. If real power injected is more than load demand, rest will be pumped to source.

REFERENCES

1. W. Huang, M. Lu, and L. Zhang, "Survey on microgrid control strategies," Energy Procedia, vol. 12, no. 0, pp. 206 – 212, 2011, the Proceedings of International Conference on Smart Grid and Clean Energy Technologies (ICSGCE 2011).
2. Chandan Kumar, Mahesh K. Mishra, "A control algorithm for flexible operation of dstatcom for power quality improvement in voltage and current control mode," Drives and Energy Systems, International Conference on Power Electronics, December16-19, 2012.
3. Y. Li, D. Vilathgamuwa, and P. C. Loh, "Microgrid power quality enhancement using a three-phase four-wire grid-interfacing compensator," Industry Applications, IEEE Transactions on, vol. 41, no. 6, pp. 1707-1719, 2005.
4. H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," Industry Applications, IEEE Transactions on, vol. IA-20, no. 3, pp. 625 –630, may 1984.
5. M. K. Mishra, A. Ghosh, A. Joshi, and H. M. Suryawanshi, "A novel method of load compensation under unbalanced and distorted voltages," Power Delivery, IEEE Transactions on, vol. 22, no. 1, pp. 288 – 295, jan. 2007.
6. M. K. Mishra, A. Ghosh and A. Joshi, "Operation of dstatcom in voltage control mode," Power Delivery, IEEE Transactions on, vol.58, no. 1, pp. 258 – 264, 2003.
7. M. K. Mishra, A. Ghosh and A. Joshi, "A new statcom topology to compensate loads containing ac and dc components," in Power Engineering societyWinter Meeting, 2000. IEEE, vol. 4, pp. 2636-2641, 2000.
8. K. Palaniswamy, D.P. Kothari, Mahesh. K. Mishra, S. Meikandashivam, and I. J. Raglend, "Effective utilization of unified power quality conditioner for interconnecting PV modules with grid using power angle control method," International journal of electrical power systems, vol. 48, no. 0, pp. 131-138, 2013.
9. H. Fujita and H. Akagi, "The unified power quality conditioner: The integration of series active filters and shunt active filters," in Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE, vol. 1, jun 1996, pp. 494 –501 vol.1.
10. L. jetto, "deadbeat controllers with ripple-free requirement for siso discrete systems," control theory and applications, IEE proceedings, vol. 137, no. 5, pp. 323-328, 1990.