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Operation of D-STATCOM in Voltage Control Mode

Vamshi Sunku Mohan Kumar
UG student, Electrical and Electronics Dept
Bangalore Institute of Technology
Bangalore, Karnataka, India

Dr. H. B. Nagesh
Asso. Prof. , Electrical and Electronics Dept.
Bangalore Institute of Technology
Bangalore, Karnataka, India

***Abstract*- A Power quality problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure or a mis-operation of end user equipments. Utility distribution networks, sensitive industrial loads and critical commercial operations all suffer from various types of outages and service interruptions which can cost significant financial loss per incident based on process down-time, lost production, idle work forces etc. This paper presents steady-state distribution model with controls of a Flexible AC Transmission System (FACTS) controller, namely D-STATCOM to study their effect on voltage drop in distribution system. Simulation is carried out by MATLAB with Simulink toolbox to verify the performance of the proposed method.**

Keywords: FACTS, voltage drop, MATLAB/SIMULINK.

I. INTRODUCTION

Power distribution systems, ideally, should provide their customers with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency. However, in practice, power systems, especially the distribution systems, have numerous nonlinear loads, which significantly affect the quality of power supplies. As a result of the nonlinear loads, the purity of the waveform of supplies is lost. This ends up producing many power quality problems. Power quality phenomenon or power quality disturbance can be defined as the deviation of the voltage and the current from its ideal waveform. Faults at either the transmission or distribution level may cause voltage sag or swell in the entire system or a large part of it. Also, under heavy load conditions, a significant voltage drop may occur in the system. Voltage sag and swell can cause sensitive equipment to fail, shutdown and create a large current unbalance. These effects can incur a lot of expense for the customer and cause equipment damage.

Conventional compensation systems, such as capacitor banks, synchronous machines have been used for long to increase the power flow in steady state by controlling the voltage of the distribution network. It has been shown that transient stability as well as stability in permanent system of an electrical network can be improved if the compensation can react quickly using thyristors as switches and in particular the new controllable components in both opening and closing (IGBT).

To avoid losses by Joule effect on distribution lines caused by inductive currents and also avoid the voltage drops, we should compensate the reactive power. With the restructuring of Power Systems and with shifting trend towards distributed and dispersed generation, the issue of Power Quality is going to take newer dimensions. To solve this problem, power electronics controller based custom power devices are used. Based on results at the point of collapse, design strategies are proposed for the controller. A radial system is used to illustrate the application of proposed controller model.

Most of these compensators are efficient but still have some defects: high reaction time or harmonic generation. In electrical distribution there are two main families of applications based on three-phase voltage inverter structure. On the other hand, the systems called D-FACTS(Flexible AC Transmission System dedicated to the distribution network) and secondly, interfaces to connect to the network of decentralized energy producers. Two types of VSC-based compensators have been commonly used for mitigation of the voltage sags and swells and regulating the load voltage. The first one is a shunt device called D-STATCOM (Distribution Static Compensator) and the second one is a series device called DVR (Dynamic Voltage Restorer). Depending on their mode of connection, they behave as current sources (case shunt), or as voltage sources (case series). They are operated in closed-loop voltage-control, which is considered best from the point of view of precise and fast control against sudden variations in the supply voltage and the load.

The study presented in this paper is based on the control voltage for a shunt compensation of reactive power using D-STATCOM. A simple output voltage feedback control has been used for the operation of the VSC under closed loop.

II. VOLTAGE SOURCE CONVERTER

A voltage source converter is a power electronic device, which can generate a sinusoidal voltage of any required magnitude, frequency and phase angle. The VSC is used to inject the 'missing voltage' which is the difference between the nominal voltage and the actual. The converter is an energy storage, which will supply the inverter with a DC voltage. A widely used method is the two level or multilevel three-phase converters which shares a dc capacitor between all phases. The purpose of this capacitor is mainly to absorb harmonic ripple and hence it has a relatively small energy storage requirement, particularly when operating in balanced conditions. The size of this capacitor has to be increased if needed to provide voltage support in unbalanced conditions. The solid-state electronic device (IGBT) in the inverter is then switched to get the desired output voltage.

IGBT is a three terminal controllable switch that combines the fast switching times of the MOSFET with the high voltage capabilities of the GTO used as a switching device in VSI. Normally the VSI is not only used for voltage dip mitigation, but also for other power quality issues, e.g. flicker and elimination of line harmonics, improve voltage regulation and power factor correction.

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Another important component in VSC is DC link capacitor. While the reactive power is generated internally by the switching action of the converter, a DC capacitor must still be connected to the input of the VSC. The main reasons for this are to provide a voltage source and circulating path for the current. The selection of a DC link capacitor is a trade-off between two things:

1. The response time of the D-STATCOM to variations in the required output. A smaller capacitor ensures faster response times.
2. Ripple voltage on the capacitor should be less than 10% of the nominal capacitor voltage. Larger capacitors are better in this regard, they are also better for lowering harmonic distortion on the AC side.

However, second harmonic appears in the DC bus voltage under unbalanced load currents or unbalanced voltages. By considering the second harmonic ripple voltage across the capacitor, the capacitance is calculated as,

$$C_{DC} = I_0/(2w.v_{DC,\,pp}) \quad (1)$$

where I_0=the capacitor current, w=is the angular frequency, and $v_{DC,\,pp}$= the ripple in capacitor voltage.

Considering the ripple as 5%, $v_{DC,\,pp}$= 0.05*360= 18 V, I_0= 50000/360= 138.88 A, C_{DC} is obtained as 12,286.7 µF. Thus, each capacitance is chosen to be 12,500 µF.

Figure 1 shows a six-pulse, controlled bridge rectifier connected to an ideal three-phase source with commutating inductances included in each phase. Only two thyristors will conduct at any time, one on the top half of the bridge and one on the bottom half of the bridge. Also, in order to have a voltage across the load, the two conducting diodes must be in different legs of the bridge, e.g., diodes 1 and 4 cannot be on at the same time.

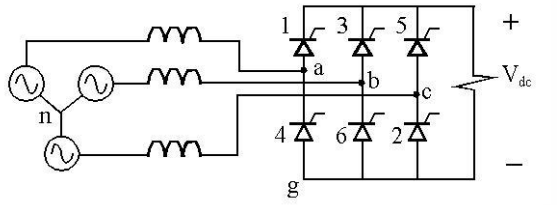

Fig.1: Schematic of six-pulse, controlled bridge rectifier with commutating inductance

Fig.2 shows phasor representation of waveforms of the six line-line voltages that are available from the three-phase source. There are six waveforms because polarity must be considered, i.e., the voltage from a to b is the opposite of the voltage from b to a. The voltage of a to b would be delivered to the DC load if diodes 1 and 6 are conducting, while the voltage of b to a would be delivered when diodes 3 and 4 are conducting.

The diodes that are ON at any given time are determined by which line to line voltage has the highest magnitude at that point in time. Thus at t=0, the voltage from c to b, V_{cb}, is the highest. Referring back to Fig.1, diodes 5 and 6 would be conducting. At 30 degrees, the voltage V_{ab} becomes higher than V_{cb}, causing diode number 1 to become forward biased and diode 5 to be reversed biased. As a result, the current transfers from diode 6 to diode 1.

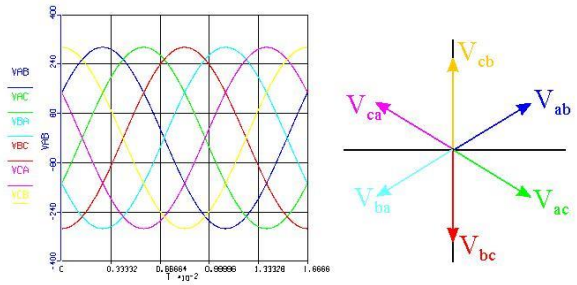

Fig.2: Waveforms and phasors of voltages that make up the output DC voltage

Equation 2 gives the average DC value for the uncontrolled case (zero firing delay). In this equation, V_{rms} is the rms value of the line to neutral phase voltage in the Wye-connected source. Thus, there is a factor of the square root of two accounting for the peak value of the sinusoidal waveform, while the square root of three factor accounts for the difference in magnitude of the line-line voltage as compared to the line-neutral voltage.

Equation 3 provides the average DC voltage when the thyristor is operated with a delay angle. Clearly, if the delay is zero, equation 3 reduces to equation 2.

$$Vdc = \frac{3\sqrt{3}\sqrt{2}\,Vrms}{\pi} \quad (2)$$

$$Vdc = \frac{3\sqrt{3}\sqrt{2}\,Vrms}{\pi}\,cos\alpha \quad (3)$$

In reality, it is impossible for the current in one phase and thyristor to instantaneously transfer the current to another phase and thyristor because there is inductance in both the source and in each thyristor.

III. CONTROLLER

Maintain constant voltage magnitude where a sensitive load is connected, under system disturbances. The control system only measures the r.m.s voltage at the load point i.e. no reactive power measurements are required. The VSC switching strategy is based on a PWM technique which offers simplicity and good response. Also PWM is used to vary the amplitude and the phase angle of the injected voltage. PWM offer more flexible option. High switching frequencies improve efficiency of the converter. PWM is one of the most popular switching schemes used for VSCs. It compares an input (reference) sine wave to a fixed frequency triangular (carrier) wave and this allows the firing pulses for the solid state switches to be generated. The phase and magnitude of the fundamental component of the output voltage can be directly controlled by varying the magnitude and phase of the reference sine wave. The AC output contains harmonics based around multiples of the switching frequency can be chosen to optimize triple and low order harmonic elimination. The main reasons for this choice are that it combines simplicity with robustness to achieve the desired level of control. There are a number of different methods which are available to generate the required output from the VSC, the most popular methods are phase angle control and constant DC link voltage scheme. The phase angle control scheme is mainly employed in square wave control strategies i.e. FFS. The parameter which must be controlled is the phase angle α, this is the phase angle between V_{GRID} and V_{COMP} across the leakage reactance. This method is used to dynamically control the DC voltage magnitude.

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Control is achieved by increasing or decreasing α which results in further charging or discharging of the capacitor.

Typically, when a VSC is operated in PWM mode, the constant DC link voltage scheme is employed. Control is achieved by adjusting two parameters; α and also MA (PWM modulation index). α is controlled in order to control the rate of absorption of real power from the grid which supplies converter losses and maintains V_{DC} at a predetermined value. The reactive power transfer control loop functions by varying MA in order to vary the direction and amount of reactive power being transferred. This control strategy is traditionally implemented with a proportional and integral (PI) control algorithm.

The triangular wave (V_{TRI}) is at a constant frequency f_{SW} which determines the switching speed of the IGBTs. The modulating wave ($V_{CONTROL}$) which can be used to vary the amplitude, phase and frequency of the output is at the required fundamental frequency f_1. The amplitude modulation ratio or modulation index is defined as:

$$MA = V_{control}/V_{tri} \quad (4)$$

The frequency modulation ratio is defined as:

$$mf = f_{sw}/f_1 \quad (5)$$

The peak value of the fundamental component of the output voltage is given in as:

$$V_o = MA \times V_{dc} \quad (6)$$

Amplitude of the fundamental component of system is,

$$V_o = MA \times V_{dc}\ (MA<1) \quad (7)$$

Figure 5 shows the output of a VSC for a bipolar switching scheme. A single modulating wave is compared to a triangular carrier wave in order to generate the output which switches between two states, $+V_{DC}$ and $-V_{DC}$. Figure 6 presents the results of a Fourier analysis of the output. The output voltage harmonics appear at sidebands centred around the switching frequency and its multiples. This is defined by equation 8.

$$h = (l \times mf) \pm k \quad (8)$$

Where mf is chosen as an odd integer and h is the harmonic order, odd values of l result in harmonics only being present for even values of k and even values of l result in harmonics only being present for odd values of k. This is illustrated in Figure 6.

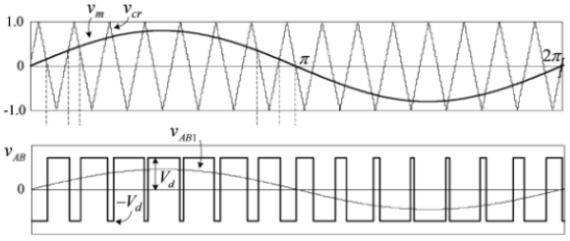

Fig 5: bipolar switching scheme-frequency spectrum

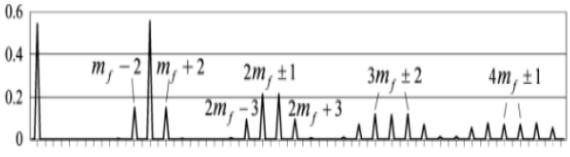

Fig 6: Bipolar switching scheme - frequency spectrum

The PI controller gain values are selected by using a trial and error method. As Figure 7 shows, the open loop step response of the system was not first order. This made practical use of an industry standard tuning rule such as Ziegler–Nichols or Cohen–Coon difficult. Figure 7 shows the response of V_{LOAD} to a steep increase in sending end voltage. Optimization of controller gain values is achieved by tuning each gain value individually starting with the reactive power controller, K_P (proportional gain) then T_i (integral action time). The same approach is taken for the active power controller. Gain values are initially set to zero, then increased while the system response is monitored with a focus on response speed and reliability.

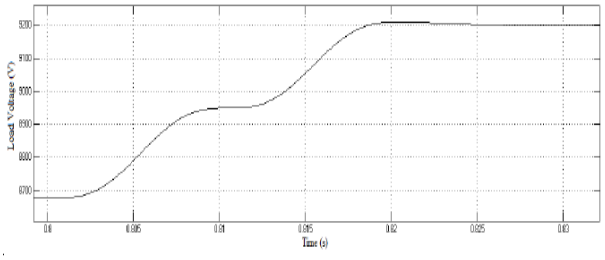

Fig 7: Response of VLOAD to a steep increase in sending end voltage.

IV. MODELLING OF D-STATCOM

D-STATCOM consists of a VSC, a dc energy storage device, a controller as shown in Figure 9. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the D-STATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

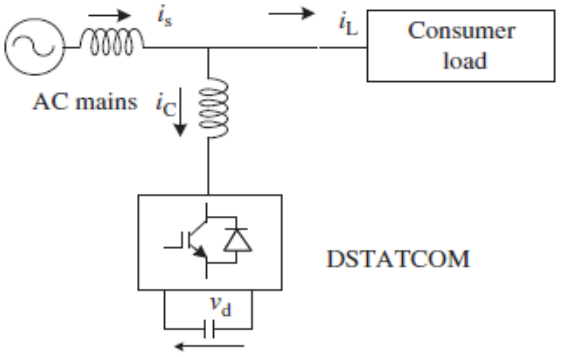

Fig 8: Schematic Diagram of D-STATCOM

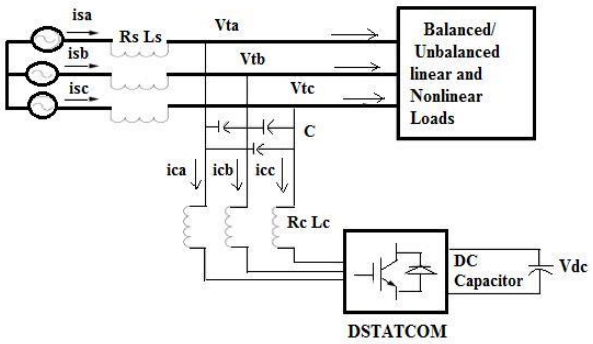

Fig 9: D-STATCOM connected to a three phase system

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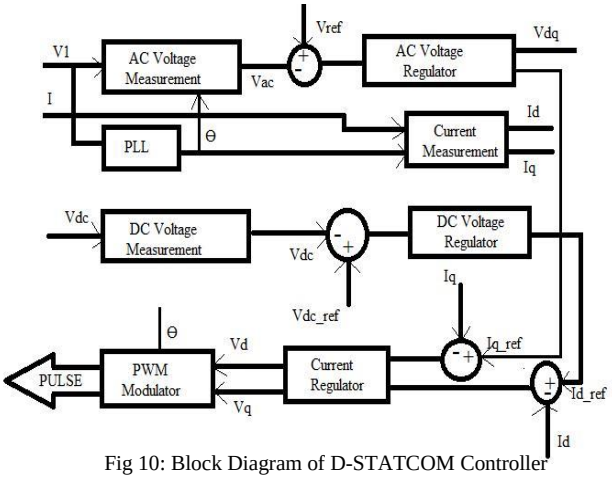

Fig 10: Block Diagram of D-STATCOM Controller

Phase Locked Loop (PLL) synchronizes the positive sequence component of the three phase primary voltage V_1. The output of the PLL($\sin\theta, \cos\theta$) is used to compute the direct-axis and quadrature-axis components of the AC three phase voltages (V_d, V_q) and currents (I_d, I_q) as shown in Figure 9. dq0 rotating reference frame is employed because it offers higher accuracy than the stationary frame based technique. Measurement system measuring the d and q components of AC positive sequence voltage and current to be controlled as well as DC link voltage V_{dc}. An outer regulation loop consisting of an AC voltage regulator and a DC voltage regulator. The output of the AC voltage regulator is the reference current I_{q_ref} and the output of the DC voltage regulator is the reference current I_{d_ref} for the current regulator. There are two PI regulators in the voltage controller block. The first one is responsible for controlling the terminal voltage through the reactive power exchange with the AC network. This PI regulator provides the reactive current I_{q_ref}. Another PI regulator is responsible for keeping DC voltage constant through a small active power exchange with the AC system compensating the active power losses in the transformer and inverter. An inner current regulation loop consisting of a current regulator. There are two PI controllers in the current regulator also. The current regulator controls the magnitude and phase of the voltages generated by the PWM inverters from the reference currents (I_{d_ref}, I_{q_ref}) produced respectively by the DC voltage regulator and AC voltage regulator (in voltage control mode). The V_d and V_q voltages are converted into phase voltages V_a, V_b, V_c which are used to synthesize the PWM voltages. The I_q reference comes from the outer voltage regulation loop (in automatic mode) or from a reference imposed by Q_{ref} (in manual mode). The I_d reference comes from the DC-link voltage regulator.

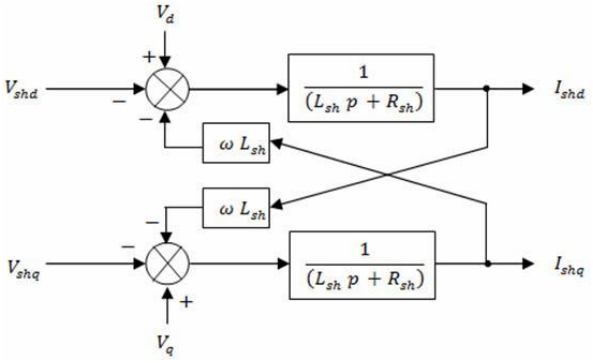

Fig 11: D-STATCOM Model

$$V_d = i_d * w_1 \quad (9)$$

$$V_q = i_q * w_1 \quad (10)$$

Selection of the DC Bus Voltage - The minimum DC bus voltage of the VSC of the D-STATCOM should be greater than twice of the peak of the phase voltage of the distribution system. The DC bus voltage is calculated as,

$$Vdc = \frac{2\sqrt{2}\,VLL}{\sqrt{3}\,m} \quad (11)$$

where m is the modulation index and is considered as 1 and V_{LL} is the AC line output voltage of the D-STATCOM. Thus, V_{DC} = 677.69V for a V_{LL} = 415V and it is selected as 700 V.

Selection of a DC Bus Capacitor - The value of the DC capacitor (C_{DC}) of the VSC of the D-STATCOM depends on the instantaneous energy available to the D-STATCOM during transients. The principle of energy conservation is Active Shunt Compensation applied as,

$$\frac{1}{2}Cdc(Vdc^2 - Vdc1^2) = K1 * 3VaIt \quad (12)$$

where V_{DC} is the nominal DC voltage equal to the reference DC voltage and V_{DC1} is the minimum voltage level of the DC bus, 'a' is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the DC bus voltage is to be recovered. Considering the minimum voltage level of the DC bus (V_{DC1}) =677.69V, V_{DC} = 700 V, V= 239.60V, I= 76.51A, t= 30 ms, a=1.2, and variation of energy during dynamics =10% ($k1$= 0.1), the calculated value of C_{DC} is 12882.75 µF and it is selected as 13000 µF.

Selection of an AC Inductor - The selection of the AC inductance (L_r) of a VSC depends on the current ripple $I_{cr,pp}$, switching frequency f_s, and DC bus voltage (V_{DC}) and it is given as,

$$L_r = \frac{\sqrt{3}\,m\,V_{DC}}{12a f_s I_{cr,pp}} \quad (13)$$

where m is the modulation index and a is the overloading factor. Considering $I_{cr,pp}$=15%, f_s= 1.8 kHz, m=1, V_{DC} =700V, and a =1.2, the value of L_r is calculated to be 4 mH. The round-off value of 4mH is selected in this investigation.

$$V_d = \frac{2}{3}[V_a sinwt + V_b \sin\left(wt - \frac{2\pi}{3}\right) + V_c \sin(wt + \frac{2\pi}{3}) \quad (14)$$

$$V_q = \frac{2}{3}[V_a coswt + V_b \cos\left(wt - \frac{2\pi}{3}\right) + V_c \cos(wt + \frac{2\pi}{3}) \quad (15)$$

$$V_o = \frac{1}{3}[V_a + V_b + V_c] \quad (16)$$

$$V_a = V_d sinwt + V_q coswt + V_o \quad (17)$$

$$V_b = V_d \sin\left(wt - \frac{2\pi}{3}\right) + V_q \cos\left(wt - \frac{2\pi}{3}\right) + V_o \quad (18)$$

$$V_b = V_d \sin\left(wt + \frac{2\pi}{3}\right) + V_q \cos\left(wt + \frac{2\pi}{3}\right) + V_o \quad (19)$$

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$$V_q = -V_q^* - wL_s i_q + V_{q\,ref} \quad (20)$$

$$V_d = -V_d^* - wL_s i_d + V_{d\,ref} \quad (21)$$

$$\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{L_s} & 0 \\ 0 & \frac{-R_s}{L_s} \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{1}{L_s} \begin{bmatrix} V_q^* \\ V_d^* \end{bmatrix} \quad (22)$$

$$\begin{bmatrix} V_q \\ V_d \\ V_o \end{bmatrix} = m \begin{bmatrix} sin\alpha \\ cos\alpha \\ 0 \end{bmatrix} V_{DC} \quad (23)$$

$$\text{modulation index m} = \frac{\sqrt{V_q^2 + V_d^2}}{V_{DC}} \quad (24)$$

$$\text{firing angle } \alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) \quad (25)$$

$$V_{DC} = \frac{1}{C} \int i_{DC}\, dt \quad (26)$$

$$i_{DC} = m(i_q \sin\alpha + i_d cos\alpha) \quad (27)$$

V. WORKING

The amplitude of the voltage of D-STATCOM may be controlled to adjust the quantity of reactive power to share with the network. In general, the voltage of D-STATCOM V_{sh} is injected in phase with the line voltage V_t, and in this case there is no exchange of energy with the active network, but only reactive power to be injected (or absorbed) by the D-STATCOM.

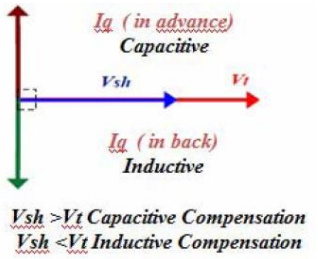

Fig 12: Phasor diagram of D-STATCOM

The reactive power exchange with the network is done by varying the amplitude of the output voltages. Depending on the amplitude of these tensions, the three following operating systems are available for the D-STATCOM. The basic principle of operation for a D-STATCOM is explained with the help of Figure.

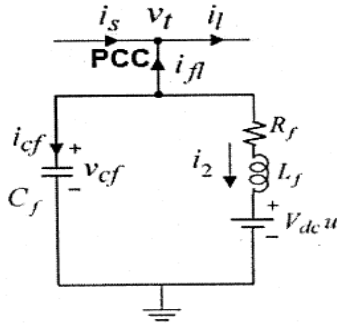

Fig 13: Single phase equivalent circuit of D-STATCOM

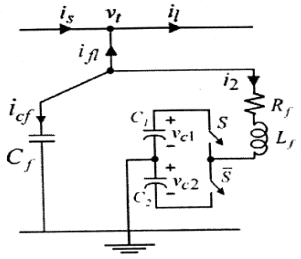

Fig 14: Equivalent circuit with DC source simplification

Figure13 shows the single phase equivalent circuit of D-STATCOM connected to the Point of Common Coupling (PCC). The D-STATCOM is realized by a two-level neutral-clamped VSC, as shown in Fig. 14. A filter capacitor (Cf) is used in parallel with the VSC circuit to provide a path for the high-frequency components. PCC voltage is terminal voltage in denoted by vt. Switching variable u is constrained to be ± 1. Here, there are two DC storage capacitors, namely, $C_1$and C_2. The voltage across each capacitor is maintained at V_{DC}. In Fig.14, S is the status of the top switch, bottom switch being complementary. This means for S=0(1) , the top switch is closed (open), while the bottom switch is open (closed) connecting the output of the inverter leg to $+V_{DC}(-V_{DC})$. Therefore, through switching the inverter supplies a voltage $\pm V_{DC}$. This is represented as $V_{DC}u$ in Fig.13. The variable u controls the status of the inverter switches through gate drive circuits. The switching variable u is obtained from the continuous signal u_c by a hysteresis action around zero, i.e.

if $u_c(k) > h$ then $u = 1$

else if $u_c(k) < -h$ then $u = -1$

where h is pre-specified hysteresis band- which determines frequency.

The output voltage of converter (V_{sh}) is controlled in phase with the system voltage (V_t) and the output current of the D-STATCOM (I_q) varies depending on V_{sh}. If:

1. $V_t < V_{sh}$: The phase angle of I_q is leading with respect to the phase angle of V_t by 90 degrees. Leading reactive power flows from the D-STATCOM (capacitive mode).
2. $V_t > V_{sh}$: The phase angle of I_q is lagging with respect to V_t by 90 degrees; the DSTATCOM consumes reactive power flows and is in inductive mode.
3. $V_t = V_{sh}$: No reactive power is delivered to the power system.

Lagging reactive power flows into the D-STATCOM (inductive mode). The amount of the reactive power is proportional to difference between V_t and V_{sh}. The variation of the output voltages amplitude is achieved by varying the direct voltage across the capacitor. The D-STATCOM can deliver a capacitive or inductive current independent of the network voltage. So it can provide the maximum capacitive current even at low voltage values. The structure and operational characteristic is shown in Figure 15. The D-STATCOM smoothly and continuously controls voltage from V1 to V2. However, if the system voltage exceeds a low-voltage (V1) or high voltage limit (V2), the D-STATCOM acts as a constant current source by controlling the converter voltage (Vi) appropriately.

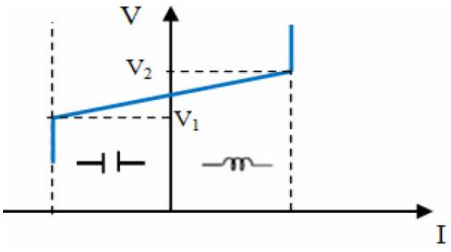

Fig.15: V-I characteristics of a D-STATCOM

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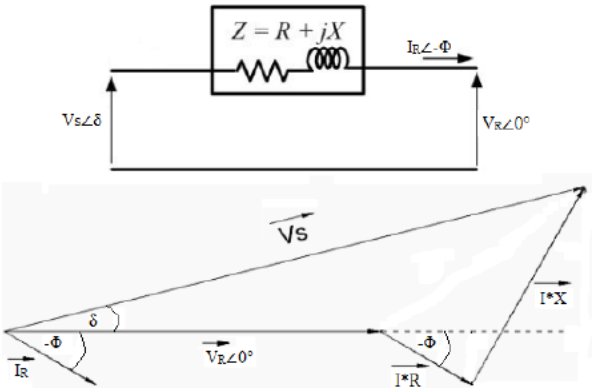

Fig 16: Uncompensated distribution line

In Figure 17, a shunt compensator has been installed at the receiving end. It compensates the reactive component of the current at the receiving end and hence the reactive component being drawn from the source is reduced or almost eliminated. An improvement in voltage regulation can be seen.

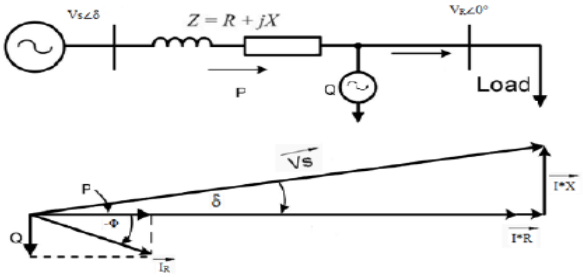

Fig 17: Distribution line with shunt compensation

Assuming a lossless line, and $I_S = I_R$ let the sending end voltage = $V_S\angle\delta$ and the receiving end voltage = $V_R\angle 0°$. The resistance of the line will be neglected as it tends to be much smaller than the inductance.

Therefore, from source:

$$\boldsymbol{I^*}=(|\boldsymbol{Vs}|\angle\boldsymbol{\delta}-|\boldsymbol{Vr}|\angle\boldsymbol{0})/\boldsymbol{X} \quad (28)$$

$$\boldsymbol{Sr}=\boldsymbol{Pr}+\boldsymbol{jQr}=\boldsymbol{Vr}^*\times\boldsymbol{Ir}^*=(|\boldsymbol{Vr}|\times|\boldsymbol{Vs}|\angle\boldsymbol{90\text{-}\delta})/\boldsymbol{X}-(|\mathrm{Vr}|^2\angle\boldsymbol{90})/\boldsymbol{X} \quad (29)$$

The real power over the line is :

$$\mathbf{Pr}=(|\boldsymbol{Vr}|\times|\boldsymbol{Vs}|\boldsymbol{cos}(\boldsymbol{90}-\boldsymbol{\delta}))/\boldsymbol{X}-((|\mathrm{Vr}|^2\boldsymbol{cos90})/\boldsymbol{X} \quad (30)$$

And from this:

$$\mathbf{Pr} = ((|\boldsymbol{Vr}| \times |\boldsymbol{Vs}|)/\boldsymbol{X}^*)\mathbf{sin}\boldsymbol{\delta} \quad (31)$$

Similarly, QR is :

$$\boldsymbol{Qr} = (|\boldsymbol{Vr}| \times |\boldsymbol{Vs}|\boldsymbol{sin}\ (\mathbf{90} - \boldsymbol{\delta}))/\boldsymbol{X} - ((|\mathrm{Vr}|^2\boldsymbol{sin90})/\boldsymbol{X} \quad (32)$$

This yields:

$$\boldsymbol{Qr} = \boldsymbol{Vr} \times (\boldsymbol{Vr} - \boldsymbol{Vscos\delta})\ /\boldsymbol{X} \quad (33)$$

$$|\boldsymbol{Vs}| - |\boldsymbol{Vr}| = \boldsymbol{Qr} \times \boldsymbol{X}\ |\boldsymbol{Vr}| \quad (34)$$

From equation 34, it can be said that the scalar difference between the voltages at either end of the line depends on the reactive power, i.e. transmitting reactive power causes a voltage drop across the line.

Shunt compensation improves system stability. Voltage stability refers to the ability of a system to return to the nominal (pre-fault) voltage at all buses following a disturbance. In a regular power system, the amount of real power transmitted depends on the transmission angle (δ), which is the phase angle between V_S and V_R. The reason for this is that the other parameters concerning power flow; sending end voltage and line impedance are typically fixed. So, as δ is increased, power flow increases. This is valid up to δ = 90°, at which point power flow is at its maximum. Any further increase in the angle δ will result in the system becoming unstable. Therefore system stability margins are employed and this results in δ being maintained below 35°. This in turn limits the transmittable power capacity of the line far below its thermal loading limit. The addition of shunt compensation at the midpoint of the line increases the stability margin of the system as proven in Figure 18 thus increasing the maximum power transfer capability of the line. The reason for this is that maximum power transfer now does not occur until δ = 180°.

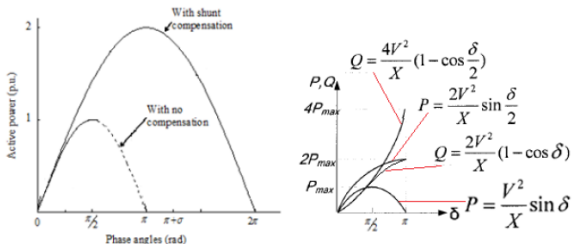

Fig 18: Transmission angle curve

Introduction of the midpoint shunt compensator, improves stability.

The real power transfer across the line is,

$$P = \frac{(2V)^2}{X sin\frac{\delta}{2}} \quad (35)$$

The reactive power generated by the compensator,

$$Q = \frac{(4V)^2}{X(1-cos\frac{\delta}{2})} \quad (36)$$

It can be said that compensating the reactive power at the receiving end of the line will reduce voltage drop across the line as given by equation 38.

$$V.\Delta V = RP + XQ \quad (37)$$

considering R≈ 0,

$$V.\Delta V = XQ,$$

$$\therefore V \propto Q \quad (38)$$

VI. SIMULINK MODEL OF D-STATCOM

I. Without D-STATCOM

Consider the voltage at the generating station level of 230kV. It is transmitted through the transmission line having resistance of 10Ω, inductance of 1mH and capacitance of 1uF. This voltage is stepped down to 400V using a 230kV/400V step-down transformer. This voltage is fed to a RL load say having R=12.1Ω and L=0.1926H. Consider another load connected in parallel with this load through a circuit breaker having step time of 1sec as shown in Figure 19. The second load is used to test the system's stability under sudden increase in load. This load draws more magnetizing current from the source which results in decrease in load voltage and power factor. If this condition persists for a long duration, it causes system instability due to unavailability of power and eventually results in load shedding. Rating of second load is taken as R=0.05Ω, L=0.0059H. Voltage at 1st load is measured. When the system is run, output voltage is at 400V from time t=0 to t=1sec. At t=1sec, step signal is given to circuit breaker which closes the contact. The second load gets connected and the voltage reduces.

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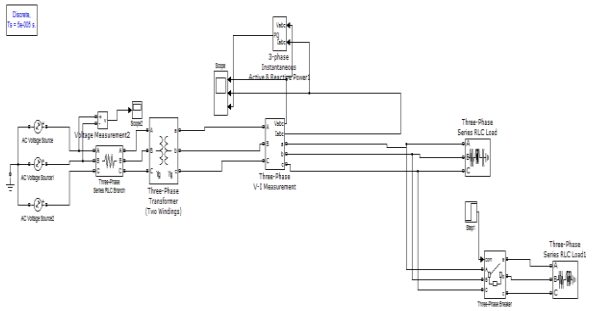

Fig 19: Test system without D-STATCOM

II. With D-STATCOM

Figure 20 shows power system with D-STATCOM. Voltage at 1st load is measured. When the system is run, output voltage is at 400V from time t=0 to t=1sec. At t=1sec, step signal is given to circuit breaker which closes the contact. The second load gets connected and the voltage reduces. At t=3s, D-STATCOM is connected across the load and the voltage at the load side increases to the reference value. Thus the voltage at the load side is maintained constant irrespective of the load connected.

D-STATCOM consists of a universal bridge and a control circuit as seen from Figure 20. The bridge consists of a dc voltage source of 22kV. a capacitor of 750uF is connected in parallel. Six IGBTs are connected in form of a H-bridge and gate pulses are given in an order. The outputs are taken from middle part of the connections. These are connected to 1st load through a circuit breaker controlled by step control having step time t=3sec. Output voltage ($V_{m,rms}$) across one line is measured. The control circuit consists of transformation block that transforms the three phase abc to dqo components since the d and q components are interlinked so in order to control the three phase voltage d and q components are separated out as vd and vq. vd is the horizontal component of voltage and vq is the quadrature component of the voltage and both are in per unit quantity (pu) which is given by equations 10 and 11.

As seen from the controller part vd is made close to unity and vq component is made close to zero so as to maintain the power factor close to unity and this is done by applying error signal to the PI controller and the output of the PI controller is given to the PWM generator which gives pulses to the Voltage Source Converter to control the voltage at the load side. At t=3s D-STATCOM is connected across the load and the voltage at the load side increases to the reference value. Thus the voltage at the load side is maintained constant irrespective of the load connected.

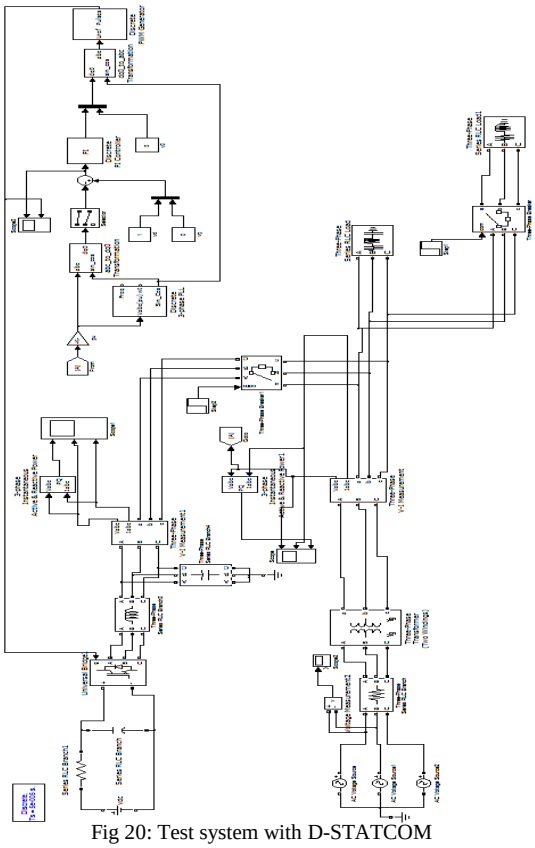

Fig 20: Test system with D-STATCOM

Alternate design for D-STATCOM is given by figure 21. In this output voltage generated is not seperated into dqo components, rather it is abc voltages are taken directly. Output voltage being an analog signal, is converted into digital signal using ADC . This signal is compared with a constant signal of 1V ,an error signal is generated which is given to PI controller. This signal is limited to $\pm 0.5V$ using a saturator. This signal generated is delta which is fed to pulse generator. The line voltages of loads are also fed to the pulse generator. This generated 6 pulses. The pulses are given directly to even numbered IGBTs (T_2, T_4, T_6). Logically complemented pulses are fed to the odd numbered IGBTs (T_1, T_3, T_5).

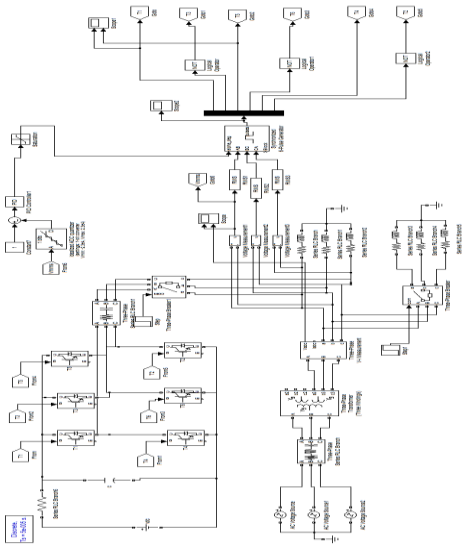

Fig 21: Alternate design of test system with D-STATCOM

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Limitations of design proposed

1. Load 1 constant

- For L=0.0059H
  R=0.2Ω, output= 400V
  R>0.2Ω, output< 400V
  R<0.2Ω, output>400V
- For R=0.2Ω
  L=0.0059H, output=400V
  L>0.0059H, output=400V till t=4sec, then lowers to small value
  L<0.0059H, output<<400V
- For R=0.05Ω
  L=0.0059H, output slightly greater than input, ripples at starting of output
  L>0.0059H, output=400V from t=2 to 4sec, then output reduces, ripples at t=2,t=4sec
  L<0.0059H, output drops to very small value at t=2sec and remains there

2. Load 2 constant

- For R=12.1Ω
  L=0.1926H, output=400V
  L>0.1926H, output=400V, ripples at t=4sec, ripples increases for increase in L
  L<0.1926H, output=400V, ripples at t=2and t=4sec
- For L=0.1926H
  R=12.1Ω, output=400V
  R>12.1Ω, output=400V, small transient at t=2sec
  R<12.1Ω, output=400V

System parameters

Sl. no.	System Parameters	Standards
1.	Source	Y-g, 3Ø, 230kV, 50Hz
2.	Inverter Parameters	IGBT based, 3 arm, 6 pulse, carrier frequency 475 Hz
3.	PI controller	KP=1.2, KI=1, sample time=50µF
4.	Transformer 1	Δ/Y/Y 230k/400/400V
5.	Transformer 2	Δ/Y-g 230k/400V
6.	Transformer 3	Δ/Y-g 230k/400V
7.	Load 1	R=12.1Ω, L=0.1926H
8.	Load 2	R=0.2Ω, L=0.0059H

VII. RESULT

Consider the test system without D-STATCOM, as shown in figure19. Original voltage is 400V from t=0 to t=1sec. At t=1sec, circuit breaker connecting to the second load is given a pulse signal, it gets closed. Due to the load added, voltage reduces to 330V for the values of R and L selected as shown in the figure 22. Upon adding the D-STATCOM at t=3sec, voltage restores back to 400V as shown in the figure 23.

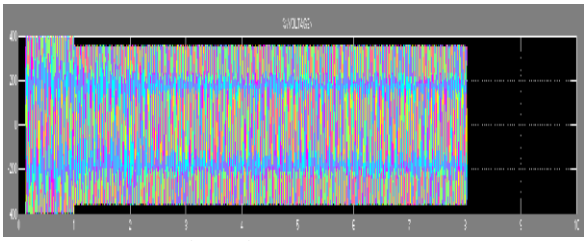

Fig 22: Waveform of test system without D-STATCOM

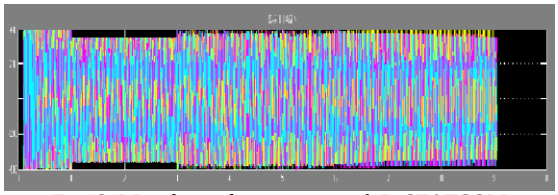

Fig 23: Waveform of test system with D-STATCOM

VIII. CONCLUSION

The D-STATCOM has demonstrated excellent performance for the particular values of R and L selected and it can be concluded that D-STATCOM effectively improves the voltage magnitude in distribution networks and has the limitations in the design as given above.

The work can be expanded in the following areas:

1. Making a comparison between the D-STATCOM based on two and multi-level IGBT voltage source converter.
2. Dynamic loads can be considered in future work and the effect of D-STATCOM with them can be studied.
3. Other advanced controllers like fuzzy controller, hysteresis current control, and adaptive fuzzy controller can be employed with D-STATCOM to increase the effectiveness of D-STATCOM in distribution network.

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