Novel Techniques For Circumventing The Glitch Effects On Digital Circuits For Low Power VLSI Design

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Abstract—*One of the requirements when using high-level power optimization techniques is the ability to estimate circuit power consumption quickly. Bit-level estimation techniques which take into account the glitch activity in a circuit take too long to provide power estimates. In this paper we present a novel method such that a new complementary metal-oxide semiconductor (CMOS) gate design that has different delays along various input to output paths within the gate. The delays are accomplished by inserting selectively sized "permanently on" series transistors at the inputs of a logic gate. The attempt is made demonstrate the use of the variable input delay CMOS gates for a totally glitch-free minimum dynamic power implementations of digital circuits. The key contributions presented by this work include a novel technique to model and elimination of glitch activity in digital circuits using different techniques and modified circuit for elimination of glitch is presented.*

Index Terms— CMOS gate design, Transistor Sizing, Glitch, power optimization.

I. INTRODUCTION

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. The power consumption of these circuits has two components. The *dynamic power* [1, 3] is consumed only when the circuit performs a function and signals change. *Leakage or static power* [2, 3] is consumed all the time, i.e., even when the circuit is idle. It is unnecessary and one would like to eliminate it. But there are practical difficulties. Because the advanced CMOS technologies have higher leakage, this component has received much attention. The ways to reduce leakage work at the transistor design and manufacturing process levels. On the other hand, it has been realized that the dynamic power cannot be eliminated completely because it is caused by the computing activity. It can, however, be reduced by circuit design techniques.

Dynamic power consumed in the normal operation of a circuit consists of the essential power and glitch power [3, 4]. Glitches are spurious transitions caused by the imbalances in arrival times of signals at the inputs of gates [3].

II. BACKGROUND

The research work so far is focused on modeling of glitch effects and circumventing those effects by different methodologies. Since, every signal transition consumes a finite amount of energy. For the correct functioning of a logic circuit, every signal net needs to transition at most one time in one clock cycle. But in reality, the gate outputs transition more than once and these unnecessary transitions are called *glitches*. These transitions consume energy and are quite unnecessary for the correct functioning of the circuit. Vishwani D. Agrawal, Tezaswi Raja and Michael Bushnell, [1, 2] has shown glitch power consumption can be as much as 40% or higher as compared to the overall power consumption and it is advantageous to eliminate glitches from circuits as power consumption is critical in today's chips. Vishwani D. Agrawal, Tezaswi Raja and Michael Bushnell [1] [3] demonstrated the use of the variable input delay CMOS gates for a totally glitch-free minimum dynamic power implementations of digital circuits.

Altaf Abdul Gaffar, Jonathan A. Clarke, George A. Constantinides,[5] noticeably explains that the use of glitch activity based power models to reduce the over 20 times underestimation of macro-models, by providing power estimates which within a mean relative error of 30% compared to low-level power estimation.

From the thesis report on "Power optimized multipliers" [9] multipliers use 30% to 75% of its power in this kind of spurious switching. This shows there is a lot of potential of reducing power consumption by reducing glitches.

The paper is organized as follows. In section III, briefs on Glitching Effect. Section IV, is on proposed glitch free circuits. Section V summarizes the experimental results obtained, while section VI presents the conclusions of the work.

III. THE GLITCHING EFFECT

The following discussion focuses on power dissipation in CMOS circuit and occurrence of glitch effect in the digital circuit.

There are many ways of combining transistors to perform the logic functions such as NOT, NAND, NOR, etc. We will describe the CMOS design style which is most prominent in current day technologies. A CMOS gate is constructed by a combination of MOSFETs to realize a logic function. But a MOSFET is not an ideal switch. When *open* it provides a large but finite resistance between its source and drain terminals. When *closed* it provides a small nonzero

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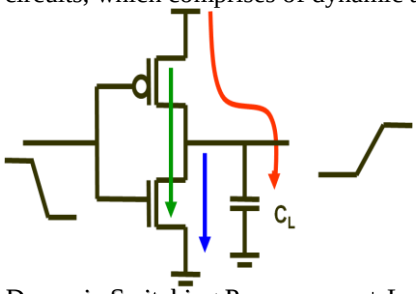
resistance. For a CMOS gate, the output signal change follows the input change with a certain delay. First, the closing and opening of MOSFETs in the gate depends upon the slope of input signals. Then, the output signal change requires charging or discharging of the output capacitance through a low resistance path provided by the "ON" MOSFETs. [2]

Fig. 1 indicates power dissipation in the CMOS circuits, which comprises of dynamic and leakage powers.



Dynamic Switching Power (red line) + Leakage Power (Blue line)

Fig 1 Power dissipation in CMOS circuit

So far we have looked at where the power is dissipated. As we have seen, switching activity dictates some of the power usage in CMOS. A problem arises when the inputs on an *element* or *gate* do not change at the same time. This might cause the element to use energy more than one times instead of once. This leads to the problem that some circuits switch more than they need to reach their final state. This effect is called glitching [2, 3].

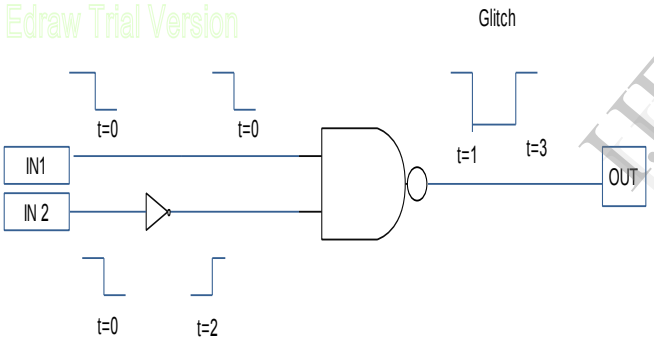


Fig. 2 Circuit showing the formation of glitches [1]

Consider a circuit as shown in fig 2.1, where the inverter has a delay of 2 units and the NAND gate has a 1 unit delay. Due to differential arrival times at the inputs of the NAND gate, the output produces a glitch consisting of two transitions.

A glitch may cause a high signal to become low or a low signal to become high. A positive glitch may occur on a logic low signal causing it to overshoot for a brief period. Similarly, a negative glitch may occur on a logic high signal causing it to undershoot for a brief period. Glitches, if untreated, may affect the operation of a circuit and hamper the performance of the entire system of which the circuit is a part. In digital systems, glitches may tamper with clock signals and handshake signals that drive various circuits within the system. For example, in a memory array if a glitch occurs in an address signal while it is being latched, then the wrong address may be read, which may lead to an unrecoverable system error. Also, glitches may cause chips to receive or transmit noisy signals to other chips.

Thus, an attempt is made in designing the circuits to anticipate and handle spurious pulses or glitches in order to maintain the consistency and reliability of electrical circuit operation. A glitch removal circuit tries to remove glitches and restore an input signal to its original shape. These are discussed in detail in result section.

IV. PROPOSED GLITCH FREE CIRCUITS.

Un-optimized Circuit.

Consider the simple example circuit of Fig. 2. Assume that the delays of all gates are the minimum allowed by the technology through sizing of transistors in gates appropriately. The circuit was simulated for rising signals at all three inputs using *Virtuoso* and spectre simulator from *Cadence*. The results are shown in figure 4 & 8, as expected, output has some glitches which are power consumable and depreciates the speed of the design. Hence, the endeavor is made in removing the occurrence glitch effectively by following different methods as discussed below.

(a) Glitch Delay and Glitch Blocking Circuit.

A glitch removal circuit for removing positive and negative glitches shown in figure 3 from an input signal, comprising: a delay circuit having first and second inverters connected in series, the first inverter receiving the input signal and the second inverter generating a first delayed input signal, and a third inverter having an input connected to the output of the second inverter, the third inverter generating a second delayed input signal.

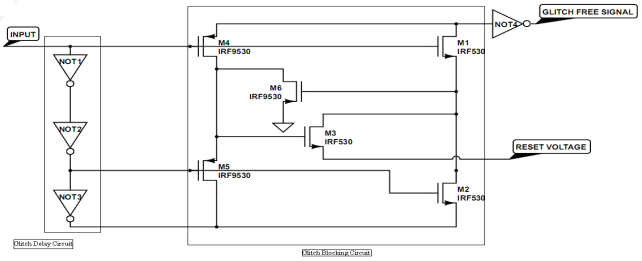


Fig. 3 Glitch Delay and Glitch Blocking Circuit [8]

In another embodiment, the present discussion provides a method for removing both positive and negative glitches from an input signal to generate a glitch free signal, using a glitch blocking circuit having first and second PMOS transistors and first and second NMOS transistors. The glitch removing method includes the steps of:

Step1. Delaying the input signal to generate a delayed input signal.

Step2. Applying the input signal to the gates of the first PMOS and first NMOS transistors.

Step3. Applying the delayed input signal to the gates of the second PMOS and second NMOS transistors.

Step4. If the input signal is glitch free, then inverting the output of the glitch blocking circuit and providing the inverted signal as the glitch free signal and storing the glitch free signal for later use.

Step5. If the input signal has a glitch, then switching off the glitch blocking circuit for duration of the glitch and providing the previously stored glitch free signal as an output.

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Though this technique eliminates the glitches efficiently but, the major overhead with this technique is glitch blocking circuit itself led to increase the delay there by decreases the switching speed of the digital circuits.

(b). Buffer Optimized Circuit.

The buffer optimization using conventional gates requires the use of one buffer for the circuit to operate at the same speed. The optimized circuit with the buffer is shown in Fig. 3. It is implemented using two CMOS inverters and has an overall delay of 2 delay units. The buffer optimized circuit was simulated for the same vector-pair as the un-optimized circuit. As expected, the optimization eliminated all glitches as shown in fig. 9. However, the buffer optimization requires that the transition of input 1 should pass through the buffer. This increases the total number of transitions in this circuit.

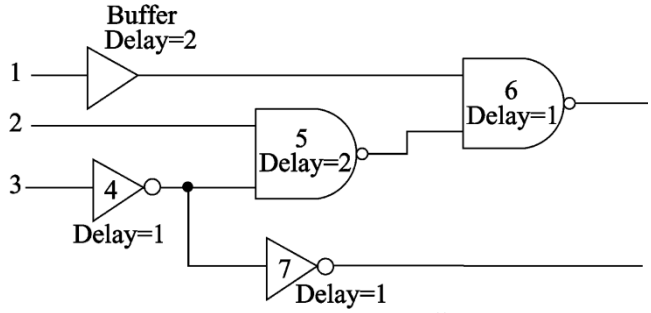

Fig. 3. Design with two-inverter delay buffer

(c) Low-Power Design with Proposed Gate.

When variable input-delay gates are used, the optimized circuit is shown in Fig. 7. We have used the single *n*MOS transistor implementation here but any of the proposed designs could have been used. The glitches at the outputs of gates 5 and 6 are eliminated in this optimized design as well.

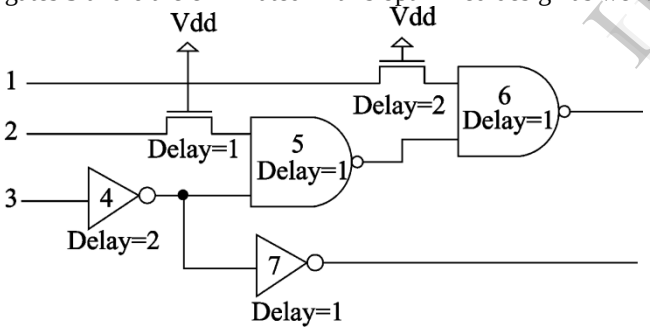

Fig. 4. Design with proposed input delays.

V. EXPERIMENTAL RESULTS

The work discussed till now is carried out on various tools such as Xilinx ISE, Modelsim and Cadence. The results on these tools are synthesizable. The Schematic is done on Virtuoso platform and simulated on spectre simulator; the layout work for schematics is carried out on Assura. However, figure 4 shows the simulation result of un-optimized circuit, result in occurrence of glitch, which is carried on Xilinx ISE tool. Figures 5, 6 & 7 show the schematic for three different techniques as discussed above and figures 8, 9 & 10 discuss about the simulation results respectively, these simulation results clearly shows that proposed gate design do away with the glitches effectively, thus leads to efficient low power and high speed VLSI design.

Figure 11 provides layout of proposed low-power gate design, 8216 $(\eta m)^2$ is its total area consumed. Watching out results of figure 12, the proposed design eradicated the episode of glitches and concluding to the development of low-power and high-speed VLSI design.

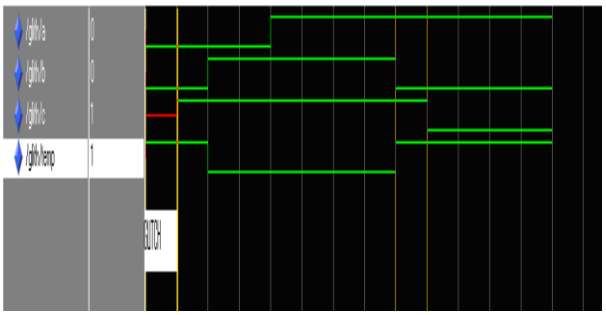

Fig. 4 Simulation result of fig 2.1

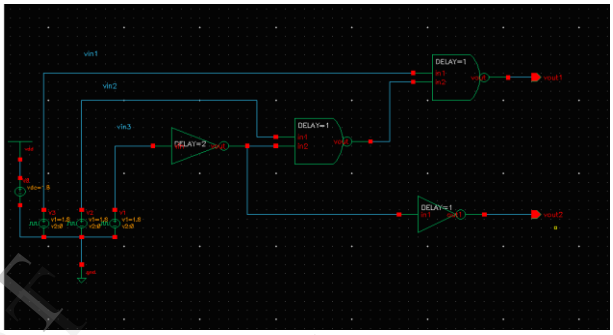

Fig. 5 Schematic of Unoptimized Circuit.

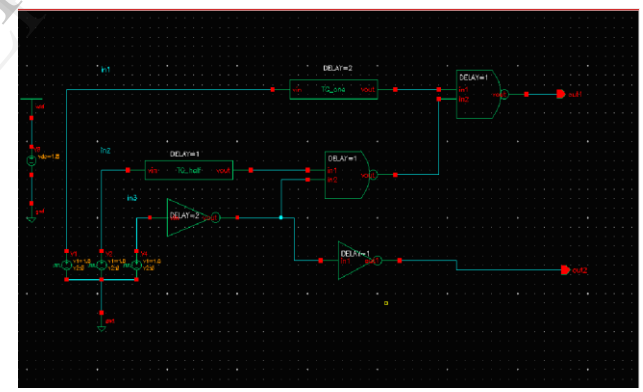

Fig. 6 Shematic of design with two-inverter delay buffer circuit.

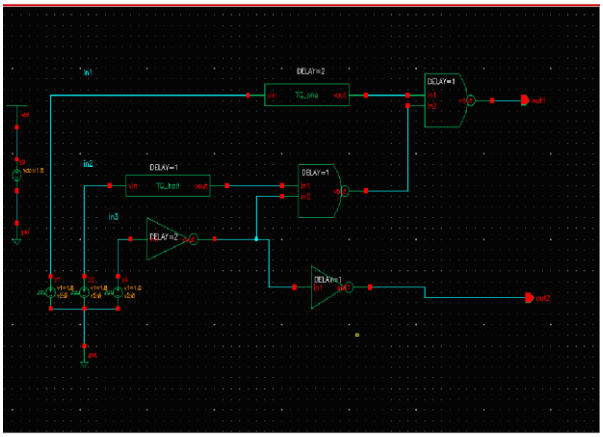

Fig. 7 Low power design with proposed gate.

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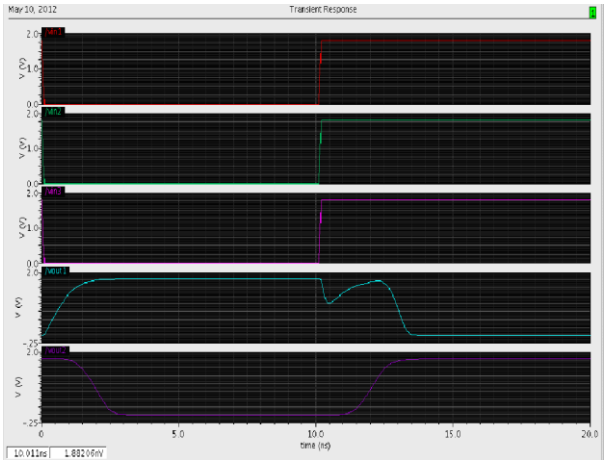

Fig. 8 Simulation result of fig 5.

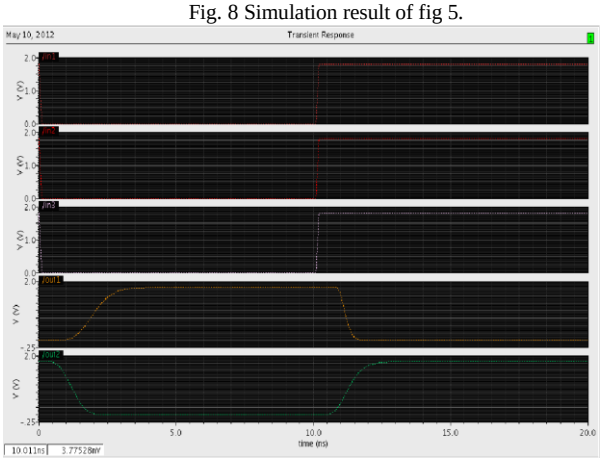

Fig. 9 Simulation result of fig. 6

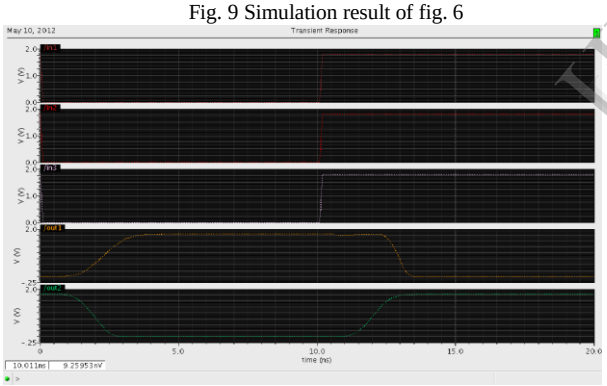

Fig. 10 Simulation result of fig. 7

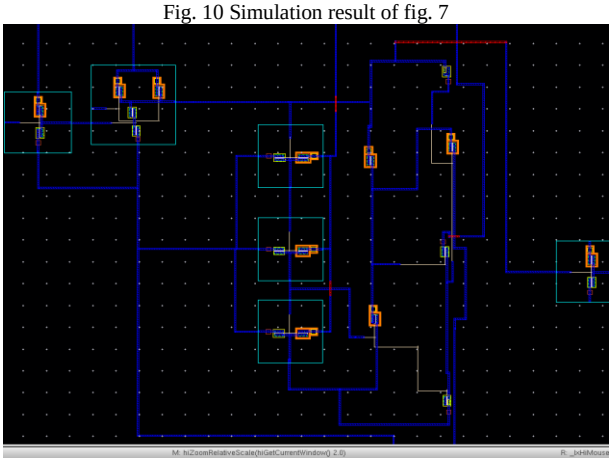

Fig 11. Layout of proposed gate design

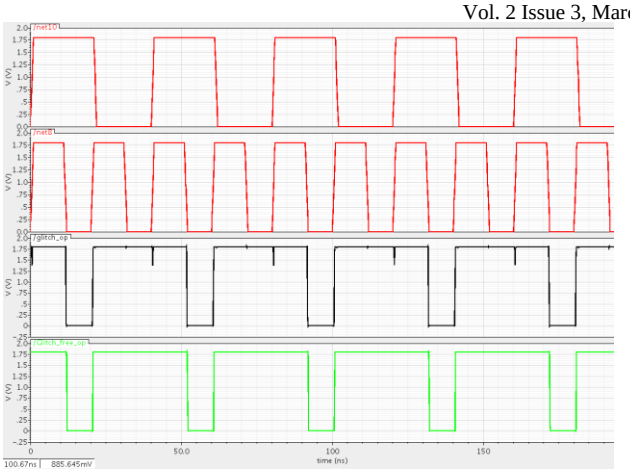

Fig.12 Glitch free output waveform for the proposed design.

Table I. Power Report

Technology: 180nm , Voltage=1.8V

Design Techniques	Power Consumed in (mW)
Un-optimized circuit	4.8
Buffer Optimized Circuit	3.9

Table II. Transistor Count and Logic activity

SIMULATION OF THE THREE DESIGNS OF THE EXAMPLE CIRCUIT FOR INPUT 000⟶111

Design Techniques	Transistor Count	Logic Activity	
		Gate Transitions	Reduction
Un-optimized circuit	12	8	0.0%
Buffer Optimized Circuit	16	5	37.5%
Proposed Design	14	3	62.5%

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VI. CONCLUSION

The procedure discussed here is independent of any operational conditions and hence the optimization is valid for all input vectors sequences. It is possible to reduce the hardware overhead of delay buffers by customizing the optimization to a subset of highly probable or worst-case vectors.

The notion behind this work is to eliminate glitches in the digital designs by adopting either one of the two techniques which we have discussed so far by allowing only essential computing activity to occur and hence obviously making an attempt to reduce total dynamic power dissipation by reducing number of transitions at output. Objective of the proposed design is to minimize total dynamic power dissipation by reducing total number of transition i.e. reducing the logic activity.

Table II briefs that logic activity in buffer optimized circuit is 5, which means that almost 37.5% of logical activity is reduced when compared to un-optimized circuit. Further taking in to consideration of proposed design, the beauty of reducing the logical activity is reduced to 62.5% and 40% as compared with un-optimized and Buffer Optimized Circuit respectively.

All of the above techniques clearly eliminates the glitch effects in the digital techniques, while proposed technique is more advantages, since logical activity in the proposed designed is reduced by 62.5% which in-turn decreases the switching activity.

A possible area for future investigation is the use of the CMOS transmission gate for realizing delays in 90, 65, 45 nm, and even finer CMOS technologies. Though intended to add resistance in the charging path, the transmission gate also adds capacitance causing extra power consumption.

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