Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 12, December-2020

Novel Technique of Nine Level Inverter for Harmonic Reduction with Reduced Switches

Sanamehreen Malik
Department of Electrical Engineering,
Parul University.
Vadodara, India.

***Abstract*— This paper introduces a unique design of Multi-level inverters (MLI) for harmonic reduction. The proposed technique is advantageous because it uses minimum number of power electronic switches as compared to the traditional MLI resulting in reduced Electromagnetic Interference (EMI), reduced switching loss and low Total Harmonic Distortion (THD). The 9 level output is obtained using unipolar sine wave linked with 9 level cascaded H bridge Multi-level inverter (CHBMLI) implementing concept of carrier in phase disposition Pulse width modulation technique. MATLAB/SIMULINK is used for the modeling and analyzing the system. Fast Fourier Transform (FFT) algorithm is used for analyzing the presence of Total Harmonic Distortion (THD) in the system.**

Keywords*— Multilevel Inverters (MLI), Electromagnetic Interference (EMI), Total Harmonic Distortion (THD), Cascaded H bridge Multilevel Inverter (CHBMLI), Fast Fourier Transform (FFT).

I. INTRODUCTION

Renewable energy sources are much in trend to abate environmental pollution and other ecological problems. Most of the renewable energy sources gives power in the form of direct current, thus power conversion plays a significant role in power system. Several topologies and control techniques are day by day researched and implemented to enhance the power derived from the renewable sources [1].

Commonly 2 level inverters are used in industry for low power applications. Multilevel inverters are specifically used for high power applications. The Multilevel inverter attracts attention because of the low switching losses, good power quality and high voltage capability [2]. The grid integration of conventional 2 level inverter injects high amount of harmonics. Multilevel inverters are capable of creating smoother stepped level output with more voltage levels together [3]. More the number of voltage level, smoother the waveform and it becomes near to sinusoidal wave [4].

Almost every power electronic device operates at high switching frequency. The switching process leads to conduction losses and switching losses. The handling of power of power electronic switches gives rise to conduction losses. Switching loss mainly occurs due to switching frequency, current of the power electronic switches and the voltage jump of each switching. The modulation techniques mainly used are unipolar modulation and bipolar modulation [5] [6].

The proposed model is designed for grid integration purpose. All the IEEE limits and allowable range of the harmonics is being focused on along with the minimum utilization of power electronic switches for the generation of required level output.

II. CLASSIFICATION OF MULTILEVEL INVERTER

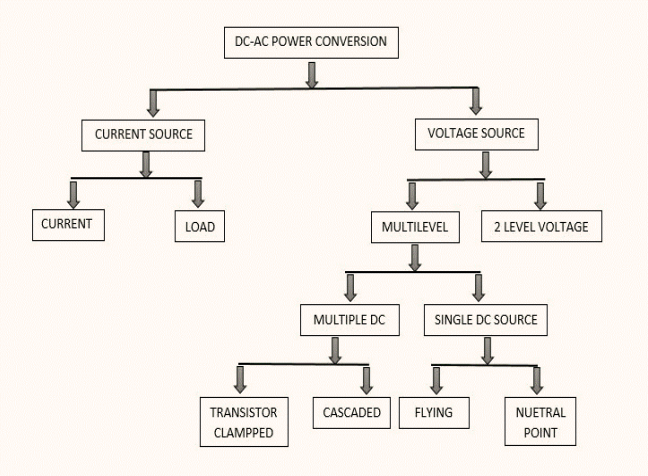

Fig: 1 Classification of MLI

The above Figure shows the classification of inverter into Cascaded H bridge multilevel inverter (CHBMLI), Flying Capacitor multilevel inverter (FCMLI), Diode clamped Inverter [7].

III. COMPARISON OF CONVENTIONAL INVERTER WITH MULTILEVEL INVERTERS.

TABLE 1 : COMPARISON OF CONVENTIONAL AND MULTILEVEL INVERTERS[8]

S. No.	Parameters	Conventional Inverter	Multilevel Inverter
1.	THD in output voltage	Higher	Lower
2.	Voltage regulation	Not adjustable	Adjustable
3.	Switching frequency	Higher	Lower
4.	Switching losses	High	Less
5.	Efficiency	Low	High
6.	Applications	Low voltages	Higher Voltages
7.	Control Scheme	Simple	Complex

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 12, December-2020

TABLE 2: PARAMERTER COMPARISON OF DIFFERENT LEVEL OF INVERTERS[9],[10],[11]

S. No.	Parameters	5-Level	7-Level	9-Level
1.	Power Electronic Switches	6	7	9
2.	Capacitors	2	3	4
3.	Voltage THD (%)	4.73%	3.63%	2.48%
4.	Current THD (%)	2.53%	2.35%	2.15%

The above table gives us the brief idea of the THD percent present in the system with different numbers of the levels. From the analysis we found that as we increase number of levels, total harmonic distortion gets reduced. Considering the complexity, cost and THD the system is modelled for generating 9 level output.

IV. PULSE WIDTH MODULATION TECHNIQUES [12]

Pulse Width Modulation Techniques are classified into two categories i.e.

- Phase Shifted PWM (PS PWM)
- Level-shifted PWM (LS PWM)

A. Phase Shifted PWM (PS PWM):

Phase Shifted PWM applies several triangular carriers that have the same frequency and same peak to peak amplitude, but there is a phase shift between any two adjacent carrier waves. "For n voltage levels, (n-1) carrier signals are required, and they are phase shifted with an angle of $\theta = (360°/n-1)$". The gate signals are generated with a proper comparison of carriers and a modulating signal.

B. Level-shifted PWM (LS PWM):

"Level Shifted PWM also uses some carrier signals, but they are arranged in different levels among the carriers". According to the disposition of carrier waves, the LS PWM can be listed into three main type i.e.

a) Phase disposition (PD), when all the carrier signals are in phase,
b) Phase opposition disposition (POD), when all the carrier signals above zero reference are in phase but in opposition with those are below zero references.
c) Alternate phase opposition disposition (APOD): when the modulating signal of each phase is in opposition from each other.[12],[13]

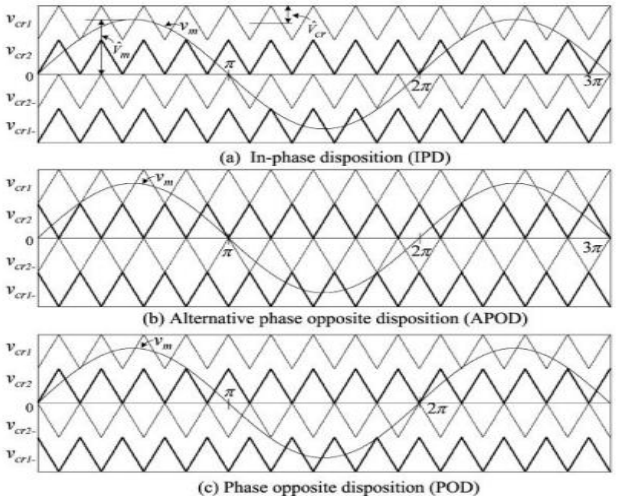

Fig 2: Level Shifted PWM Techniques [14]

TABLE 3: THD COMPARISONS OF PWM TECHNIQUE [15],[16]

S. No.	PWM techniques	No. of level	THD%
1.	Phase Disposition	3	52.06%
2.	Phase Opposition Disposition	3	54.17%
3.	Alternate Phase opposition Disposition	3	54.17%
4.	Phase Disposition	5	26.69%
5.	Phase Opposition Disposition	5	26.96%
6.	Alternate Phase opposition Disposition	5	37.13%
7.	Phase Disposition	7	18.05%
8.	Phase Opposition Disposition	7	22.48%
9.	Alternate Phase opposition Disposition	7	25.20%
10.	Phase Disposition	9	16.77%
11.	Phase Opposition Disposition	9	17.08%
12.	Alternate Phase opposition Disposition	9	17.10%
13.	Phase Disposition	11	12.48%
14.	Phase Opposition Disposition	11	13.24%
15.	Alternate Phase opposition Disposition	11	13.30%
16.	Phase Disposition	13	10.68%
17.	Phase Opposition Disposition	13	12.54%
18.	Alternate Phase opposition Disposition	13	12.57%

The table 3 gives us the brief idea about the PWM techniques used for particular level of inverter and the amount of THD in percentage for each of them.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 12, December-2020

V. PROPOSED NINE LEVEL INVERTER.

A. Circuit Configuration and working principle.

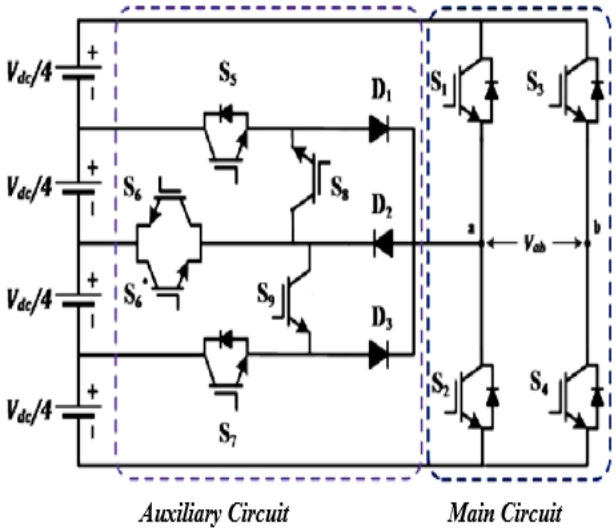

Fig. 3 Circuit Diagram of Nine level inverter.

The Fig. 3 is of the proposed technique of nine level Inverter with reduced number of switches. The inverter designed is economical without affecting the inverter operation. The inverter is mainly dived into two parts; main circuit and the auxiliary circuit. The purpose of the main circuit is to control the output and the voltage polarity. The main circuit is a normal H- bridge configuration inverter. The switches that forms the main circuit are S_1, S_2, S_3 and S_4. These switches are power metal oxide semiconductor field effect transistor (MOSFET) with reverse diode. The auxiliary circuit is formed by switches S_5, S_6, S_{6*}, S_7, S_8, S_9 and the Diodes D_1, D_2, D_3. The switches S_5 and S_7 are power MOSFET with reverse diode .The switches S_8 and S_9 are power MOSFET without body diodes. While S_6 and S_{6*} are bidirectional. The source is divided into four part each having voltage of $V_{dc}/4$.

B. Switching Sequence.

TABLE 4: SWITCHING SEQUENCE OF NINE LEVEL INVERTER

State		V_{ab}	I_{out}	Current Path
i.	Zero	0	+	(S_1& D_{S3}) or (S_2& D_{S4})
ii.	Zero	0	-	(S_3& D_{S1}) or (S_4& D_{S2})
iii.	Active	$V_{dc}/2$	+	S_7, D_3& S_4
iv.	Active	$V_{dc}/2$	-	D_{S7}, D_2, S_9& D_{S4}
v.	Active	$V_{dc}/4$	+	S_6, S_8, D_1& S_4
vi.	Active	$V_{dc}/4$	-	S_6^* , D_2& D_{S4}
vii.	Active	$3V_{dc}/4$	+	S_5, D_1& S_4
viii.	Active	$3V_{dc}/4$	-	S_7S_7, D_3& S_4
ix.	Active	V_{dc}	+	S_1, S_4
x.	Active	V_{dc}	-	D_{S1}& D_{S4}
xi.	Active	$-V_{dc}/2$	-	D_{S5} , S_8 , D_2& S_3
xii.	Active	$-V_{dc}/2$	+	S_5 , D_1& D_{S3}
xiii.	Active	$-V_{dc}/4$	-	S_3, D_2& S_6^*
xiv.	Active	$-V_{dc}/4$	+	S_6, S_8, D_1& D_{S3}
xv.	Active	$-3V_{dc}/4$	-	S_3, D_2, S_9& D_{S7}
xvi.	Active	$-3V_{dc}/4$	+	S_7 , D_3& D_{S3}
xvii.	Active	$-V_{dc}$	-	S_3, S_2
xviii.	Active	$-V_{dc}$	+	D_{S3}& D_{S2}

C. Simulation of Proposed Model

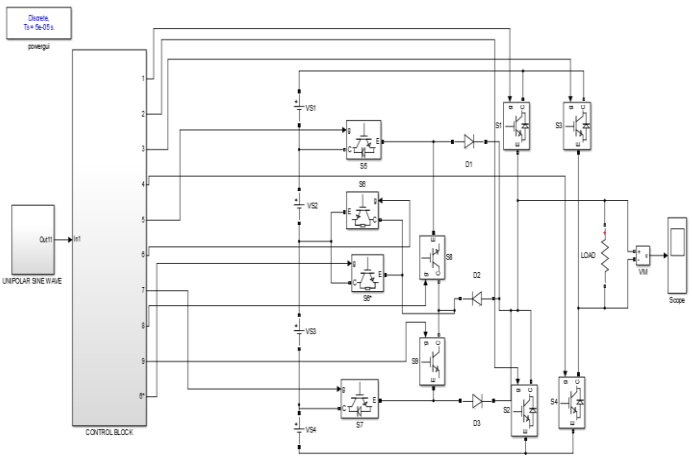

Fig. 4 MATLAB simulation for 9 level inverter

To get the desired output a single phase rectifier is used for creating the unipolar sine wave. The unipolar sine wave will generate the four main comparison wave namely A, B, C and D. This comparison wave will compare our output from each switching pattern thus resulting in the required pattern for the output generation. The simulation is being carried out using MATLAB software having version 2013a. The rating used in the simulation for generation of unipolar sine wave are, AC supply having normal rating i.e.230 Volts 50 Hz, Transformer of rating 100VA, 230/24V, Diodes connected to the resistance of 1 ohm. The comparison is being made using the logical comparators and then is being fed to the switches $S_1 - S_9$.

D. Switching pattern and Control Stratergy

The logical operators used for comparison and the comparison wave along with unipolar wave generation are in the control block as described in Fig. 4. Keeping in mind the switching sequence and the output the switching pattern is decided as described in Table 4.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 12, December-2020

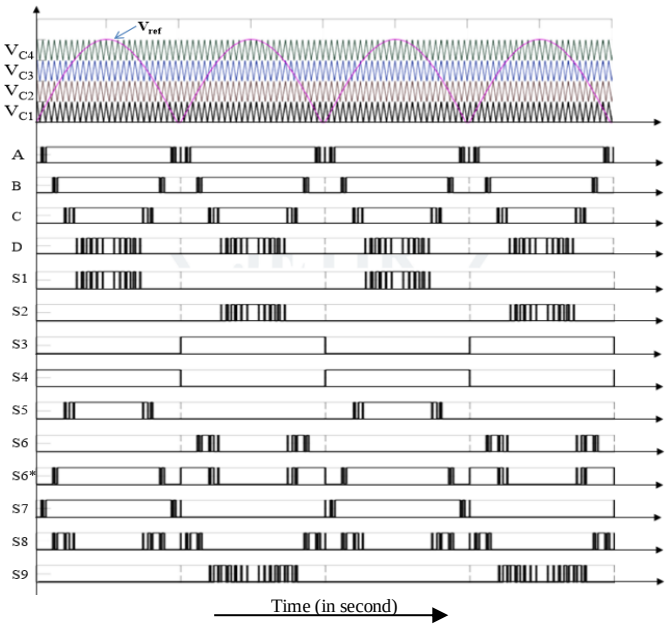

Fig. 5 Switching Pulse for 9-Level inverter

VI. SIMULATION RESULT

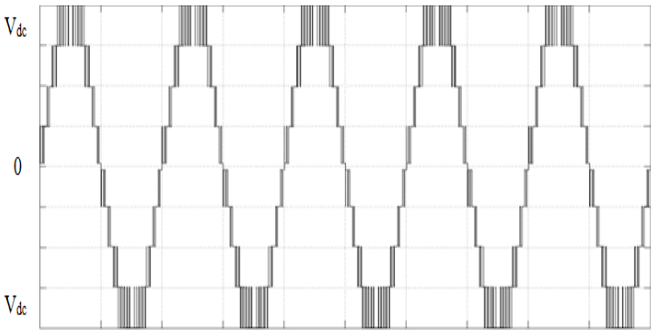

Fig. 6 Output Voltage Waveform of 9-Level Inverter

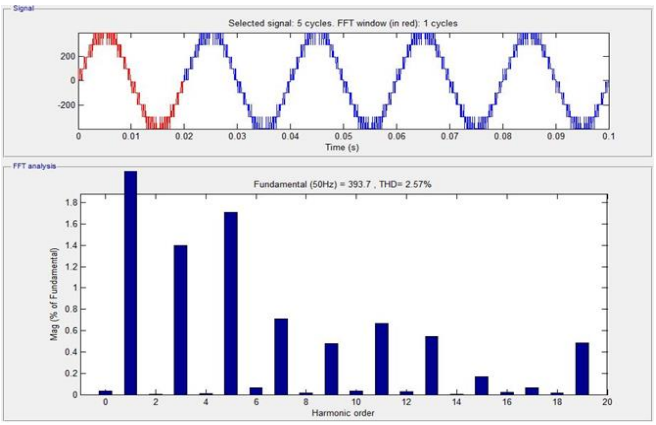

Fig. 7 FFT analysis for THD in output voltage

VII. CONCLUSION

The proposed new topology of the single phase Nine level inverter is suitable for the grid integration. The amount of harmonics present in the system are within the IEEE-519 standard. The Phase disposition Pulse width modulation technique used for lowering the harmonic content in the proposed system. The harmonic content present in the system is only 2.57% giving us the nine level output. The main advantage of this proposed inverter is it is economical, less number of switches resulting into the less amount of switching losses and High power density.

ACKNOWLEDGEMENTS

Author would like to express their gratitude to the Royal Academy of Engineering (RAE), Parul University (PU), Larsen & Toubro (L&T) and University of Surrey. This research paper is out of research work carried out as part of Industry Defined Research Project entitled 'Green Refrigeration Systems Using Solar Energy' funded by Royal Academy of Engineering, UK under Newton Bhabha Fund under the Higher Education Partnership – India Program.

REFERENCES

[1] Jagabar Sathik Mohd.Ali*, Vijayakumar Krishnaswamy, " An assesment of recent multilevel inverter topologies with reduced power electronic component for renewable application." Renwable and sustainable energy reviews (2017).

[2] P. Palanivel S.S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques." The Institution of Engineering and Technology 2011- Power Electron., 2011, Vol. 4, Iss. 8.

[3] Vivekkumar.A.Patel, Prakash.K. Jariwala, Divyakant.V.Parmar, Pratik.B.Patel, Priyank.D.Patel, "A Simplified Topology for Nine level Modified Cascaded H-bridge Multilevel Inverter with Reduced Number of Switch & Low THD", International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056 Volume: 04 Issue: 04 | Apr -2017

[4] Smt N. Sumathi 1, R. Tulasi Ram2, "A Multilevel Inverter Topology For Renewable Power Generation," International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056 Volume: 02 Issue: 06 | Sep-2015

[5] U. S. Selamogullari, D. A. Torrey, and S. Salon, "A systems approach for a stand-alone residential fuel cell power inverter design," IEEE Trans. Energy Convers., vol. 25, no. 3, pp. 741–749, Sep. 2010.

[6] C. Y. Chen, Y. H of DSP-based voltage-frequency conversion system," in Proc. Int. Symp. Comput. Commun. Control Autom., May 2010. Lin, J. F. Chen, and R. L. Lin, "Design and implementation

[7] SourabhRathore, Mukesh Kumar Kirar, and S. K Bhardwaj, "Simulation Of Cascaded H- Bridge Multilevel Inverter Using Pd, Pod, Apod Techniques," Electrical & Computer Engineering: An International Journal (ECIJ) Volume 4, Number 3, September 2015.

[8] AnjaliSudarsanan, Roopa R, Sanjana S, "Comparison of Conventional & New Multilevel Inverter Topology," International Journal of Scientific & Engineering Research, Volume 6, Issue 2, February-2015 330 ISSN 2229-5518 IJSER © 2015

[9] Muhammad Arif, Madiha sultan, Jawadsaleem, Abdul Majid, "THD of analysis reduced switch 5-level inverter using multicarrier PWM schemes" International conference on innovative trends in computer engineering,2016.

[10] Cathrine E. S. Feloups, Ahmed I. M. Ali, Essam E. M. Mohamed, "Single-Phase 7-Level PWM Inverter for PV Systems Employing Multi-level Boost converter" International conference on innovative trends in computer engineering,2018

[11] M. Saad bin Arif, Shahrine Md. Ayob, Atif Iqbal, Sheldon Williamson, Zainal Salam," Nine-level Asymmetrical Single Phase Multilevel Inverter Topology with Low switching frequency and Reduce device counts" IEEE,2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 12, December-2020

[12] Bin Wu, "High-Power Converters And Ac Drives," Canada, John Wiley, 2006

[13] I B F Citarsa, I N W Satiawan, I K Wiryajati, and Supriono, " Performance analysis of cascaded h-bridge multilevel inverter using mixed switching frequency with various dc-link voltages," IOP Conf. Series: Materials Science and Engineering 105 (2016)

[14] TanujDabas1, Ram Avtar, "THD Analysis of Cascaded H-Bridge With Level Shifted Multicarrier Modulation," Advances in Computer Science and Information Technology (ACSIT) Print ISSN: 2393-9907; Online ISSN: 2393-9915; Volume 2, Number 7; April – June 2015

[15] SourabhRathore, Mukesh Kumar Kirar, and S. K Bhardwaj, "Simulation Of Cascaded H- Bridge Multilevel Inverter Using Pd, Pod, Apod Techniques," Electrical & Computer Engineering: An International Journal (ECIJ) Volume 4, Number 3, September 2015.

[16] B.Harish[1], U.Raja Kiran[1], B.Madan lal[1], Soubhagya Kumar Dash[2] , "Power Quality Improvement of DC-AC Converter by Using Cascaded H-Bridge Multilevel Inverter", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization) Vol. 3, Issue 2, February 2014.