Novel Low-Power, Energy-Efficient Full Adder for Ultra Deep-Submicron Technology

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***Abstract* - Power consumption has emerged as a primary design constraint for integrated circuits (ICs).Full adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU, and the power consumption of an ALU can be lowered by lowering the power consumption of full adder. So the full adder designs with low power characteristics are becoming more popular these days. This paper presents a novel low power, energy efficient full adder circuit implementation for ultra deep sub-micron design. With rapid technology scaling, the main focus in low power design is targeted to reduce the static power while trading other vital requirements such as driving capability, delay, total power and noise immunity. Based on the fact that transmission logic has good driving capability and full signal swing than pass transistor logic, a new full adder cell is proposed to reduce delay and power-delay product (PDP).The simulations have been carried out with TANNER EDA simulation tool using PTM 65nm technology files. Simulations have been carried out for different supply voltages and loading conditions to compare the performance of the proposed circuit with respect to the existing ones.**

1. INTRODUCTION

The demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power is one of the premium resources a designer tries to save when designing a system. Full adders are fundamental units in various circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators, parity checkers, and so on [1]. Full adders are often used in the critical paths of complex arithmetic circuits for multiplication and division. These in turn form the core of any system and thereby influence the overall performance of the entire system. Enhancing the performance of the full adder can significantly affect the system performance. Figure 1 shows the power consumption breakdown in a modern day high-performance microprocessor [2].

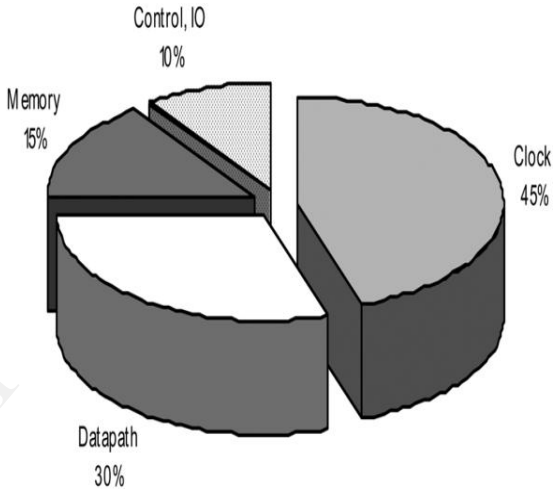

Figure 1

The datapath consumes roughly 30% of the total power of the system. Adders are an extensively used component in datapaths and, therefore, careful design and analysis is required for these units to obtain optimum performance. At the circuit level, an optimized design is desired to avoid any degradation in the output voltage, consume less power, have less delay in critical path, and be reliable even at low supply voltage as we scale towards deep sub micrometer. Good driving capability under different load conditions and balanced output to avoid glitches is also an important virtue.

Several logic styles have been proposed in the literature [1-8] to design 1-bit full adder cell. Each design has its own merits and demerits in terms of output signal swings, driving capabilities, speed, power, switching activity, noise immunity and so on. Generally, the focus in deep submicron technology is to reduce the static power by replacing nMOS with pMOS transistors [8] or by stacking effect or by reducing the transistor count [7]. In designing so, the designers often trade for other vital requirements such as area, driving capability, delay, total power and noise immunity. The performance of such a full adder cell as a single unit is good but when these cells are used as a building block of complex circuits, the performance degrades drastically.

In this paper, we presented an optimized design for a full adder cell craved for low power, low energy, reliable

operation at low supply voltage, avoiding degradation in the output voltage, good driving capability under different loading conditions. The rest of the paper is organized as follows. In section 2, general overview of full adder with its sub modules is presented. In section 3, the circuit for module II is proposed and combination of module II and III is presented. Using the proposed combination in Section 3, we build a new full adder cell in Section 4. Simulation results are presented in Section 5. Section 6 concludes the paper.

2. FULL ADDER COMPONENTS

A full adder can be broken down into three modules by extracting the logical expression for the outputs SUM and Cout using the binary inputs A, B and Cin [3-7]. Module I essentially perform the XOR(H) and XNOR(~H) functions in terms of the inputs A and B. In [6], the circuit for module I uses ten transistors and performs well at low supply voltages. We consider this circuit for module I in our design. Module II and III generates SUM, Cout respectively using three signals Cin, H and ~H as inputs.

3. PROPOSED CIRCUIT FOR MODULE II

The expression for output of module II can be expressed as SUM = Cin·H+ ~Cin · ~H. The proposed circuit for module II is shown in Figure 2(a). A transmission gate followed by a static inverter at the output is used to implement Cin·H. A transmission gate preceded and succeeded by static inverter implements ~Cin· ~H. Only one among the two transmission gates is ON and the other is OFF at any time. The inverter (enclosed in circle in Figure 2) can be shared between proposed module II and module III in [6], as shown in Figure 2(b).

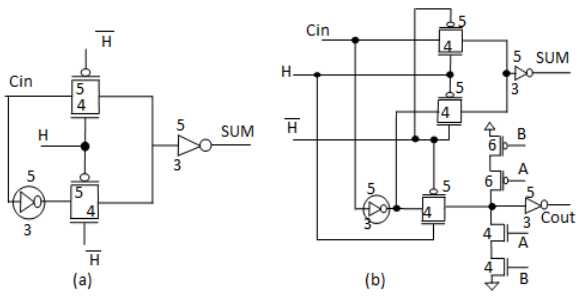

Figure 2: (a) Proposed module II, (b) Combination of module II and III with shared inverter

4. PROPOSED FULL ADDER CELL

In this section, we will present the new full adder design based on the circuits discussed in Section 2 and 3.

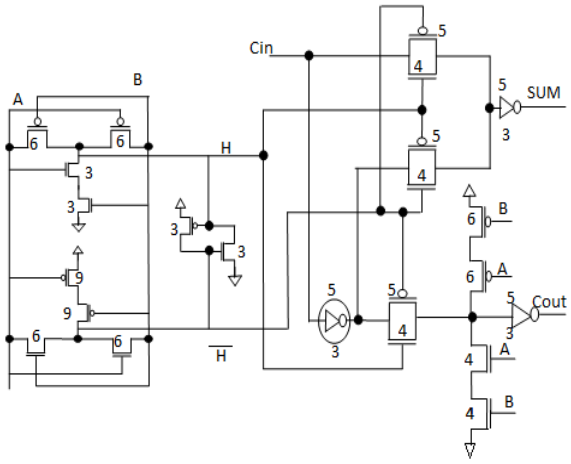

Figure 3: Proposed Full adder

In our proposed circuit, a single static inverter is shared to drive the transmission gates of both the modules II and III. At any point of time, only one among the two transmission gates driven by the inverter common to modules II and III are ON and the other is OFF. The compliment of Cin is propagated in module III when H is at logic '1' and ~H is at logic '0'. In the other case, when H is at logic '0' and ~H is at logic '1', the compliment of Cin is propagated in module II. The additional inverter for module II reduces the loading effect on H and ~H signals and speeds up the circuit in module II to generate the SUM output.

5. SIMULATION RESULTS

All the circuits are simulated in TANNER EDA using PTM [9] 65nm technology model files. The simulation test bench along with transistor sizes of each buffer is shown in Figure 4. The performance of the circuit is evaluated in terms of the worst-case delay, power consumption and PDP for supply voltages 1.1V and 0.9V at 250 MHz frequency. A change in the input may or may not lead to change at the output. As a result, some internal node may be switching even if there is no switching at the output, this leads to some power consumption. All the possible input combinations are taken into account for an accurate result.

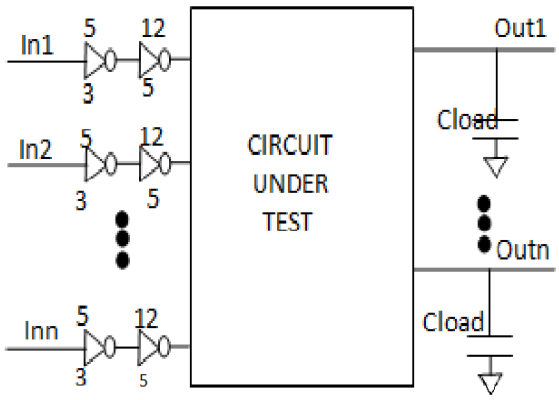

Figure 4: Simulation test bench

Table 1: Comparison of Full adders for different supply voltages

C_L=1.5fF Freq=25Hz	Adder in[5]		Adder in [6]		Proposed Adder	
	1.1V	0.9V	1.1V	0.9V	1.1V	0.9V
Power(µw)	4.30	2.72	5.081	3.1073	3.961	2.149
Delay(pS)	303.1	567.37	420.19	1254.8	230.1	280.3
PDP(aJ)	1304	1543.5	2135	3899	911	602

Table 1 shows the comparison of full adders at different supply voltages. The proposed full adder showed a good improvement in terms of power and delay when compared to adder in [5] and [6] at the cost of increase in static power.

Table 2: Comparison of Full adders for different values of C_L

V_{dd}=1.1V F=250MHz	Adder in [5]		Adder in [6]		Proposed Adder	
	2.5fF	3.5fF	2.5fF	3.5fF	2.5fF	3.5fF
Power(µW)	4.674	5.044	5.479	5.8587	4.139	4.312
Delay(pS)	320.2	336.5	438.6	453.48	240.4	260.7
PDP(aJ)	1496	1697	2403	2657	995	1124

We embedded our full adder cell in carry ripple(RCA) 4-bit full adder circuit to evaluate it in a realistic operating condition. The 4-bit full adder test circuit is shown in Figure 5 and the results are presented in figure 6.

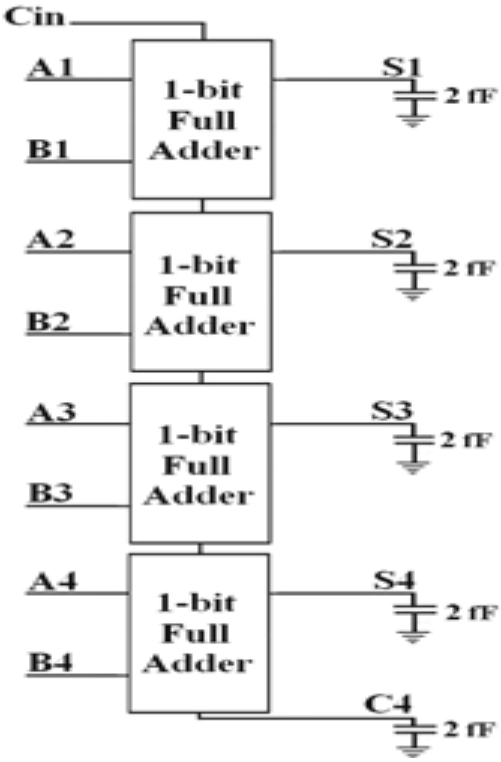

Figure 5

The observations for PDP from figure 6 show 20% improvement when compared to its best counterparts.

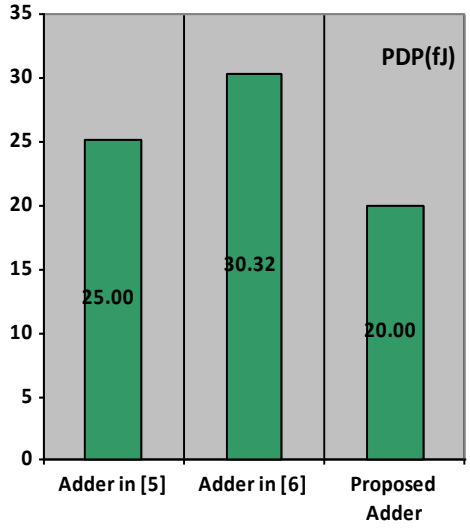

Figure 6: PDP results in 4 bit RCA for V_{dd}=1.1V, C_L=2 fF and Frequency = 50MHz

6. CONCLUSION

The simulation results show that the full adder is suitable for applications in ultra deep-submicron technologies. It provides better delay and energy characteristics and performs well at different supply voltages and loading conditions, making it suitable building block for complex circuits to be

used in dynamic voltage and frequency scaling (DVFS) scenario.

7. REFERENCES

[1] H.T.Bui, Y.Wang, and Y. Jiang, "Design and analysis of low power 10-transistor full adders using XOR–XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol. 49, no. 1, pp. 25–30, Jan.2002

[2] V. Tiwari, D. Singh, S. Rajgopal, G. Mehta, R. Patel, and F.Baez,"Reducing power in high-performance microprocessors," in Proc. Conf. Des. Autom. 1998, pp. 732-737

[3] Shams,A.M,.; Darwish, T.K.;Bayoumi, M.A.;, "Performance analysis of low-power 1-bit CMOS full adder cells," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.10, no.1, pp.20-29, Feb 2002

[4] Radhakrishna, D.; "Low-voltage low-power CMOS full adder," Circuits, Devices and Systems, IEE Proceedings - , vol.148, no.1, pp.19-24, Feb 2001.

[5] Chip-Hong Chang; Jiangmin Gu; Mingyan Zhang; , "A review of 0.18µm adder performance for tree structured arithmetic circuits" Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.13no.6, pp. 686- 695, June 2005.

[6] Goel, S.; Kumar, A.; Bayoumi, M. A.; , "Design of Robust, Energy-Efficient Full Adders for Deep-Sub micrometer Design Using Hybrid-CMOS Logic Style," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.14, no.12, pp.1309-1321, Dec. 2006

[7] Fayed, A.A.; Bayoumi, M.A.;, "A low power 10-transistor full adder cell for embedded architectures," Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on, vol.4, no., pp.226-229 vol. 4, 6-9 May 2001.

[8] Weiqiang Zhang; Linfeng Li; Jianping Hu; , "Design techniques of P Type CMOS circuits for gate-leakage reduction in deep sub-micron ICs," Circuit and Systems, 2009.MWSCA'09.52nd IEEE International Midwest Symposium on, vol., no., pp.551-554, 2-5 Aug.2009.

[9] Predictive technology model currently available online at www.eas.asu.edu/~ptm.