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New Multi Level Inverter with LSPWM Technique

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Abstract

As the most important part in multilevel inverters are switches which define the reliability, circuit size, cost, installation area and control complexity. This paper presents the nine level cascaded H-bridge multilevel inverter based on a multilevel DC link (MLDCL) An MLDCI can be a diode-clamped phase leg, a flying-capacitor phase leg, or cascaded half-bridge cells with each cell having its own DC source. Compared to diode clamped & flying capacitor type MLDCI inverters cascaded H-bridge multilevel inverter requires least no of components to achieve same no of voltage levels. Optimized circuit layout is possible because each level has same structure and there are no extra clamping diodes or capacitors. The MLDCL provides a DC voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave to the bridge inverter, which in turn alternates the polarity to produce an AC voltage. Compared with the existing type of cascaded H-bridge multilevel inverter, the MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels, the required number of active switches is 2 (m-1) for the existing multilevel inverters, but it is m+3 for the MLDCL inverters. LSPWM technique has been used to improve the MLDCLI performance. Simulation results are presented to verify the performance of the cascaded H-bridge MLDCL inverter supplying R & RL load.

***Keywords*- Cascaded H-Bridge, Level shift PWM, Total Harmonic Distortion**

I. INTRODUCTION

Multilevel inverters have received increasing interest for power conversion in high-power applications due to their lower harmonics, higher efficiency and lower voltage stress compared to two-level inverters[1]. Various topologies for multilevel inverters have been introduced and widely studied [2]. The most considerable of these topologies are the diode clamped [neutral-point clamped (NPC)] inverter [7], the capacitor clamped (flying capacitor) inverter [8] and the cascaded H-bridge inverter with separated dc sources . Multilevel inverters generate a staircase waveform. By increasing the number of output levels, the output voltages have more steps and harmonic content on the output voltage and the THD values are reduced. Therefore, they produce high quality output voltage by increasing the level number.

Multilevel inverters have very important development for high power medium voltage AC drives.

Usually, GTO-based two-level inverters were the choice for medium- or high-voltage level applications such as motor drives and static var compensation. Multilevel inverters using IGBTs are proposed for replacing the GTO-based two-level inverters in medium-voltage applications. Because IGBTs can switch faster and have less-demanding gate drive requirements than GTOs, IGBT-based multilevel inverters can significantly reduce the size and weight of passive filter components and offer better voltage waveforms. As the number of voltage levels, m, grows, the number of active switches increases according to $2\times(m-1)$ for the cascaded H-bridge, diode-clamped and flying capacitor multilevel inverters [1][6][5][7].

This paper presents a new class of multilevel inverters based on a multilevel dc link (MLDCL). An MLDCL can be a diode-clamped phase leg or a flying capacitor phase leg; or it can be constructed by connecting in series a number of half-bridge cells, each having its own dc source. A multilevel voltage source inverter can be formed by connecting an MLDCL with a single-phase bridge inverter. The MLDCL provides a dc voltage with the shape of a staircase, with or without pulse width modulation (PWM), to the bridge inverter, which in turn alternates the polarity to produce an ac voltage. Compared with the existing multilevel inverters, the new MLDCL inverters can significantly reduce the switch count as the number of voltage levels increases beyond five. For a given number of voltage levels, m, the new inverters requires m+3 active switches.

Table I: Comparison of MLI Topologies

Converter type	**Diode clamped**	**Flying capacitor**	**Cascaded inverter**	**MLDC inverter**
Main switching device	(m-1)*2	(m-1)*2	(m-1)*2	M+3
Main diode	(m-1)*2	(m-1)*2	(m-1)*2	(m+3
Clamping diodes	(m-1)*(m-2)	0	0	0
Dc bus capacitors	m-1	m-1	(m-1)/2	(m-1)/2
Balancing capacitors	0	(m-1)*(m-2)/2	0	0

By using PWM techniques the inverter's fundamental voltage can be controlled and the harmonics can be attenuated. In this method a carrier signal at the desired switching frequency (□□□) is generated and compared with the command or modulating voltage signal (□□) and gate signals for the switching devices are generated by comparing the modulating signal with the carrier signal. When the magnitude of the modulating signal is above the carrier, the upper switch is ON and when below, the lower switch is ON [4]

II. CASCADED H-BRIDGE MLDCL INVERTER TOPOLOGY

Cascaded H-Bridge inverter (CHI) has more advantage than other topologies in view of cost and efficiency, this CHI can be used with MLDCL to reduce the layout of the circuit. Figure.1 shows a block diagram of the presented cascaded H-bridge MLDCL inverter topology, which consists of a multilevel DC source to produce DC-link bus voltage V_{bus} and a single-phase full-bridge (SPFB) inverter consists of four switches S1-S4 to alternate polarity of DC-link bus voltage to produce an AC voltage. The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches S_{ak} and S_{bk}. The two switches and operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the dclink voltage by reversing the switches..[1]

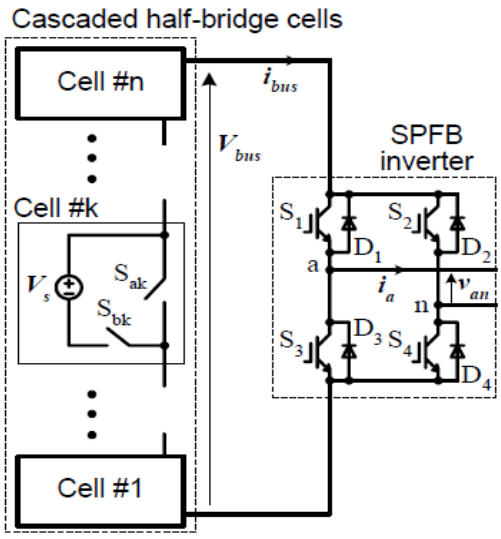

Figure 1 Block diagram of Cascaded H-bridge MLDCL inverter

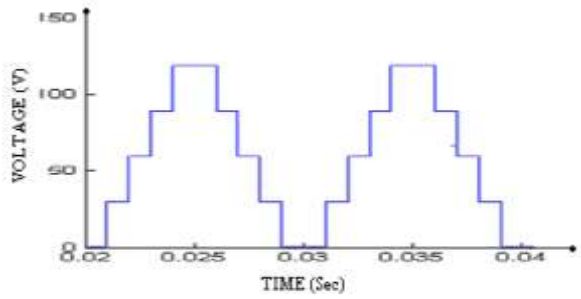

Fig 2 Output voltage waveform

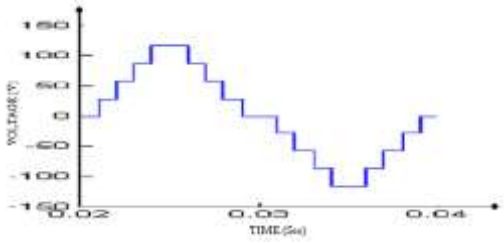

Fig 3 Voltage bus and output voltage wavefroms

One application area in the low power range (< 100 kW) for the MLDCL inverters is in PM motor drives employing a PM motor of very low inductance. The proposed inverters can utilize the fast-switching capable, low cost low-voltage MOSFETs in the half-bridge cells, the diode-clamped or capacitor-clamped phase legs and IGBTs in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photo voltaic[1]

III. PULSE WIDTH MODULATION TECHNIQUE

These carrier-based modulation schemes are also applicable for multilevel inverters and they are generally classified into two categories: phase-shifted multicarrier modulation (PSPWM) and level-shifted multicarrier modulation (LSPWM).The other multicarrier methods such as carrier rotation pulse width modulation (CRPWM) and modified level shifted multicarrier pulse width modulation techniques .These methods require complex shape of the carrier signal and difficult to implement as the number of levels increases. The PSPWM is applicable for CHB and FCMLI topologies only where as the LSPWM is topology independent [4] [8].

Level-Shifted Multicarrier Modulation:

Similar to the phase-shifted modulation, an n-level inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular

carriers, all having the same frequency and peak-to-peak amplitude. The (m-1)triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index (m_f) is remains same as that for the phase-shifted modulation scheme whereas the amplitude modulation index (m_a) is defined as

$$m_a = \frac{V_m}{V_{cr}(m-1)} \quad \text{----------(1)}$$

Where Vm the peak amplitude of the modulating is signal and v_{cr} is the peak amplitude of each carrier signal and □ is the number of levels in the inverter. There are three alternative level-shifted modulation techniques have been reported in the literature depending upon the phase relation between individual carriers[3] [4]

1. Phase Opposition Disposition (POD): In this carriers
above the reference zero point are out of phase with those
below zero by 180o.
2. Alternative Phase Opposition Disposition (APOD): In this
carriers in adjacent bands are phase shifted by 180o.
3. Phase Disposition (PD): In this all carriers are in phase
across all bands.

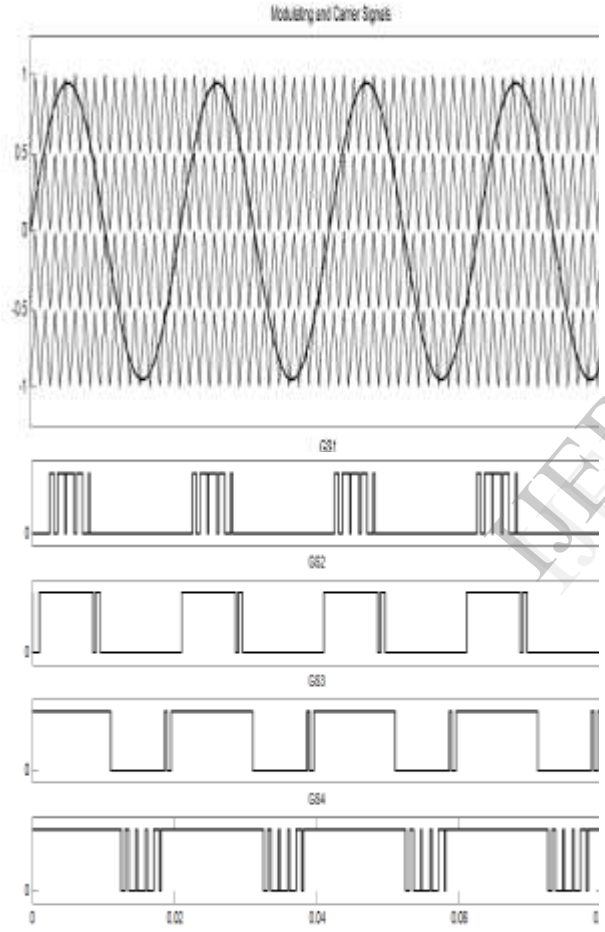

Fig 4 Waveform of Level shift PWM technique

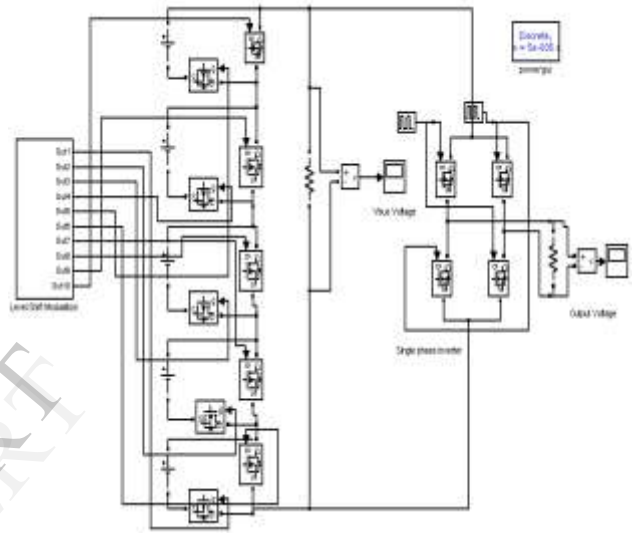

Fig 5 Simulation circuit diagram

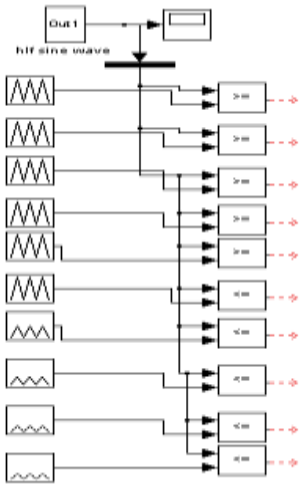

Fig 6 simulation model for LSPWM

IV SIMULATION RESULTS

Below are the simulation results for LSPWM applied to MLDCLI. Fig 5 shows the Simulink circuit diagram the results of 1-Φ and 3-Φ are shown in figs 10 & 11.

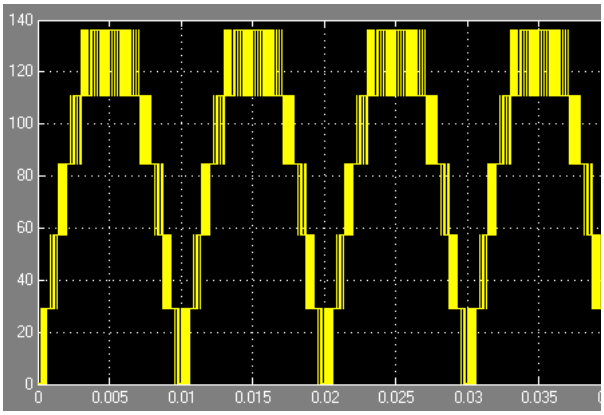

Fig 7 V_{bus} voltage with R-Load

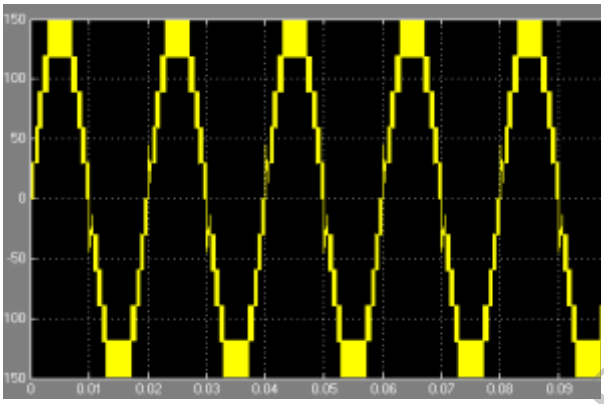

Fig 8 Voltage waveform RL load

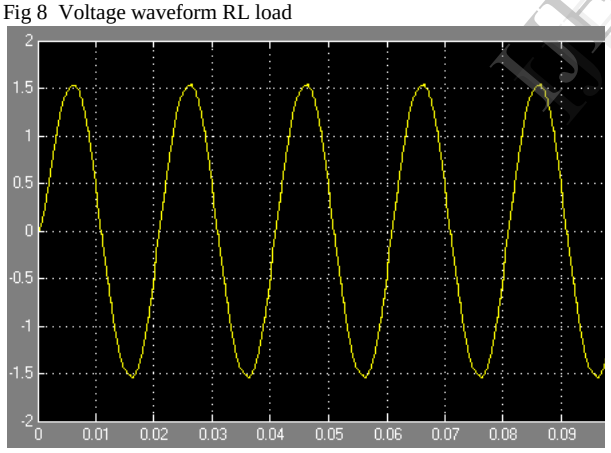

Fig 9 Current waveform in RL

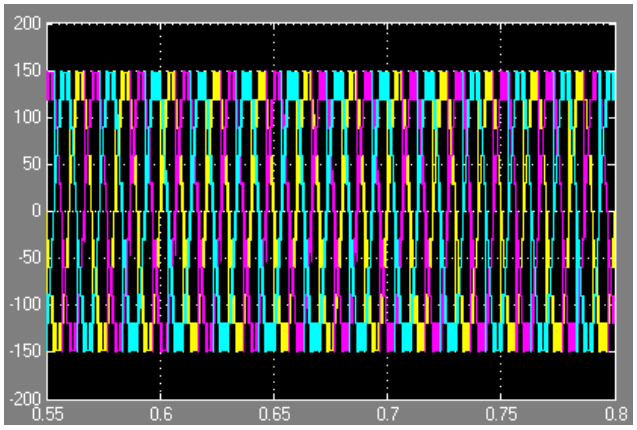

Fig 10 3-Φ Voltage waveform for RL Load

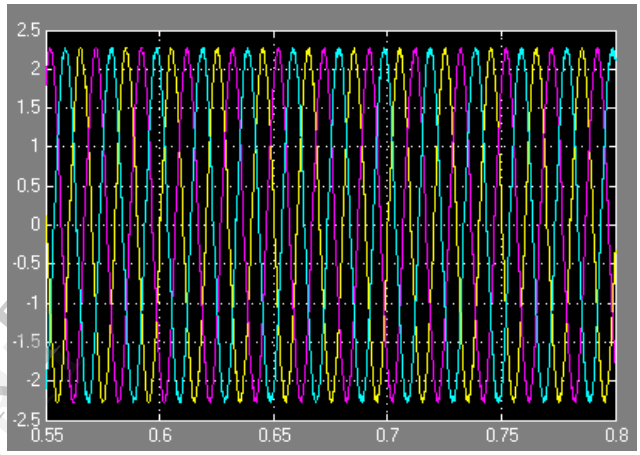

Fig 11 3-Φ Current waveform for RL Load

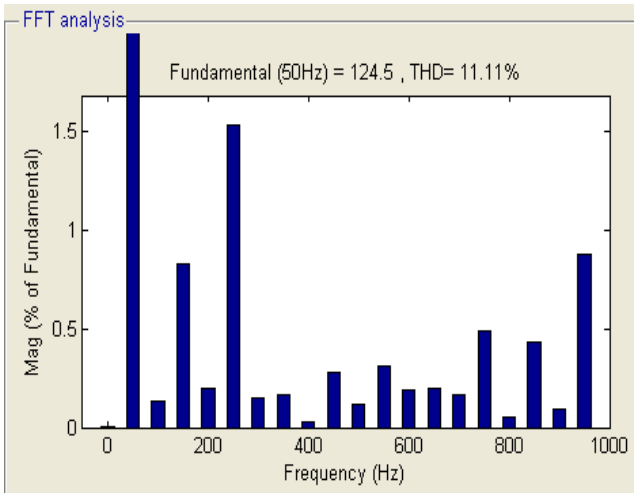

Fig 10 shown THD of R load for 1-Φ output

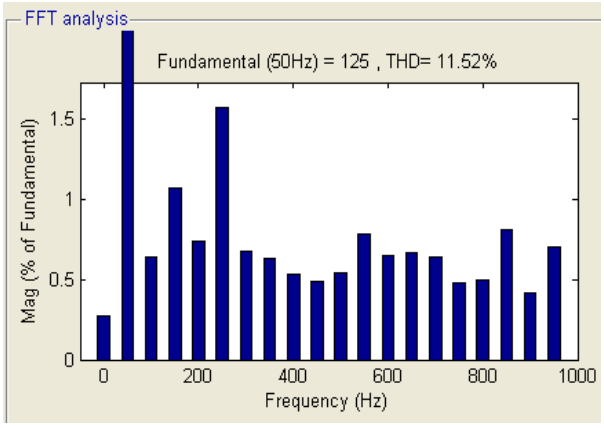

Fig11 shown THD of RL load for 1-Φ output

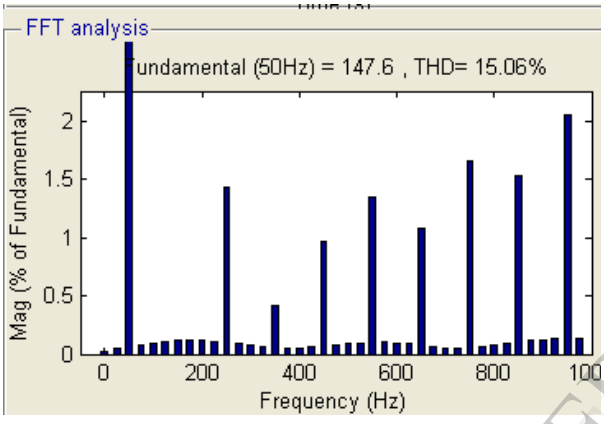

Fig 12 shown THD of RL load for 3-Φ output

V CONCLUSION

With other Multilevel inverters the size, circuit complexity, cost is more when compared with MLDCL inverter. In this paper, cascaded H bridge Eleven Level MLDCL can reduce the number of switching devices, so that the size and the cost of the topology reduced. Total Harmonic distortion for R & RL is 11.11 and 11.52 respt.for single phase output and 15.06 for three phase output. we can implement the same circuit in Hardware using FPGA and DSP controllers

VI ACKNOWLEDGEMENT

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