

# New Generation Transistors

\*K.V.Naveen Kumar ,\*T. Bhargav ,\*T.Sandeep,\*\*T.S.R.Prasad,\*\*T.Ravi

\*Final Year B.Tech ,Department Of Ece ,K L University ,Vaddeswaram, Ap, India

\*\*Assistant Professor M.Tech(P.Hd), K L University

## Abstract

Advancing the silicon transistor has always been a process of addition and subtraction: add power and efficiency while making the unit itself ever smaller. This has been important because the silicon transistor is essentially the building block for modern consumer electronics—the smaller and more powerful we can make them, the smaller, more powerful, and more capable we can make our personal tech. Recently, it looked as if we were reaching our limits in moving the traditional planar (that is, two-dimensional) transistor forward. Moore's Law, it seemed, was in danger, and with it our ability to keep up our blistering pace of technological advancement. Thanks to Intel for its revolutionary invention "Tri-Gate 3-D transistor", however, Moore's Law may now continue to hold true for years to come. This has several advantages: First, it maximizes current flow in the "on" state while bringing it as close to zero as possible in the "off" state for highly increased efficiency at all times; second, it can transfer between the two states with blistering speed, switching between on and off over 100 billion times per second; third, performance can be boosted by connecting the transistors together, and thanks to their vertical structure, a high number can be concentrated together on an integrated circuit. (Did we mention that the Tri-Gate 3-Ds are a mere 22 nanometers, meaning over 100 million can fit on the head of a pin?). 3-D Tri-Gate transistors enable chips to operate at lower voltage with lower leakage, providing an unprecedented combination of improved performance and energy efficiency compared to previous state-of-the-art transistors. The capabilities give chip designers the flexibility to choose transistors targeted for low power or high performance, depending on the application. The 22nm 3-D Tri-Gate transistors provide up to 37 percent performance increase at low voltage versus Intel's 32nm planar transistors. This incredible gain means that they are ideal for use in small handheld devices, which operate using less energy to "switch" back and forth. Alternatively, the new transistors consume less than half the power when at the same performance as 2-D planar transistors on 32nm chips. "The performance gains

and power savings of Intel's unique 3-D Tri-Gate transistors are like nothing we've seen before," said Mark Bohr, Intel Senior Fellow. "This milestone is going further than simply keeping up with Moore's Law. The low-voltage and low-power benefits far exceed what we typically see from one process generation to the next. It will give product designers the flexibility to make current devices smarter and wholly new ones possible.

## Contents:

### Introduction

- Traditional Planar Transistor
  - Design of 32nm Transistor
- The 3-D Trigate Transistor
  - Design of 22nm Transistor

### What's a FIN?

### Future of Computing

### What does it mean for us?

### Tri-Gate Transistors Benefits

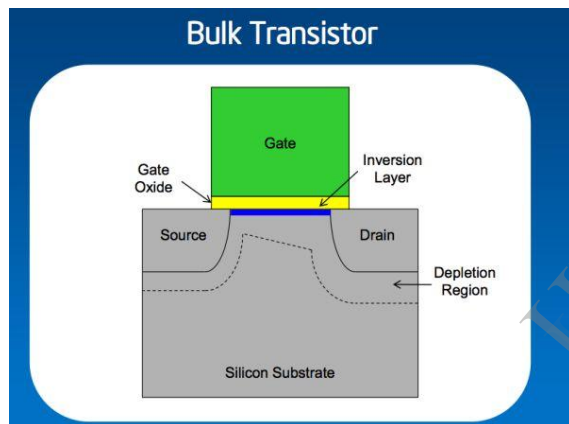
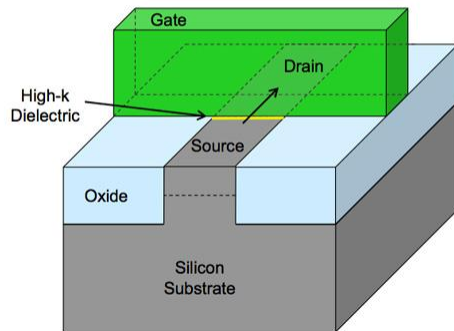
### Bibilography

## Introduction:

Transistors are the building blocks of microprocessors, which are the 'brains' or computational devices inside PCs, laptops, smartphones and pretty much all modern electronic devices. A transistor is essentially an automated switch that can store information as either a '1' or a '0', depending on whether the switch is on — letting electric current through — or off. The wiring of several transistors together creates a device called a logic gate, which takes these ones and zeros and performs basic calculations with them. Home computers available today contain billions of transistors wired into logic gates, and have huge processing power as a result.

Here's a simple diagram of a standard 32nm planar transistor, exactly what you'd find in a Sandy Bridge CPU:

## Traditional Planar Transistor



The goal of a transistor is to act as a very high speed electrical switch. When on, current flows from the transistor's source to the drain. When off, current stops. The inversion layer (blue line above) is where the current flow actually happens.

Ideally a transistor needs to do three things:

- 1) Allow as much current to flow when it's on (active current)
- 2) Allow as little current to flow when it's off (leakage current)
- 3) Switch between on and off states as quickly as possible (performance)

The first item impacts how much power your CPU uses when it's actively doing work, the second impacts how much power it draws when idle and the third influences clock speed.

In conventional planar transistors it turns out that voltage in the silicon substrate impacts leakage current in a negative way. Fully depleted SOI (silicon on insulator) is an option to combating this effect.

The smaller you make the transistors, the more difficult it is to make advancements in all three of these areas all while increasing transistor density. After all not only do you have to worry about keeping power under control, but the whole point to shrinking transistor dimensions is to cram more of them into the same physical die area, thus paving the way for better performance (more cores, larger caches, higher performance structures, more integration).

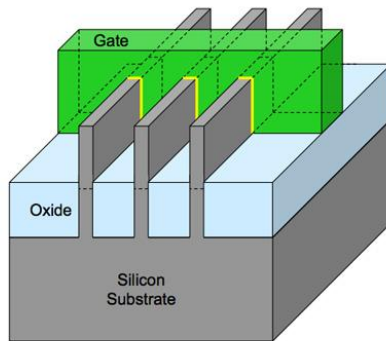
### The 3D Tri-Gate Transistor

A 3D Tri-Gate transistor looks a lot like the planar transistor but with one fundamental change. Instead of having a planar inversion layer (where electrical current actually flows), Intel's 3D Tri-Gate transistor creates a three-sided silicon fin that the gate wraps around, creating an inversion layer with a much larger surface area.

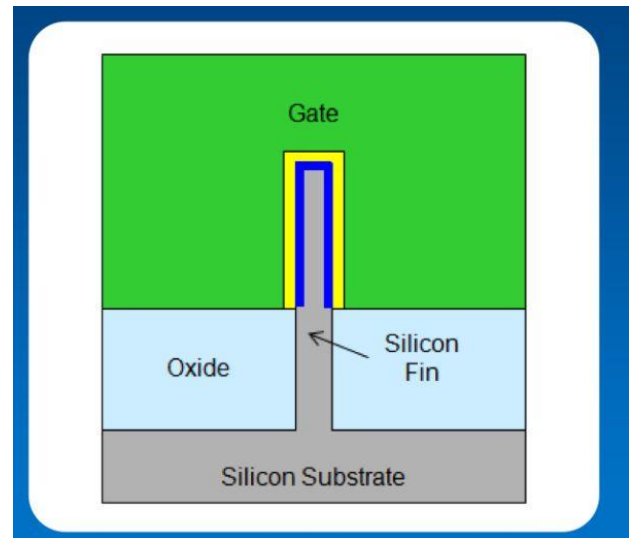
### What's a Fin?

The gate wraps around the fin. The current is controlled by using a gate on each of the three sides of fin - two on each side and one across the top - rather than just one on the top, as in case with the 2D planar transistors. Intel's explanation here is simple and clear: "the additional control enables as much transistor current flowing as possible when transistor is in the ON state (for performance) and as close to zero as possible when it is in OFF state (to minimize power) and enables the transistor to switch very quickly between the two states.

## 22 nm Tri-Gate Transistor



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance



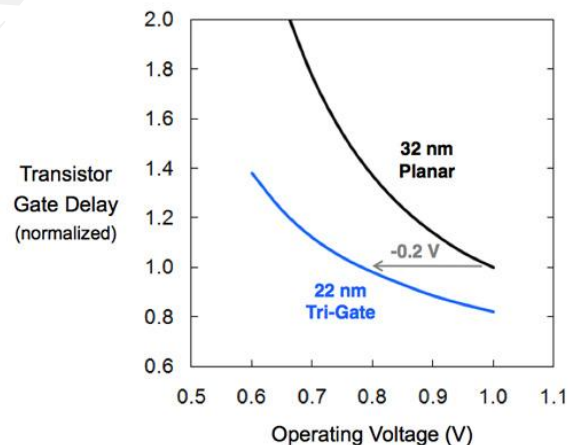
There are five outcomes of this move:

- 1) The gate now exerts far more control over the flow of current through the transistor.
- 2) Silicon substrate voltage no longer impacts current when the transistor is off.
- 3) Thanks to larger inversion layer area, more current can flow when the transistor is on.
- 4) Transistor density isn't negatively impacted.
- 5) You can vary the number of fins to increase drive strength and performance.

The first two points in the list result in lower leakage current. When Intel's 22nm 3D Tri-Gate transistors are off, they'll burn less power than a hypothetical planar 22nm process.

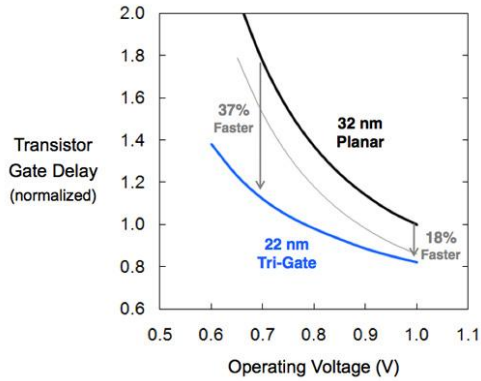
The third point is particularly exciting because it allows for better transistor performance as well as lower overall power. The benefits are staggering:

## Transistor Gate Delay



At the same switching speed, Intel's 22nm 3D Tri-Gate transistors can run at 75 - 80% of the operating voltage of Intel's 32nm transistors. This results in lower active power at the same frequency, or the same active power at a higher performance level. Intel claims that the reduction in active power can be more than 50% compared to its 32nm process.

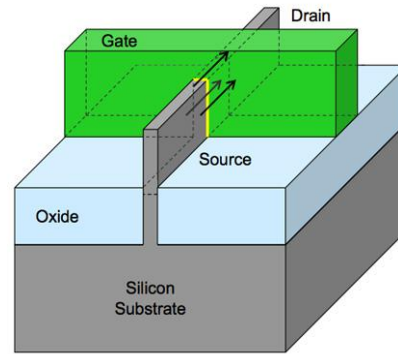
## Transistor Gate Delay



At lower voltages Intel is claiming a 37% increase in performance vs. its 32nm process and an 18% increase in performance at 1V. High end desktop and mobile parts fall into the latter category. Ivy Bridge is likely to see gains on the order of 18% vs. Sandy Bridge, however Intel may put those gains to use by reducing overall power consumption of the chip as well as pushing for higher frequencies. The other end of that curve is really for the ultra mobile chips, this should mean big news for the 22nm Atom which I'm guessing we'll see around 2013.

Intel is claiming a 2x density improvement from 32nm to 22nm (you can fit roughly twice as many transistors in the same die area at 22nm as you could on Intel's 32nm process).

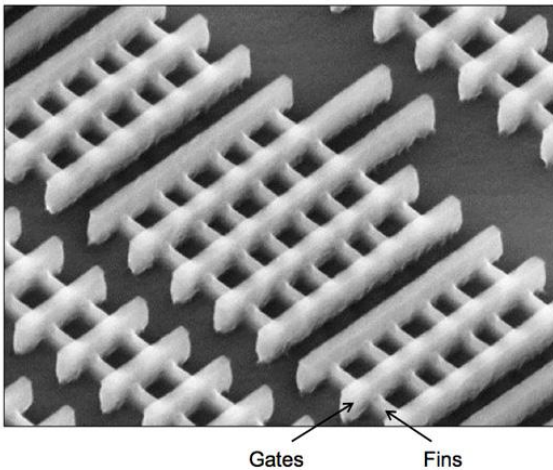
## 22 nm Tri-Gate Transistor



It's also possible to vary the number of fins to impact drive strength and performance, allowing Intel to more finely tune/target its 22nm process to various products.

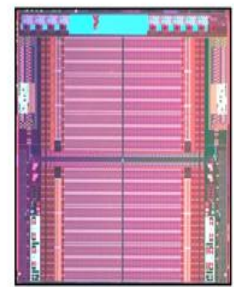
The impact on manufacturing cost is also minimal. Compared to a hypothetical Intel 22nm planar process, the 3D Tri-Gate process should only cost another 2 - 3%

## 22 nm Tri-Gate Transistor



## 22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3<sup>rd</sup> generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs



22 nm SRAM, Sept. '09

22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. '09

Intel is now demonstrating the world's first 22 nm microprocessor (Ivy Bridge) and it uses revolutionary Tri-Gate transistors

You'll note that the move to 3D Tri-Gate transistors doesn't negatively impact transistor density. In fact

All 22nm products from Intel will use its 3D Tri-Gate transistors.



## What Does This Mean

Intel's Ivy Bridge is currently scheduled for a debut in the first half of 2012. Intel is purposefully being vague about the release quarter as Sandy Bridge is doing well and isn't facing much competition at the high end at least.

The impact of Intel's 22nm 3D Tri-Gate transistors on high end x86 CPUs will be significant. Intel isn't expecting its competitors to move to a similar technology until 14nm. The increases in switching speed at the same voltage could allow Intel to finally hit or exceed that magical 4GHz barrier in a stock CPU. I suspect Intel will likely use the gains to deliver lower power CPUs however there's always the possibility of some very fast Extreme Edition parts.

The bigger story here actually has to do with Atom. The biggest gains Intel is showing are at very low voltages, exactly what will benefit ultra mobile SoCs. Atom has had a tough time getting into smartphones and while we may see limited success at 32nm, the real future is what happens at 22nm. Atom is due for a new microprocessor architecture in 2012, if Intel goes the risky route and combines it with its 22nm process it could have a knockout on its hands.

### Intel's 3D Transistor: Why It Matters

Intel's 3D transistors are no small feat. Some are calling it a breakthrough that will allow Intel to continue to make chips that adhere to Moore's Law (i.e. the number of transistors that can be placed on a circuit will double every two years).

Even that impressive feat is just business as usual. After all, Moore's Law has been in effect for decades. The bigger news would be if Moore's Law no longer applied to Intel chips.

So what's the big deal with Intel's 3D transistors? The answer lies in more than just smartphones, tablets, and set-top boxes. This fundamental new way of making the circuits of microchips could have a dramatic impact on everything from the smallest handheld devices to the biggest datacenters.

### The Future of Computing

There's no denying that the future of computing lies in small, low-power solutions coupled with big-iron cloud services. Smartphones are becoming personal computers, powerful enough to run simple desktop computing environments. Tablets are cannibalizing

laptops. Entire home entertainment experiences are being jammed into tiny set-top boxes and embedded into televisions. Even Microsoft's next version of Windows will run on low-power ARM-based chips.

Intel hasn't excelled in all of these areas. It has a presence in televisions, thanks to Google TV and the Boxee Box, but so far the company hasn't gained much traction in smartphones and tablets. Intel's Moorestown chips are largely ignored. Its Medfield chips aren't due to appear in any products until later this year, and they still may not fare well against the more-established ARM processors.

With 3D transistors, Intel may finally have the ammunition it needs to do battle in the smartphone and tablet markets. Intel claims its new transistors can switch 37 percent faster than those made with its existing 32-nm process in chips that operate at low voltage, or 18% faster in chips that operate at high voltage. Transistors switching at the same speed as those in the company's 32nm chips can operate at significantly lower voltage, cutting power consumption in half. This change in how chips are produced is expected to raise production costs by a modest 2 or 3%, which is well worth the dramatic improvement in performance.

### What It Means for You :

The first products to hit the market using this new manufacturing technique will be Intel's "Ivy Bridge" line, the successor line to the current "Sandy Bridge" line. This means the new technology will first appear in laptops, desktops, and servers that use Intel's chips. The faster switching speeds, lower voltage operation, and lower leakage should make Ivy Bridge processors considerably more energy-efficient than the Sandy Bridge CPUs in systems today. These products are expected to hit the market in early 2012.

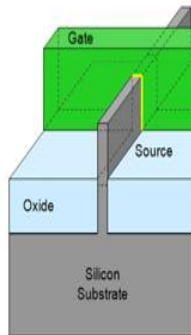
It will take more time for the 22nm process, and its associated 3D transistor technology, to show up in Intel's low-power Atom CPU lineup and system-on-chips designed for smartphones and tablets. In April, Intel said it would release its first true ARM competitor in 2013. This manufacturing technology is what will make that product possible.

Intel will use this 3D transistor structure on all chips produced on its 22nm manufacturing process, regardless of the type of chip or to which market it is targeted. The upsides should be considerable and the downsides minimal. Other chip fabrication companies have been working on 3D gate structures, but aren't expected to bring them to market for some time. Most of Intel's competitors aren't expected to

ship 22nm high-performance products until at least late 2012, and won't use a 3D gate structure similar to Intel's until the next major manufacturing process step, a couple of years later.

## Tri-Gate Transistor Benefits

- Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
  - 37% performance increase at low voltage
  - >50% power reduction at constant performance
- Improved switching characteristics (On current vs. Off current)
- Higher drive current for a given transistor footprint
- Only 2-3% cost adder (vs. ~10% for FDSOI)



### Gated SOI Transistor With Variable Vt and 0.5V Operation Achieving Near Ideal Subthreshold Slope" SOI Conference, 2007 IEEE International

4)Huang, X. et al. (1999) "Sub 50-nm FinFET: PMOS" International Electron Devices Meeting Technical Digest, p. 67. December 5–8, 1999.

5)Hisamoto, D. et al. (1991) "Impact of the vertical SOI 'Delta' Structure on Planar Device Technology" IEEE Trans. Electron. Dev. 41 p. 745.

### BIOGRAPHY :

K .V.NAVEEN KUMAR was born in 1991 in Guntur district pursuing B.TECH at K L UNIVERSITY ,GUNTUR DISTRICT and interested in wireless communications

T.BHARGAV was born in 1992 in Guntur district pursuing B.Tech at K L University, Guntur District and interested in Telecommunications.

T.SANDEEP was born in 1991 in Krishna district pursuing B.Tech at K L University, Guntur District and interested in Wireless systems and Computer networks.

T.Ravi M.TECH(PH.D)was born in 1972 at Guntur District. He is currently teaching at K L University. He is interested in Image Processing and networking.

T.SIVA RAM PRASAD MTECH(PH.D) was born in 1978 at Krishna district .he is currently working as assistant professor in k l university .he is interested in mobile communications

### Bibliography



various websites:

www.wikipedia.com, www.pcworld.com, news.cnet.com

1)Subramanian V (2010). "Multiple gate field-effect transistors for future CMOS technologies". IETE Technical Review**27**: 446–454.  
<http://www.tr.ietejournals.org/article.asp?issn=0256-4602;year=2010;volume=27;issue=6;page=446;epage=454;aualast=Subramanian>.

2)Wong, H-S. Chan, K. Taur, Y. "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel" IEDM 1997, p.427

3)Wilson, D.; Hayhurst, R.; Oblea, A.; Parke, S.; Hackler, D. "Flexfet: Independently-Double-