Neuro Fuzzy Control Single – Stage Single Phase AC-DC Converter for High Power factor

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Abstract: This project presents a novel design of Proportional and integral (PI) like Neuro-Fuzzy logic controller (NFLC) for AC-DC converters that integrates linear control techniques with Neuro-Fuzzy logic .The design procedure allows the small signal model of the converter and linear control design techniques to be used in the initial stages of NFLC design .This simplifies the small signal design and stability assessment of the NFLC. By exploiting the Neuro-Fuzzy logic structure of the controller, heuristic knowledge is incorporated in the design, which results in a nonlinear controller with improved performance over linear PI controllers. The major advantage of the proposed design method for NFLC is that compared to other methods is trail and error effort in the design is greatly reduced.

Index Terms—Fast output regulation, integrated buck-fly back converter (IBFC), low cost, low urrent stress, power factor correction, single-stage (SS) ac–dc converter.

I Introduction:SINGLE-STAGE (SS) high-power-factor (HPF) integrated converters have proven to be a good solution to implement power supplies that comply with harmonic regulations .SS converters integrate an input current shaper (ICS) ac–dc converter with a second dc–dc conversion stage, and use a bulk capacitor between them to attain fast output voltage regulation. At first glance, the ICS stage can be based on typical simple and well-known converters such as the boost or buck-boost, which are widely used for offline HPF applications [2]–[5]. The SS converter can operate either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The operation in CCM offers the advantage of requiring lower rootmean-square (rms) currents through the power switches, which yields higher efficiency. However, operation in CCM presents the disadvantage of having no relationship between the output power and the duty cycle of the control switch. This finally causes a high bulk capacitor voltage at low output power levels. This is an important disadvantage especially when a universal input voltage range is pursued. The other possibility is the operation of a SS dc–dc converter in DCM. In this case, the output power will depend on the duty cycle of the control switch. The operation with both inductors of the ICS and dc–dc converter in DCM is particularly interesting. In this case, the ratio between bulk capacitor voltage and the peak line voltage will depend only on the two inductances ratio, being independent of the output power. This means that a reasonable bulk capacitor voltage can be maintained for the universal input voltage range. Besides, a high bulk capacitance is not necessary, since the voltage ripple across this capacitor, at double line frequency, can be compensated by closed-loop operation. This is due to the fact that the bulk capacitor voltage is independent of the duty cycle. Therefore, the changes on the duty cycle will affect only the output voltage, thus making it possible for a fast output voltage regulation. The ICS buck converter can be integrated with the flyback dc–dc converter to obtain a very simple and well-suited topology for this sort of application. One of the advantages is that in this topology no center-tapped transformer is required, as opposed to other typical SS topologies based on the boost converter. The integrated buck-flyback converter (IBFC) has previously been proposed for other applications such as dc–dc conversion [28] and electronic ballasts [29], but has not been well investigated for HPF off-line dc power supplies. When operated in DCM, since the ratio of the bulk capacitor voltage and the peak line voltage depends only on the buck and flyback inductance ratio, the use of the buck converter as ICS permits the operation with low bulk capacitor

voltage. Thus, the conduction angle of the buck converter within the line half period is constant and independent of the peak line voltage. On the other hand, a fast output regulation can be achieved with a proper design of the error amplifier, thus compensating the voltage ripple across the bulk capacitor, and limiting its value to the hold-up time requirement. Another advantage of the IBFC that will be highlighted in this paper is that as opposed to other SS integrated converters, the control switch handles a considerably lower rms current. As will be shown, the current through the control switch is either the buck or the flyback inductor current, whichever is higher, but not the addition of the two currents, as it occurs in other integrated converters. The remaining current is handled by the diodes of the integrated switch, which give lower losses due to their voltage-source equivalent behavior. This characteristic provides quite a higher efficiency for this type of DCMoperated converters. Hence, in this paper the IBFC for HPF off-line applications is investigated. The important design characteristics such as bulk capacitor average voltage, bulk capacitor voltage ripple and currents, and voltages in the switches will be obtained. A universal input (90–250 V) 48 V-output 100 Wac–dc converter operating at 100 kHz will be designed to illustrate the application of the derived characteristic and evaluate the possibilities of this converter.

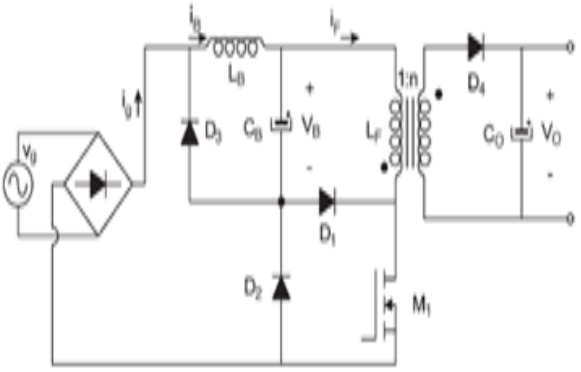


Fig1 HPF integrated buck-flyback ac-dc converter

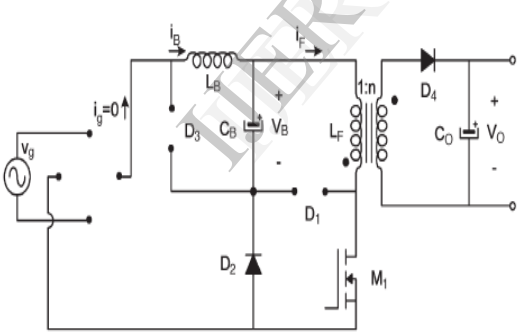


Figure 2(a)*vg* < *V*B. and*M*1 ON

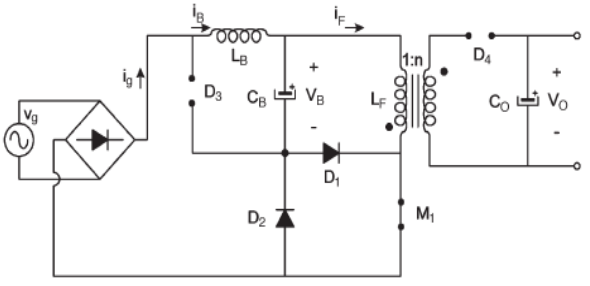


Figure 2(b)) *vg* > *V*B and*M*1 ON

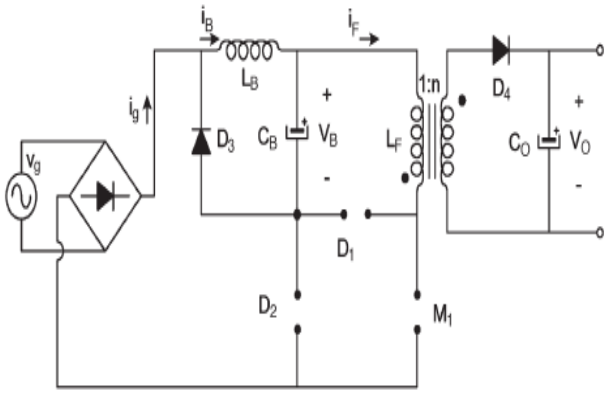


Figure 2(c) *vg* > *V*B. and*M*1 OFF.

II OFF-LINE OPERATION OF THE IBFC:

Fig. 1 illustrates the configuration of the IBFC when operated from an ac line. As stated previously, this converter has already been proposed for other power applications [4], [28], [29], but has not been analyzed and experimented for HPF dc power supplies. The simplest way of operating the IBFC is maintaining the DCM in both buck and fly back inductors. In this way, it will be demonstrated that the bulk capacitor voltage (*V*B) is independent of load, duty cycle and switching frequency, and it only depends on the ac input voltage and the ratio of the two buck and fly back inductances (*L*B and *L*F, respectively). This is an important feature of integrated converters operating in DCM, which allows them to provide fast output voltage regulation. Fig. 2 illustrates the equivalent circuits of the IBFC during a line-half period. In the time intervals where the instantaneous line voltage is lower than the bulk capacitor voltage, the rectifier bridge diodes are reverse biased and remain open. Thus, the buck inductance is not energized and diodes *D*1 and *D*3 are also open during these time intervals. The equivalent circuit is shown in Fig. 2(a). In this mode, only the flyback converter is operating through switch *M*1 and diodes *D*2 and *D*4. The operation is exactly equivalent to a flyback converter, where the energy is taken from the bulk capacitor and delivered to the load. Fig. 2(b) and (c) show the equivalent circuits within the interval in which the instantaneous line voltage is higher than the bulk capacitor voltage. In this interval, both buck and flyback inductors are energized when the control switch *M*1 is activated. Diodes *D*3 and *D*4 will remain open and the currents through the buck and flyback inductors are handled by the integrated switch formed by *M*1, *D*1, and *D*2. To understand how the currents are distributed among the three switches when *M*1 is on, an equivalent circuit is shown in Fig. 3. In this circuit, the switch *M*1 will handle the higher of the two currents *i*B and *i*F (buck and fly back currents, respectively). The diode in parallel with the higher current will be open, whereas the diode in parallel with the lower current will be closed. Since the operation is in DCM, the two buck and fly back currents are ramp waveforms starting at the same instant. Therefore, the conclusion is that the current through switch *M*1 will be either *i*B or *i*F, whichever is higher, but not the addition of the two currents. This is an advantage of this converter compared to other integrated topologies, where the currents of the two stages circulate simultaneously through the control switch. In summary, the current distribution is as follows. When *i*B > *i*F, current *i*B will circulate through *M*1, *D*1 will handle the current *i*B − *i*F, with *D*2 being off. When *i*B < *i*F, current *i*F will circulate through *M*1, *D*2 will handle the current *i*F − *i*B, with *D*1 being off. Finally, Fig. 2(c) shows the equivalent circuit when the line voltage is higher than the bulk capacitor voltage, and the switch *M*1 is open. During this interval, both buck and fly back inductors are being de energized, and the energy is supplied. to the bulk capacitor and load, respectively. In this stage, only diodes *D*3 and *D*4 will be

conducting as long as energy remains in the magnetic field of the buck and flyback inductors, respectively. The highest voltage across the switch *M*1 appears during this interval, which, with reference to Fig. 2(c), can easily be calculated to be *V*g + *V*B + *VO*/*n*.

III ANALYSIS OF THE OFF-LINE IBFC:

A. Basic Analysis

From the point of view of the ac input waveforms, the operation of the IBFC is equivalent to the two converters operating in cascade. The buck converter is only able to operate when the bulk capacitor voltage is lower than the rectified line voltage, thus driving an averaged sinusoidal current, as shown in Fig. 4. Provided that the bulk capacitor voltage is designed to be low enough, a high input-power-factor can be achieved so that the IEC-61000-3-2 standard is accomplished. To derive the bulk capacitor voltage characteristic of the IBFC, Fig. 5 illustrates the equivalent circuit of the buck converter at a low frequency. The buck converter is loaded with the flyback converter, which is represented by its equivalent resistance *R*F. Resistance *R*B represents the equivalent resistance of the buck converter when operating in DCM. It is well

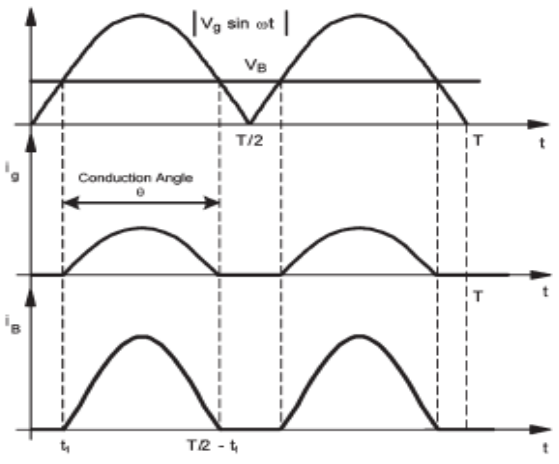


Fig. 4. Input voltage and current waveforms in the IBFC.

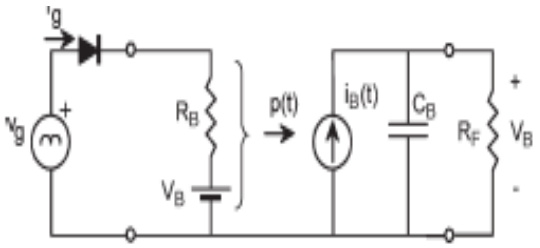


Fig. 5. Equivalent circuit of the IBFC input stage.

known that the values of these resistances are given as follows [29], [30]:

$$R_B = \frac{2L_B f_S}{D^2}, \qquad R_F = \frac{2L_F f_S}{D^2} \tag{1}$$

Where *f*S is the switching frequency and *D* is the duty cycle with which the control switch *M*1 is operated. In the circuit of Fig. 5, the instantaneous power consumed by the resistance *R*B and the voltage source *V*B is transferred to the output section formed by the filter capacitor *C*B and the equivalent resistance of the flyback converter *R*F. This power can be calculated as follows:

$$p(t) = v_g \frac{v_g - V_B}{R_B}, \qquad t_1 \le t \le \frac{T}{2} - t_1. \tag{2}$$

Therefore, assuming negligible ripple voltage across capacitor *C*B, the expression for *i*B(*t*) is subsequently obtained

$$\begin{aligned} i_B(t) &= \frac{p(t)}{V_B} \\ &= \frac{V_g}{R_B}\left(\frac{V_g}{V_B}\sin^2 \omega t - \sin \omega t\right), \qquad t_1 \le t \le \frac{T}{2} - t_1 \end{aligned} \tag{3}$$

where *V*g is the peak line voltage, ω is the line angular frequency, and *T* is the line period. The waveform of *i*B(*t*) has been depicted in Fig. 4. This expression can be normalized for the sake of simplicity as:

$$i_{B\_n}(t) = \frac{i_B(t)}{V_g/R_B} = \frac{1}{m}\sin^2\omega t - \sin\omega t, \qquad t_1 \le t \le \frac{T}{2} - t_1 \quad (4)$$

Where m = VB/Vg is the ratio between the bulk capacitor voltage to the peak line voltage. It must be noted that the current out of the time interval shown in (4) is equal to zero. To obtain the voltage VB, the average value of the current iB_n(t) must be calculated. By integrating (4) within a line period, the following expression is obtained:

$$I_{B\_n} = \frac{1}{\pi}\int_{\frac{\pi-\theta}{2}}^{\frac{\pi+\theta}{2}} i_{B\_n}(\omega t)\,d(\omega t) = \frac{1}{2m}\left(1 - \frac{2}{\pi}\sin^{-1} m\right) - \frac{1}{\pi}\sqrt{1-m^2} \quad (5$$

Where it has been taken into account that the conduction angle θ can be calculated as follows (see Fig. 4):

$$\theta = \pi - 2\cdot\sin^{-1} m. \quad (6)$$

As can be understood from the circuit in Fig. 5, the dc mean current IB will circulate through the flyback equivalent resistance, thus giving a bulk capacitor voltage VB = IBRF. Then, the following equation must be solved to obtain the voltage VB:

$$V_B - I_B R_F = 0 \quad (7)$$

Which can be rearranged as follows:

$$m - \frac{I_{B\_n}}{\alpha} = 0 \quad (8)$$

where α = RB/RF = LB/LF. Using (5) in (8), the following expression is derived:

$$m - \frac{1}{2m\alpha}\left(1 - \frac{2}{\pi}\sin^{-1} m\right) + \frac{1}{\pi\alpha}\sqrt{1-m^2} = 0. \quad (9$$

As can be noticed from (9), the voltage ratio m depends only on the inductance ratio α. Equation (9) can easily be solved by using numerical methods, and plotted as shown in Fig. 6. The characteristic in Fig. 6 is used to design the IBFC to operate with an adequate value of the bulk capacitor voltage, so that the input current distortion would be low enough to fulfill the IEC-61000-3-2 requirements.

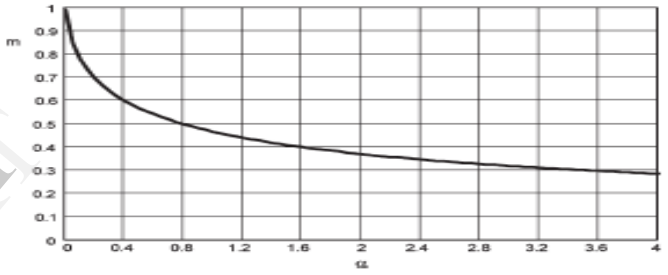


Fig. 6. Voltage ratio m as a function of the inductance ratio α.

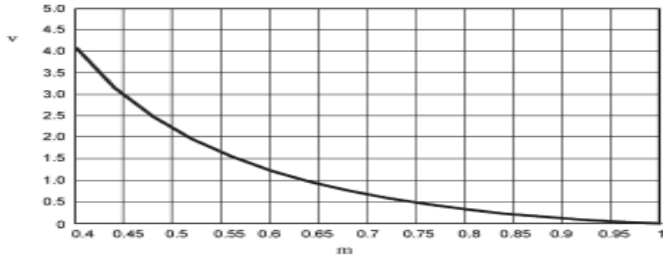


Fig. 7. Ripple factor ν as a function of the voltage ratio m.

B. Bus Voltage Ripple

Another important issue that must be analyzed before a complete design can be performed is the voltage ripple across the bulk capacitor. In a real application, this voltage ripple will distort the input current and increase its harmonic content. Therefore, it must be limited to an appropriate value. The peak-to-peak voltage ripple across the bulk capacitor can be calculated through the charge injected into the capacitor (ΔQ), as follows:

$$\Delta V_{\mathrm{B}} = \frac{\Delta Q}{C_{\mathrm{B}}} = \frac{1}{2\omega C_{\mathrm{B}}} \int_0^{\pi} |i_{\mathrm{B}}(\omega t) - I_{\mathrm{B}}|\, d(\omega t). \qquad (10)$$

This expression can be normalized, and rearranged in the following way:

$$\frac{\Delta V_{\mathrm{B}}}{V_{\mathrm{B}}} = \frac{1}{2\omega R_{\mathrm{B}} C_{\mathrm{B}}} \cdot \frac{1}{m} \int_0^{\pi} |i_{\mathrm{B\_}n}(\omega t) - I_{\mathrm{B\_}n}|\, d(\omega t).$$

Now, the following ripple factor (ν) can be defined in order to simplify expressions:

$$\nu = \frac{\Delta V_{\mathrm{B}}}{V_{\mathrm{B}}} 2\omega R_{\mathrm{B}} C_{\mathrm{B}} = \frac{1}{m} \int_0^{\pi} |i_{\mathrm{B\_}n}(\omega t) - I_{\mathrm{B\_}n}|\, d(\omega t) \quad (12)$$

which has been calculated and plotted as illustrated in Fig. 7. As can be seen in Fig. 7, the ripple factor depends only on the voltage ratio. However, the actual voltage ripple across the bulk capacitor will depend on the power handled by the converter,

TABLE I
PARAMETERS OF THE DESIGN EXAMPLE (FULL POWER OPERATION)

V_g (V_{rms})	D	R_B (Ω)	R_F (Ω)	V_B (V)	ΔV_B (V_{pp})
90	0.60	23.5	58.3	76.4	13.5
170	0.32	84.0	208.1	144.2	7.2
250	0.21	181.7	450	212.1	4.9

TABLE II
COMPONENTS OF THE LABORATORY PROTOTYPE

Component	*Value*
Buck	L_B= 42 µH EF25/3C85, N= 30 T
Flyback	L_F = 105 µH, n= 0.4, L_k= 10 µH EF25/3C85, N_1= 30 T, N_2= 12 T
M_1	Case I: IRFPE50 Case II: SPW17N80
D_1	MUR880
D_2	MUR4100
D_3	MUR840
D_4	MUR820
Bridge rectifier	4 x MUR160
C_B	470 µF / 250 V
C_O	100 µF / 100 V
Clamping snubber	D_S= BA159, C_S= 1.5 nF, R_S= 200 kΩ
EMI filter	L_{COMM}= 15 mH, L_{DIFF}= 1 mH, C_F= 150 nF

due to the presence of the buck resistance *R*B in (12). The actual voltage ripple will be obtained from the ripple factor as follows:

$$\frac{\Delta V_{\mathrm{B}}}{V_{\mathrm{B}}} = \frac{\nu}{2\omega C_{\mathrm{B}} R_{\mathrm{B}}}. \qquad (13)$$

Therefore, as long as *R*B is decreased, for example by increasing the duty cycle, more power will be handled by the converter and delivered to the load, thus increasing the voltage ripple across the bulk capacitor. Since the voltage ratio *m* is constant for each design, the higher voltage ripple will be obtained for the lower value of *R*B. Because the IBFC is intended for operation at constant frequency, the highest voltage ripple will be obtained at the highest value of the duty cycle, which corresponds to the minimum ac line voltage and full output power

C. Output Power

To complete the analysis, it is also necessary to calculate the required duty cycle for each operating point. Neglecting losses in the converter, it can be assumed that the power delivered to the load is equal to the input power of the fly back semi stage, which can be calculated as follows:

$$P_{\mathrm{O}} = \frac{V_{\mathrm{B}}^2}{R_{\mathrm{F}}} = \frac{V_{\mathrm{B}}^2 D^2}{2 L_{\mathrm{F}} f_{\mathrm{S}}}. \qquad (14)$$

From (14), the necessary duty cycle for each operating point is obtained

$$D = \frac{1}{V_{\mathrm{B}}} \sqrt{2 P_{\mathrm{O}} L_{\mathrm{F}} f_{\mathrm{S}}}. \qquad (15)$$

To allow for a proper design, it is important to investigate the duty cycle range available for the operation of the IBFC. Up until now, the operation of the two inductors (buck's and flyback's) in DCM has been assumed, thus making the bulk capacitor voltage independent of the load. The two semistages (buck and flyback) will operate with the same duty cycle, therefore the maximum value will be the following:

$$D_{\max} = \min\{D_{\text{Buck\_Max}}, D_{\text{Flyback\_Max}}\} \qquad (16)$$

where the maximum duty cycle for the buck and fly back semi stages can be calculated as follows:

$$D_{\text{Buck\_max}} = m \qquad (17)$$

$$D_{\text{Flyback\_max}} = \frac{V_{\text{O}}}{nmV_{\text{g}} + V_{\text{O}}} \qquad (18)$$

where *n* is the turn ratio of the flyback inductors. Therefore, there is a first maximum duty cycle given by the voltage ratio *m*, which is fixed by the necessary conduction angle to assure a low current distortion. Then, the flyback turn ratio *n* should be calculated to attain a maximum flyback duty cycle close to the voltage ratio *m*. This will assure the shortest dead times in the flyback output current, thus decreasing peak currents, improving efficiency, and reducing the necessary output filter capacitance. If the voltage ratio *m* is chosen to be very low, trying to achieve a nearly sinusoidal input current, the necessary flyback turn ratio will also be low, increasing peak currents and decreasing efficiency. Nevertheless, with the input current waveform as shown in Fig. 4, the minimum conduction angle to meet the IEC 61000-3-2 Class D is only 75◦, as reported in [27], which, from (6), gives a minimum voltage ratio *m* = 0.8. This is a good figure for the maximum duty cycle, as it makes possible a good design of the converter. On the other hand, the IEC 61000-3-2 Class A is less stringent than Class D. As it is well know, Class A limits are absolute, and easier to fulfill, especially for the low-medium power range for which this converter is intended.

D. Dynamic Behavior

As shown previously, the bulk capacitor voltage is independent of the output power when both semi stages operate in DCM. It only depends on the inductance ratio and the input voltage. Therefore, the output converter will operate similarly to a single converter in which both the input voltage and output power will modify the operating point. The transfer function can be represented by means of first-order responses as follows:

$$G_{\nu\text{d}} = \frac{\hat{\nu}_{\text{O}}}{\hat{d}} = \frac{nV_{\text{B}}}{\sqrt{k}} \frac{1}{1 + \frac{R_{\text{O}}C_{\text{O}}}{2}s} \qquad (19)$$

$$G_{\nu\text{g}} = \frac{\hat{\nu}_{\text{O}}}{\hat{\nu}_{B}} = \frac{V_{\text{O}}}{nV_{\text{B}}} \frac{1}{1 + \frac{R_{\text{O}}C_{\text{O}}}{2}s} \qquad (20)$$

*R*O being the converter load resistance and

$$k = \frac{2n^2 L_{\text{F}}}{R_{\text{O}}}. \qquad (21)$$

IV Design Example

Design a Universal Power Supply that accepts a Single-Phase line voltage from (90-250v_{rms}) at a Switching Frequency 100 KHz, V_0 =48V, I_O =4.2A. Assume the conduction angle θ=120 to Improve Power Factor.

$$m = \sin\frac{\pi - \theta}{2} \qquad \textbf{(22)}$$

$$\text{m} = 0.5 \qquad \textbf{(23)}$$

Since the Voltage ratio is 0.5, the bulk capacitor voltage at lowest line voltage is given by

$$m=V_B/Vg \quad \textbf{(24)}$$

$$0.5 = V_B / (\sqrt{2} * 90)$$

$$V_B = 63.63V. \quad \textbf{(25)}$$

Thus the fly back inductance is given by

$$p_o = \frac{V_B^2 D^2}{2L_F f_s} \quad \textbf{(26)}$$

$$200 = (63.63^2 * 0.5^2)/ (2 * L_F * 100000)$$

$$L_F = 25\mu H \quad \textbf{(27)}$$

The fly back turn'sratio is given by equation

$$D_{Flyback\max} = \frac{V_o}{nmv_g + V_o} \quad \textbf{(28)}$$

In order to have a maximum duty cycle of 0.5 at the lowest line voltage, the necessary turn ratio is obtained as n =0.75. Regarding the buck inductance, using the selected voltage ratio m =0.5 in, a value of the inductance ratio α =0.8 is obtained.

$$\alpha = \frac{L_B}{L_F} \quad \textbf{(29)}$$

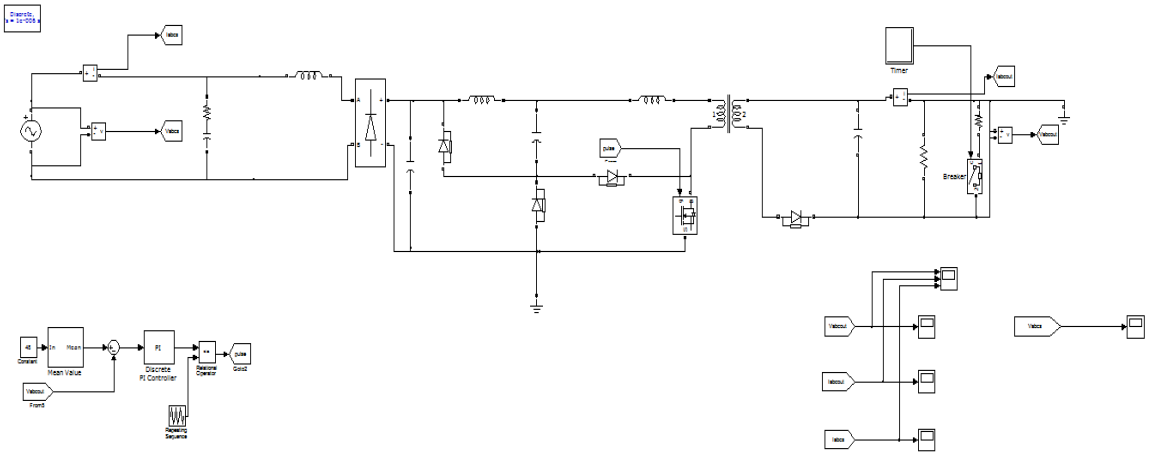
$$L_B = 0.8 * 25\mu$$

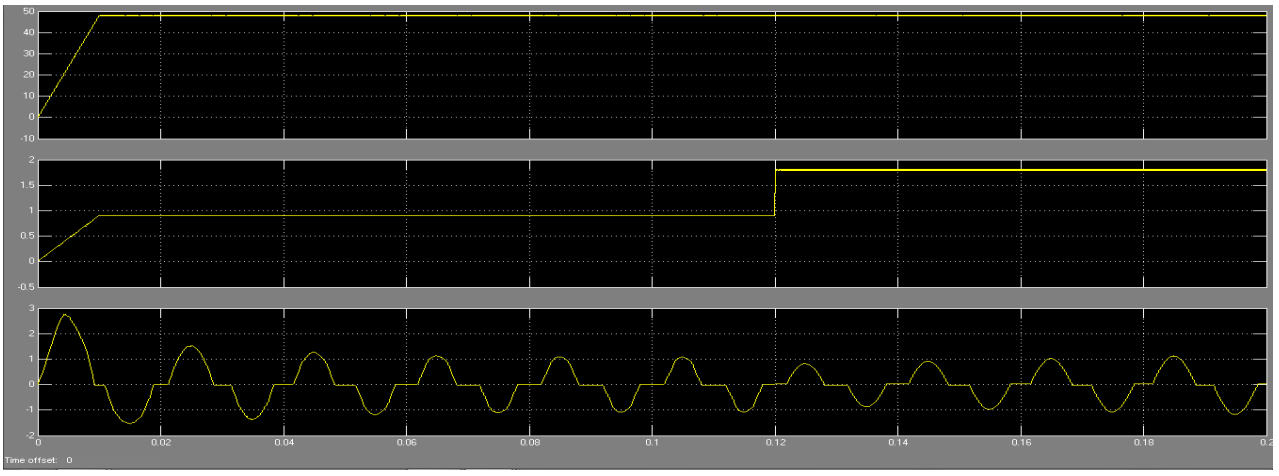
$$L_B = \textbf{20µH} \quad \textbf{(30)}$$

Finally, the design of the bulk capacitance is performed in this example based on the highest voltage ripple allowed. From a ripple factor ν =2.3 is obtained for the selected voltage ratio (m =0.5). The highest voltage ripple will rise at the lowest line voltage and full power. The highest voltage ripple selected in this design is 20% at 90Vand 200W.It should be noted that the voltage ripple will be compensated by the closed-loop error amplifier; thus a very low voltage ripple is not necessary.

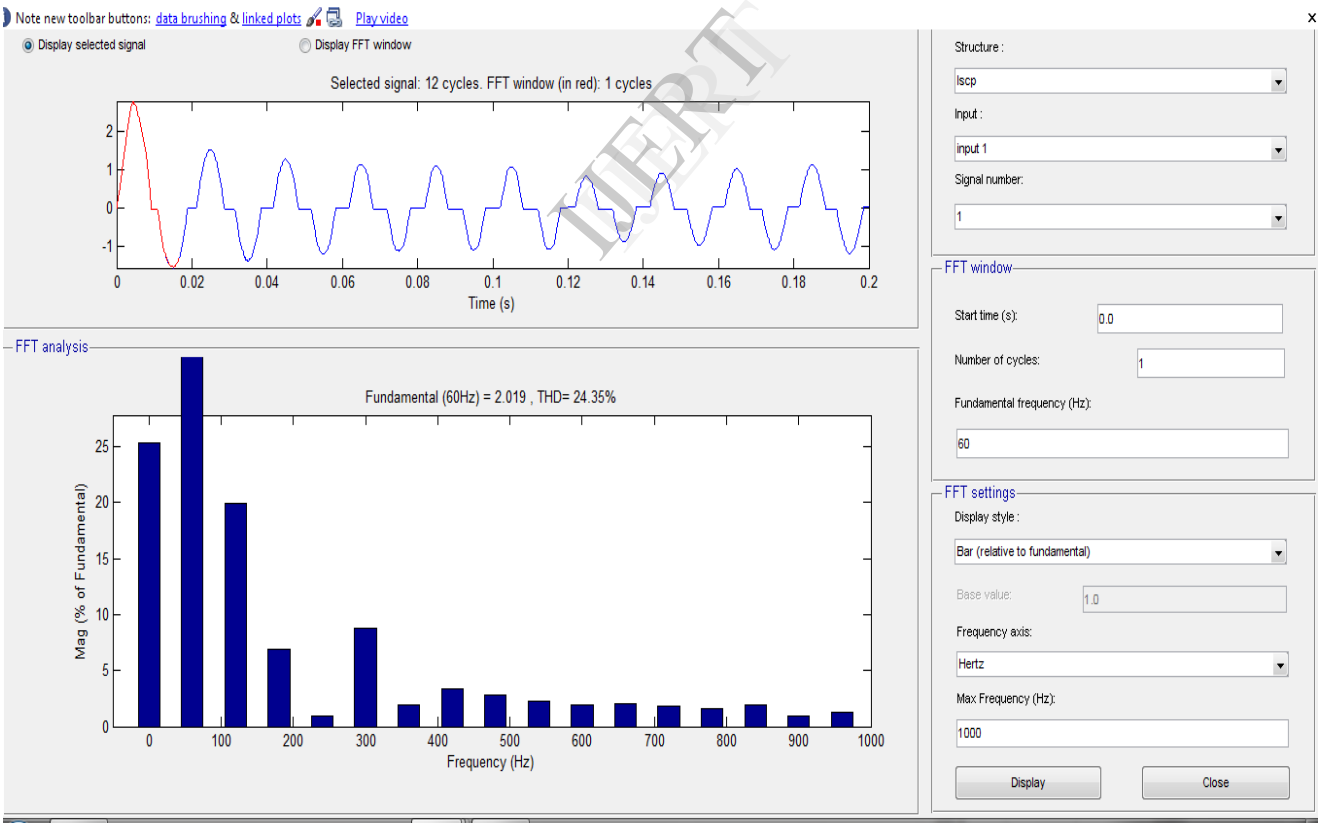
V SIMULATION CIRCUITS AND RESULTS

Integrated Buck-Fly back AC-DC converter using PI controller for High power factor



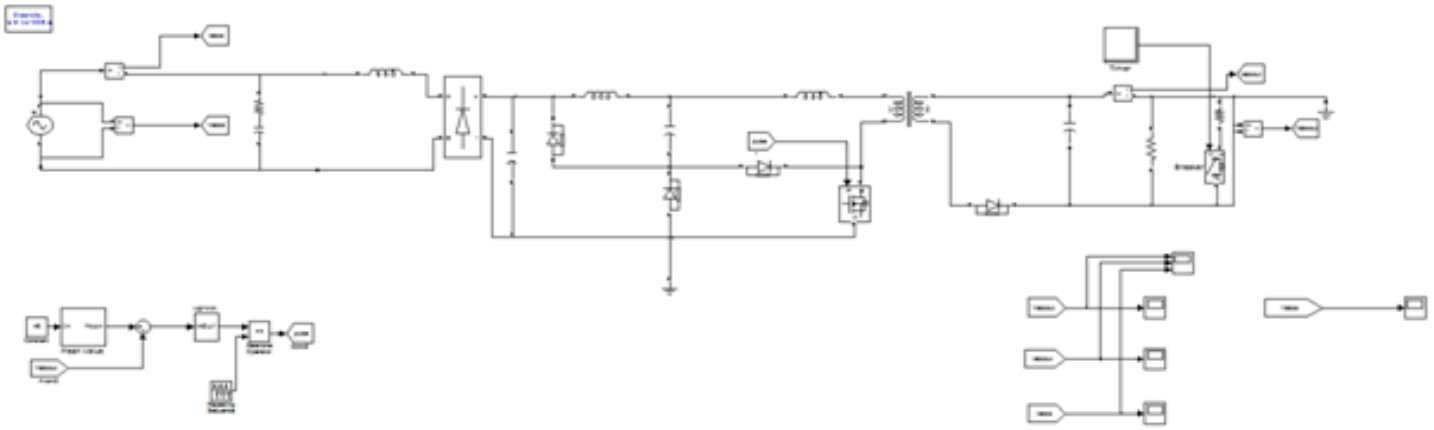


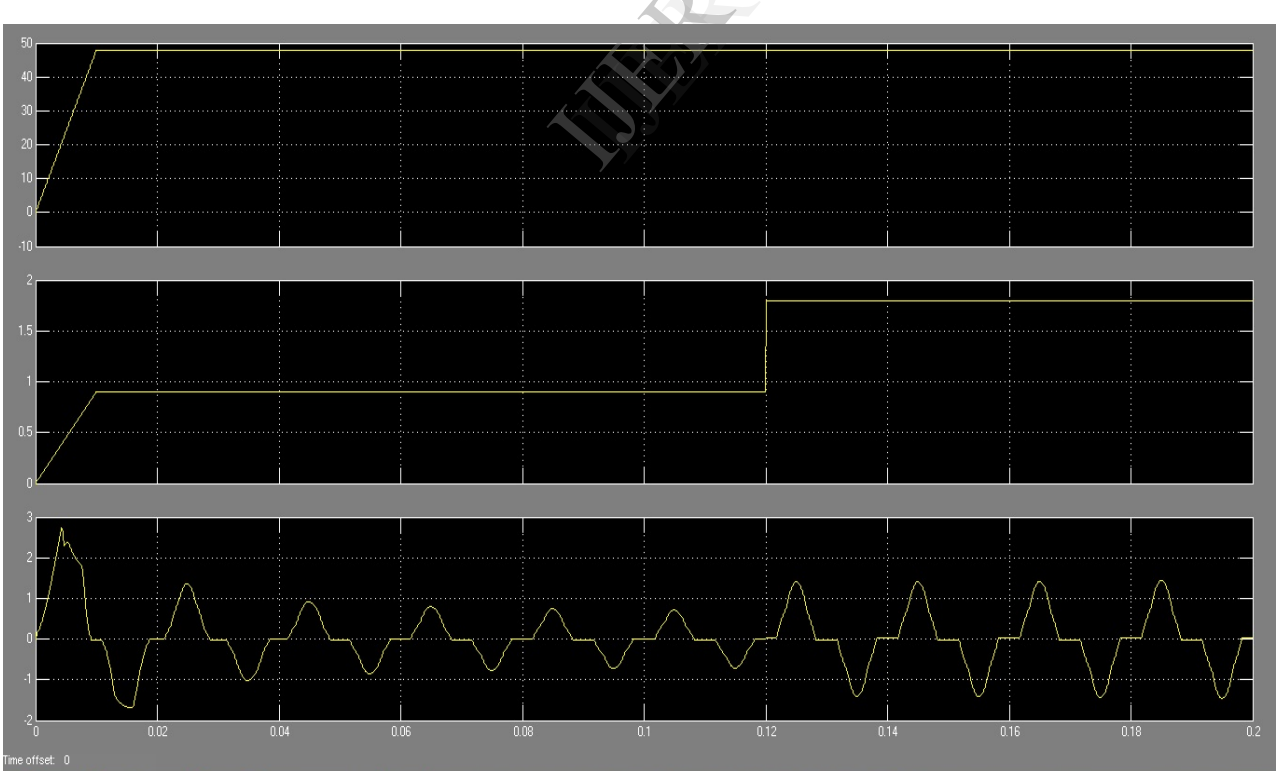
Output voltage, Output current and line current waveforms of IBFC using PI controller



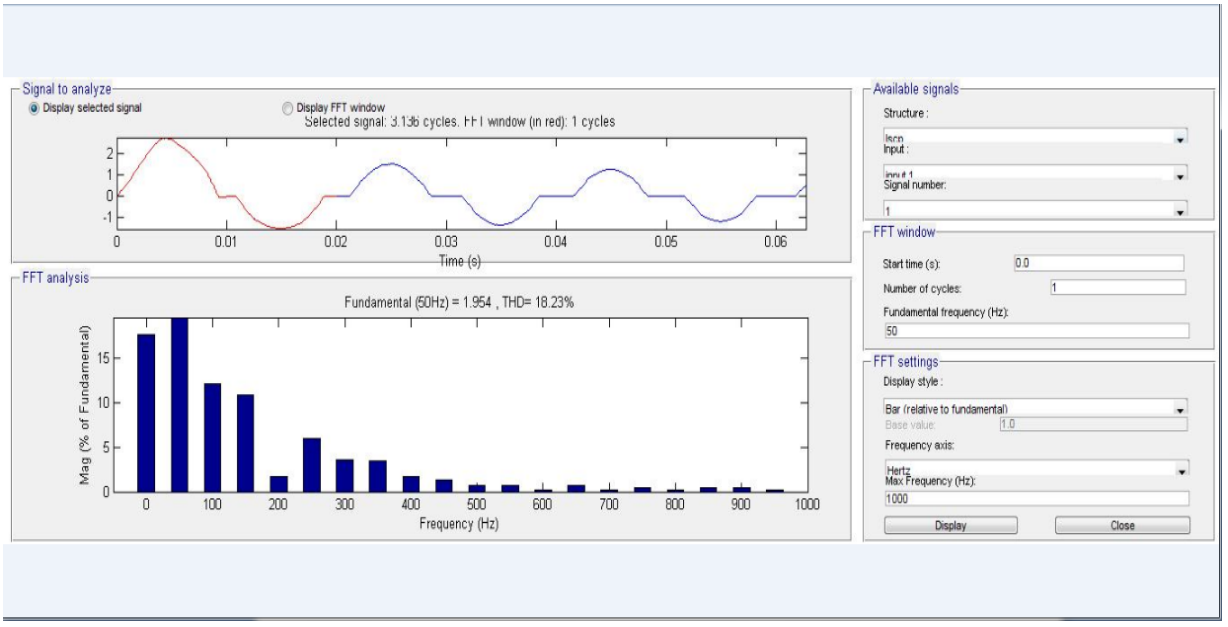
FFT Analysis for IBFC by using PI controller

Integrated Buck-Fly back AC-DC converter using NFLC controller for High power Factor





Output voltage, Output current and line current waveforms of IBFC using NFLC controller



FFT Analysis for IBFC by using NFLC controller

CONCLUSION

This project presented a design procedure of NFLCs for AC-DC converters. the proposed technique allows the small signal model of the converter and linear control techniques to be applied in the initial stages of Neuro- Fuzzy controller design. It also allows linear design techniques to be exploited. The NFLC that was designed using linear techniques serves as a known stating point from which improved performance can achieved by applying heuristic knowledge to obtain a nonlinear controller.

In the PI controller THD range is 24.35% . By using the NFLC the THD range is reduced to 18.23%. Hence the power factor of NFLC controller is improved compare to PI controller.

Performance comparison of PI and NEURO-FUZZY logic controller for high power factor

	PI controller	NFLC controller
THD value	24.35%	18.23%
Power Factor	0.9	0.94

Table: Performance comparison of PI and NEURO-FUZZY logic controller for high Power factor

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