NBTI Aware Power Gating Design Technique: An Overview

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Abstract:- **Negative-bias-temperature instability (NBTI) is becoming the primary limiting factor of circuit life time. It becomes even more critical considering the components for which even minimal parametric variations impact the lifetime of the overall circuit. PMOS header transistor used in power-gated architectures is a relevant example of such component. The sleep transistors in the functional mode are turned-on continuously, Negative Bias Temperature Instability (NBTI) influences the lifetime reliability of PMOS sleep transistors, seriously for these types of devices, an NBTI-induced current capability degradation translates into a larger voltage(IR)-drop effect on the virtual-Vdd rail, which unconditionally affects the performance and, the reliability of all gated cells.**

I. INTRODUCTION

SCALING OF MOS device geometries poses hard limitations on the development of new generations of integrated circuits. In particular, reliability has been indicated as one of the most serious concerns [1], [2]. Adverse on-chip operating conditions, characterized by extremely high substrate temperature, accelerate the degradation of the electromechanical properties of both active (i.e., transistors) and passive (i.e., interconnects) devices. Electro migration, hot-carrier injection, and time-dependent Dielectric breakdown have been indicated as the main responsible of reliability decrease [3]. If we restrict our attention to the aging sources, negative bias temperature instability (NBTI) has emerged as the dominant factor in determining the lifetime of digital devices [4]. In CMOS circuits, NBTI effects occur in p-type transistors when a logic “0” is applied to the gate terminal (gate-to-source voltage $Vgs = -Vdd$, i.e., negative bias). Under this condition, called the stress state, the magnitude of the threshold voltage (Vth) increases over time, resulting in a degradation of the drive current. In contrast, when a logic “1” is applied to the gate terminal (Vgs=0), NBTI stress is actually removed. The latter condition, called the recovery state, induces a progressive yet partial recovery of the Vth [5].

II. LITERATURE REVIEW

a) NBTI Effects

NBTI effect has emerged s a key issue for the reliability of MOSFET. NBTI effect is more prone to the PMOS transistor because it operates in negative Gate to Source Voltage. NBTI effect also occurs in NMOS transistor, but is insignificant.

NBTI manifest effects such as increase in Threshold voltage, resulting in Current Capability degradation, larger delay, and variations in Transconductance too.

Thus the key issues in NBTI are:-

1. NBTI has become the primary limiting factor of circuit life time.

2. PMOS transistor in circuits suffers from static NBTI during active mode and age very rapidly.

3. Negative bias temperature instability is a PMOS aging phenomenon that occurs when PMOS transistors are stressed under negative bias (Vgs = -Vdd) at elevated temperature.

4. NBTI is a key reliability issue in MOS-FETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage [4].

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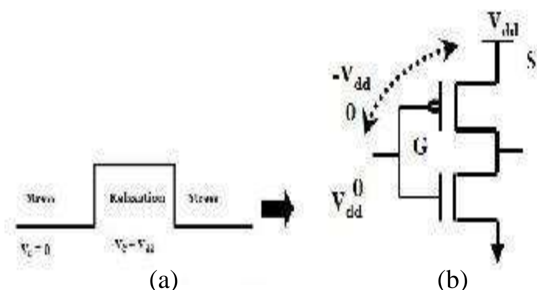

Fig.1 NBTI Effect at the Junction of PMOS transistor

When Vgs of PMOS transistor is at - Vdd, then transistor is said to be in Stress as shown in figure (1) . When negative field is applied at the gate of the PMOS, bond between the SiH atoms breaks results in H+ ion. These ions recombine with other and create a H2 atom which creates a trap between gate and Oxide, which acts as positive field. So this field gets added with the field produced by substrate, so gate to source voltage (Vgs) is required negative enough to create a channel in PMOS. So threshold of the PMOS get affected by this effect Called as "NBTI Effect".

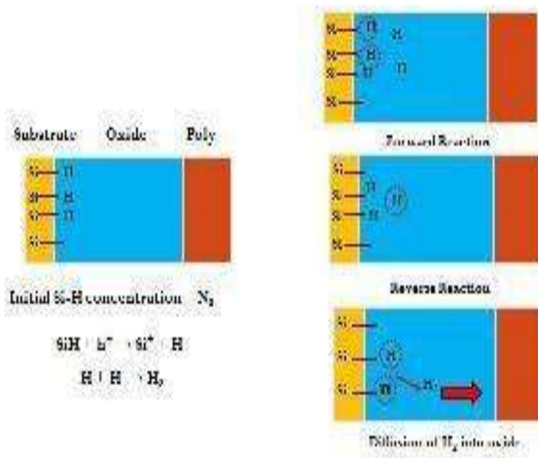

Fig.2 Charge trap inside the transistor between gate and substrate

NBTI-induced PMOS aging result as an increase in the threshold voltage (Vth) and decrease in the drive current (Ids) which intern slow down the logic gates. Experiments on PMOS aging indicate that NBTI effects grow exponentially with thinner gate oxide and higher operating temperature. If the thickness of gate oxide shrinks down to 4nm, the circuit performance can be degraded by as much as 15 % after 10 years of stress and lifetime will be dominated by NBTI.[4][5][12]

b) Technique for reducing NBTI effect

1) Adaptive body bias for reducing impact of die-to-die and within die parameter variation on microprocessor frequency and leakage

A test chip was implemented in a 150nm CMOS technology to evaluate effectiveness of the bidirectional (forward and reverse) adaptive body bias (ABB) technique for minimizing impacts of parameter variations on processor frequency and active leakage power [13]. The test chip contains 21 subsites distributed over 4.5x6.7mm. The Adaptive Body Bias Technique is shown in figure in which each Sub sites has:

- A circuit block (CUT) containing key circuit elements of a microprocessor critical path;
- A replica of the critical path whose delay is compared against an externally applied target clock frequency (') by a phase detector;
- A counter which updates a 5b digital code based on the phase detector output; and

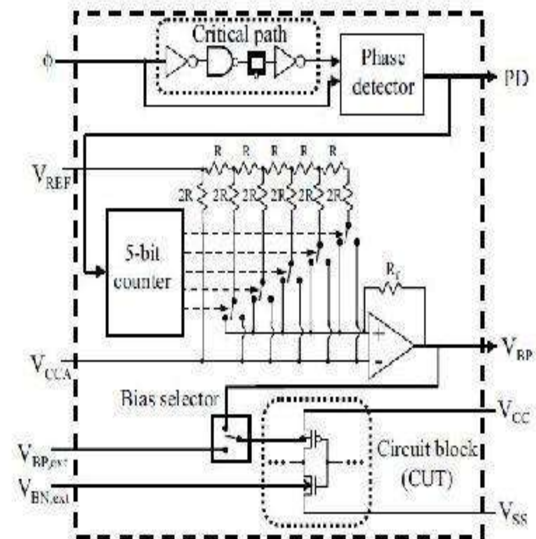

Fig.3 Adaptive Body Bias Technique

- A resistor-ladder D/A converter + op-amp driver which, based on the digital code, provides one of 32 different body bias values to PMOS transistors in both the CUT and the critical path delay elements in two orthogonal orientations [13].

For an externally applied NMOS body bias, this on-chip circuitry generates the PMOS body bias that minimizes leakage power of the CUT while meeting a target clock frequency, as demonstrated by measurements. Different ranges of unidirectional forward (FBB) or reverse (RBB) or bidirectional body bias values can be selected by using appropriate values of VREF and VCCA, and by setting a counter control bit [13].

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2) Design Techniques for NBTI Tolerant Power Gating Architectures

In this technique we characterized the NBTI effects over Power Gating techniques. Then they discussed on selection of PMOS. i.e. NBTI aware sleep transistor design.

Characterization of NBTI effect over Power Gating: - A spice framework was done and they tried to assess the NBTI effect over power gating. Figure 4 show a two phase technique. In first phase, they are trying to estimate aging in terms of current capability degradation. And in second they are trying to estimate the delay degradation [12].

Sleep-Transistor Current Capability Degradation: - This analysis consists of a two-step simulation, the pre-stress simulation phase, in which we estimate the aging effects on the PMOS sleep transistor, and the post-stress simulation phase, in which the stress information is integrated into the PMOS device parameters.

The pre-stress simulation computes the aging of the PMOS sleep transistor after a user defined usage time in the user-defined environmental setup (Vdd voltage, virtual-Vdd voltage, temperature, BB Vbs, and temperature)[5][12].

The amount of aging, calculated is then translated and annotated into device parameter degradation, i.e., threshold voltage degradation (i.e., Vth). As shown in Figure (4) , during post-stress simulation, the NBTI-induced Vth degradation is modelled using a voltage source on the gate terminal of the sleep transistor. After this process, we are able to estimate the degradation over time of the maximum current drained by the PMOS sleep transistor (Ids = Ids0 - Ids), for a given value of usage time and for any operating condition [12].

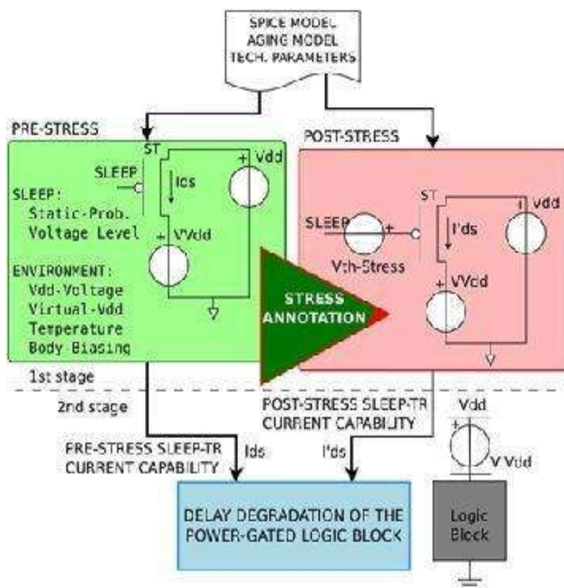

Fig.4 Characterization of NBTI effect over Power gated PMOS

Circuit Delay Degradation:- As we get the degraded value of the maximum drain current Ids now we can estimating actual delay degradation of the power-gated logic. Since the sleep transistor operates in the triode region, it behaves as a resistor. The value of a resistance is given by

Rsleep0 = (Vdd - VVdd)/Ids0 (1)

Now we got the active current Ion drawn from power-gated logic from the virtual rail, we can now estimate the new voltage drop across the sleep transistor as

V'Vdd=R'sleep.Ion (2)

The IR-drop voltage between the real Vdd and the virtual Vdd is used to estimate the actual delay degradation of Power-gated circuit [12].

III. BASIC OF POWER GATING DESIGN TECHNIQUE

Power Gating is an extremely effective scheme for reducing the leakage power of idle circuit blocks. The power (Vdd) to circuit blocks that are not in use is temporarily turned off to reduce the leakage power. When the circuit block is required for operation, power is supplied once again. During the temporary shutdown time, the circuit block is not operational – it is in low power or inactive mode. Thus, the goal of power gating is to minimize leakage power by temporarily cutting-off power to selective blocks that are not active [4].

As shown in Fig.5 power gating is implemented by a PMOS transistor as a header switch to shut off power supply to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into two parts: a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.[3][4]

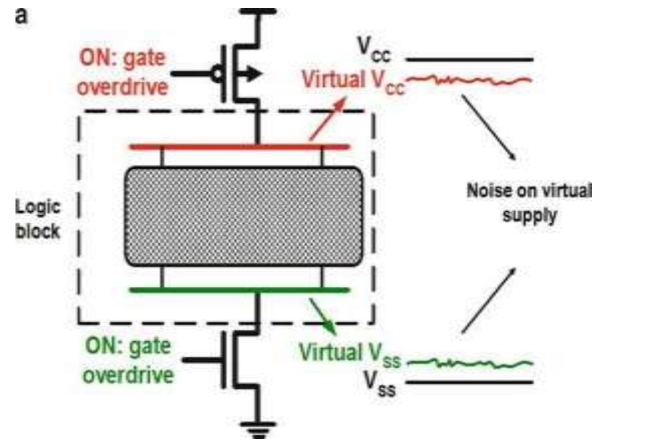

Fig.(a)

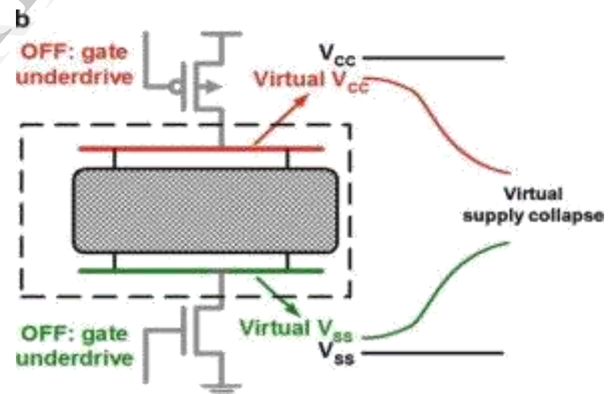

Fig.(b)

Fig.5 (a) Active mode: in the "on" state, the circuit sees a virtual Vcc and virtual Vss, which are very close to the actual Vcc, and Vss respectively. (b) Idle mode: in the "off" state, both the virtual Vcc and virtual Vss go to a floating state.

The biggest challenge in power gating is the size of the power gate transistor. The power gate size must be selected to handle the required amount of switching current at any given time. The gate must be big enough such that there is no measurable voltage (IR) drop due to it. Generally, we use 3X the switching capacitance for the gate size as a rule of thumb [2][4][8].

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1) Power-gating parameters

Power gating implementation has additional considerations than the normal timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

- *Power gate size:* The power gate size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. Generally we use 3X the switching capacitance for the gate size as a rule of thumb. Designers can also choose between header (P-MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analysis tools can accurately measure the switching current and also predict the size for the power gate.

- *Gate control slew rate:* In power gating, this is an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control signal.

- Simultaneous switching capacitance: This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

- Power gate leakage: Since power gates are made of active transistors, leakage is an important consideration to maximize power savings.

2) Comparison two power supply systems

Here we consider a standard chip (Fig 6 (a)) and a power-gated chip (Fig 6 (b)) both implementing the same functionality. But in the case of power gated chip excessive voltage drop (ΔV) across the sleep transistor. However, we increase the supply voltage, the dynamic and leakage power consumption may nullify the intended power savings [4][8].

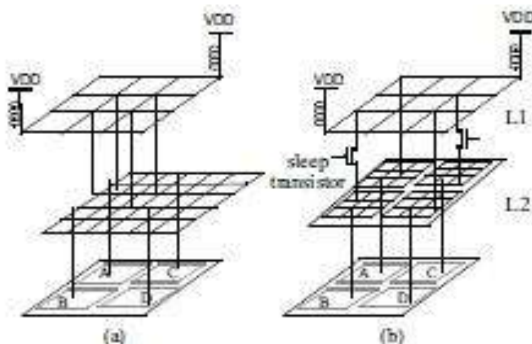

Fig.6 Power supply system (a) normal power supply system (b) power-gating system

In the standard chip, all logic circuits are connected to Vdd through a hierarchical power mesh. The entire chip is fully powered at all times. In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh. When a macro cell is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop. When sleep transistors are turned on and off, power supply currents are drawn in a short period of time, which may result in large voltage fluctuations on the power grid. This power gating noise (PGN) affects the reliability of systems- on-chips (SoCs), especially for advanced CMOS technologies having narrow noise margins. We need to add extra decoupling capacitance (decap) to reduce the gating noise and leakage currents associated with the intentionally introduced capacitors. At the same time, the switching sleep transistors consume more dynamic power. In a chip without power-gating, the non-switching part of the circuit serves as a decoupling capacitor and reduces the power grid noise. However, in the power-gated chip, the gated cells are disconnected from the power supply during idle state, which prevents them from acting as a decap for the active circuit. Thus the non-gated adjacent cell to the gated circuitry may need extra decap to guarantee that power grid noise remains within tolerable limit. Extra decap will enlarge the chip size and again consume more leakage power [8].

We will now consider the chip shown in Fig.6. Region I contains the gated macros B and C, whereas region II consists of ungated macros A and D. We qualitatively compare the leakage, dynamic power, decap and sleep transistor area of those two regions. We normalize the data to that of an ungated chip which realizes the same functionality as the gated chip. The trade-off in terms of power and area for power-gating systems can be summarized in table below [4][8].

Now we can notice that the benefit comes only from saving the leakage power of gated circuits, and the costs include: 1) area consumed by the extra decap and sleep transistors; 2) dynamic power of both regions and leakage consumption of non-gated circuit and decaps. In our study, we will attempt to quantify these benefits and costs [4][8].

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	Non-Power Gating Chip Region		Power Gating Chip Region	
	I	II	I	II
P(leakage)	1	1	↓	↑
P(dyn)	1	1	↑	↑
Area(decap)	1	1	1	↑
Area(st)	N/A	N/A	↑	N/A

Table 1: Power-gating vs. non-power gating

3) Advantages over Adaptive Biasing Technique

Leakage current comprises of different components and mechanisms, and thereby different approaches have been proposed to manage leakage current. Industries have preferred the use of multiple low power methodologies due to the limit of the exclusive use. For instance, power gating is widely accepted to reduce sub-threshold leakage current in idle state of a circuit. However, it gives only little leakage saving when software and input data make a circuit have idle periods shorter than the breakeven time of power gating, which means that there is no chance to cut off leakage current by power gating. Reverse body bias helps to reduce leakage current for the case while it reduces wide spread of leakage current due to process variation across the entire manufactured chips. However, the use of multiple low power methodologies requires large design and area overheads. Moreover, the mixed use can induce another leakage current path; hence it can give smaller improvement of leakage reduction compared to its cost increase [4][5][7]. This naturally calls for the reduction of adoption cost in each methodology without compromising the extent of leakage saving.

IV. CONCLUSION

Power considerations led to the replacement of bipolar logic by CMOS in the 1980s in spite of the former resulting in smaller and faster devices. Continuous advancements in CMOS technology enabled an exponential the scaling down of transistor area and scaling up of switching speed over the decades. Unfortunately, the power density increased prominently as a consequence. Leakage currents are expected to result in further increases in power density for technology nodes below 90 nm, which is becoming unsustainable with currently available solutions. This sets up the stage for investigation into aggressive power reduction techniques at every level of design abstraction [6].

Through this I have analyzed various fundamental device and circuit level techniques as well as power management techniques for low power CMOS technology. I discussed various sources of power consumption in a CMOS transistor. I studied the major components of power: dynamic, short-circuit, and leakage, followed by the basics of device and circuit level techniques to reduce these power components. A technique for power optimizations at higher levels is being developed due to design abstraction levels.

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