International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 02, February-2015

MVL ALU based on QSD Technique

Prajakta V. Deshmukh[1]
Dept. of Electronics and Telecommunication Engg
Savitribai Phule University of Pune
SITS, Narhe, Pune-41 Pune, India.

Mukesh D. Patil[2]
Dept. of Electronics and Telecommunication Engg
Savitribai Phule University of Pune
SITS, Narhe, Pune-41 Pune, India.

Abstract —Interconnects are the ruling contributor to delay, area and energy consumption in CMOS. Multiple-valued logic can reduce the average power and number of interconnections which reduces the overall energy consumption. In this paper, a QLUT (Quaternary Look-Up Table) structure is designed in supersede of binary LUT in FPGA. The circuit is congenial with standard CMOS processes, with one voltage supply and devoting voltage mode structures. A technique used to optimize the switches resistance and power consumption is called as clock boosting. A Quaternary Signed Digit (QSD) number system is used to perform carry free addition, borrow free subtraction and multiplication. A fast Arithmetic Logic Unit (ALU) based on radix 4 system, each improves the computational complexity. Arithmetic operations like addition, multiplication and subtraction in Modulo-4 arithmetic by using multi-valued logic (MVL).

Index Terms—Field Programmable Gate Array (FPGA), Quaternary Look-Up Table (QLUT), Multiple Valued-Logic (MVL), Standard CMOS technology, Quaternary Signed Digit (QSD).

I.INTRODUCTION

Field Programmable Gate Array (FPGA) has been steadily growing from years. They can be reprogrammed to implement any function, with any amount of parallelism. For million gates FPGA, 90% of area is consumed by interconnects [3]. As interconnects has become preponderant in digital systems, like delay, power and area [4].

In binary CMOS, static power consumption is closely related to leakage currents, and dynamic power consumption is given by

2 D D

$$PD \propto CV_{DD}^2 \qquad (1)$$

where C = Capacitance of the nodes driven.

V_{DD}= Power Supply Voltage. In CMOS process, contracting of transistors thus reduces C and devoting lower V_{DD}, hence saving power and implementing more functionality into the same area. C also includes routing capacitance related to logic gate wires, where power spent in routing may reach 70% of overall consumption [1]. Multiple-valued logic has been proposed as an alternative to binary logic. As binary logic is limited to only two states, true and false, multiple-valued logic (MVL) supersede these with nite or innite numbers of values [6]. Hence, more information can be carried in each wire, reducing the routing network. Reducing the routing will directly reduce the line capacitance and circuit area, which enables the increase in maximum operational frequency and reduction in power consumption. Therefore, the logic gates will come closer and reduce the average power required for level transitions. The new power consumption is

$$PD \propto CV_{DD}^2 V_{av} \qquad (2)$$

Vav = Average voltage between logic levels [1]. In order to deal with the static power dissipation problem using standard CMOS, maintaining the logic compaction permitted by MVL and presented with QLUT method. The use of MVL is to compact information as a one wire can carry more than two different signal levels. This show the way to reduction of interconnects cost, hence reducing area, power and delay [3].

Organization of paper is as follows: In Section II, gives a basic idea about QLUT and its methodologies and implementations. In Section III, the basic of QSD including the arithmetic logic unit concept. Section IV, concludes with result and discussion.

II. SYSTEM IMPLEMENTATION

QLUT has four logic levels and three reference voltages i.e. 1/6VDD, 3/6VDD, and 5/6VDD to decide quaternary value. Fig.1. shows Q-levels and reference voltages.

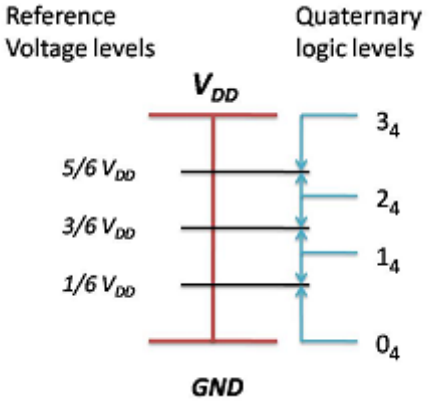

Fig. 1. Q-Logic and Reference Voltage

Quaternary variable can carry twice information than binary variable. The group of two binary variables comprises of one quaternary variable. A LUT is an operator which is array indexing based on configuration memory, where the output is depends on its input. Initially the configuration value is stored in LUT configuration memory, the logic value is assigned to the output according to the input. By programming the memory, the logic function can be implemented on LUT with the given number of input and outputs.

A quaternary function implemented by a QLUT is defined as g : Q_k = Q, over a set of quaternary input variables Y = (y_0, . . . , y_{k1}), where the values of a variable y and the function g(Y) are defined in Q = 0, 1, 2, 3. In general, if l is the number of logic levels, the total number of different functions |F| that can be implemented in a LUT is given by

$$| F |= l^{|n \times l^k|} \quad (3)$$

where n is the number of outputs and k is the number of inputs. For a LUT with a single output (n = 1), the number of different functions for binary (l = 2) and quaternary (l = 4) representations is given, respectively, by

$$| F_2 |= 2^{2^k} = 4^k \qquad | F |= 4^{4^k} = 256^k \quad (4) \quad (4)$$

With the same number of inputs and outputs, the number of possible functions that may be represented in a quaternary LUT is much larger than in a binary LUT. Therefore, reducing the total number of connections, MVL also leads to a reduction of the total number of gates[1]. Fig. 2. shows two inputs, 16 configuration (reconfigurable quaternary functions) inputs and one output QLUT. There are two main blocks in proposed QLUT: 1) 16-1 multiplexer using array of switches which

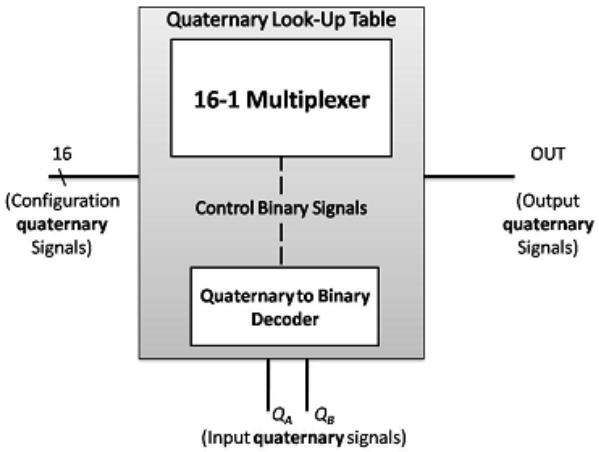

Fig. 2. Proposed QLUT

establishes a low resistance path between one configuration input and output according to the input. 2) Quaternary-tobinary Decoder which consist of a 2-bit ADC (Analog-toDigital converter) and combinational logic used to generate the control signals and given to the multiplexer. These blocks are described in following subsections.

A. 16-1 Multiplexer

Multiplexer path is made up of transmission gates (TGs) modeled by simple RC circuit. The charging time is proportional to the RC time constant, as the capacitance is constrained; the way to reduce the propagation delay is to reduce the switch resistance. Two methods are used to implement the multiplexer switches: 1. Use of CMOS TGs. 2. Use of single nMOS transistor controlled by the CB circuit. An approach for 2-input QLUT is to employ two series switches in multiplexer. To reduce resistance path and improving the QLUT speed, a single switch is used. This will slightly increase the complexity of decoder and CB circuit to control a single nMOS switch.

B. Clock Boosting Switch

In CB circuit, there are two phases. In phase 1, the capacitor (C) is charged to V_{DD}, and switch (nMOS) is open, as its gate is connected to ground. In phase 2, C is disconnected from V_{DD}, maintaining its charge, while its bottom plate is referred to V_{DD}. Hence, the switch gate voltage becomes 2 V_{DD}. In high-level model, the switches are replaced by TGs and depending upon the clock generator circuit is used to control its phases.

The proposed high-level model. In this, two switches are recognized as an inverter, reducing the number of elements and eliminating the 2-phase clock generator. To delay the signal, this inverter is used and at the same time implementing nonoverlapping clock which is used to control the other switches, the capacitor C is initially discharge and clk1= 1 (V_{DD} turns ON and connects node B to GND, while P1), N1turns OFF and a high impedance path takes place between node A and B. At the same time, P is ON and steadily charges the C (and node A) to V_{DD2}. When clk1= 0 (GND), N turns OFF, the inverter ties the lower capacitor plate to V_{DD} and P turns OFF, node A rises to 2 V_{DD} and P1is turned ON connecting node B to 2 V_{DD} as required. In practice, due to the charge redistribution with transistor Nsw gate capacitance, a small lower voltage is obtained. This small voltage will prevent the transistor for working under a gate voltage close to the maximum voltage (2.7V), avoiding early aging effect on this large transistor. To avoid its compromise towards its long term use, an nMOS in series with Nis used, avoiding the drain-source voltage to be higher than V_{DD} 1, in each transistor. A full charge of this capacitor only once at powering up, from then the capacitor gets discharge due to the charge distribution with switch gate capacitance, it should be noted.

C. Q-B Decoder

The 2-bit quaternary to binary decoder makes the use of a single row of switches to drive the input configuration signal to the output. For this, 16-control signals are generated which is applied in the clk input of each switch. These switches are used to connect single configuration input to its output. The quaternary variables are decoded into binary, to generate the control signals, making the use of binary logic gates.

III. QUATERNARY SIGNED DIGIT

In binary number system, carry may propagate through least significant digit to most significant digit. Hence the addition time is depended on word length.

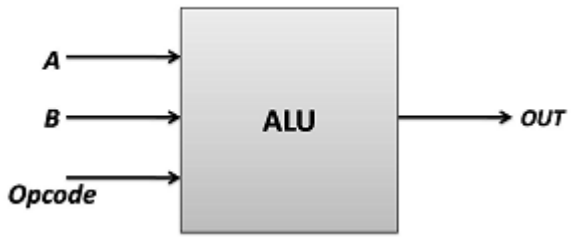

Fig. 3. MVL ALU based on QSD

In this paper, a high speed QSD ALU is anticipated which is capable of carry free addition, borrow free subtraction and multiplication. For QSD operation, first convert binary or any other input into quaternary signed digit.

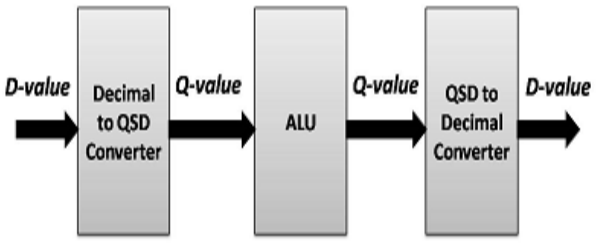

Fig. 4. Conversion of QSD

In this paper, only the positive side of QSD is taken and negative computations are taken using this positive side. So, the computational range is reduced from -3, -2, -1, 0, 1, 2, 3 to 0, 1, 2,

3 only. This gives 42% improvement in computation complexity and thus increases its efficiency. For example, the original range is of 7 symbols which are reduced to 4 symbols. Thus the computational complexity is

$$(7 - 4) * (100 / 7) \% = 3 * (100 / 7) \% = 42\%$$

If the decimal value are AD = 35 and BD= 28 which are given to the Decimal to QSD converter, as shown in fig. 4.

```
4 | 35 → 3        4 | 28 → 0
4 |  8 → 0        4 |  7 → 3
4 |  2 → 2        4 |  1 → 1
  |  0              |  0
```

Therefore, AQ = 0 2 0 3 and BQ = 0 1 3 0 then this is given to ALU which will be given to ALU which will perform Addition/Subtraction/Multiplication. If addition is to be done then the two numbers gives 0 3 3 3, then it will again convert QSD into decimal.

$$0 * (4^3) + 3 * (4^2) + 3 * (4^1) + 3 * (4^0)$$
$$= 48 + 12 + 3$$
$$= 63$$

Thus we get a decimal value at the output of Q-D converter.

IV. RESULTS AND DISCUSSION

In this paper, an innovative QLUT design is used for multiple valued combinational logic or as a building block in FPGAs. The QLUT internal functionality is implemented using simple standard CMOS structures. This feature is achieved through a quaternary-to-binary decoder that quantizes the input signals. This decoder is based on voltage mode self-referenced comparators that allow the use of a standard CMOS technology. CB technique was used to decrease the switches resistance and increase the operation frequency, while at the same time, achieving low power consumption. The QSD ALU is better than binary in terms of number of gates used and efficiency will increase with the operation speed.

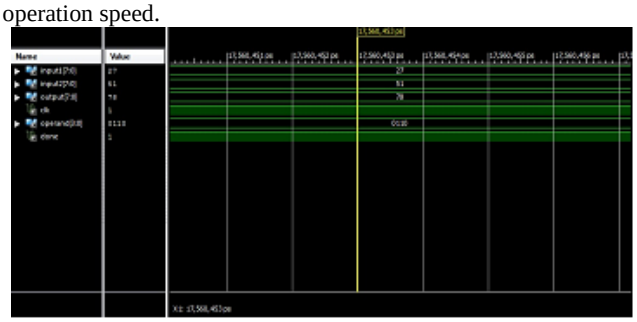

Fig. 5. Addition in QSD

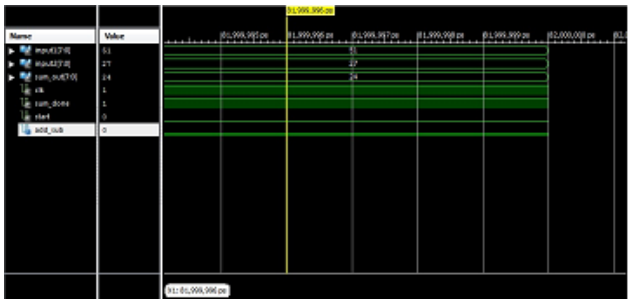

Fig. 6. Subtraction in QSD

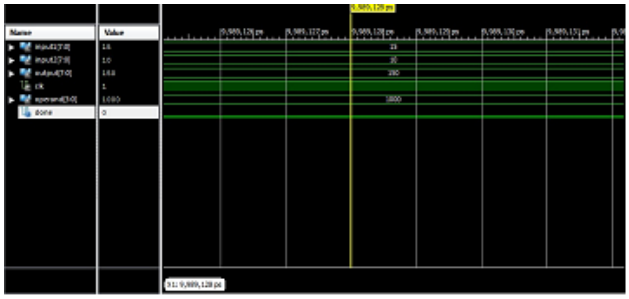

Fig. 7. Multiplication in QSD

QSD consume 25% less space than BSD to store number. Therefore, the design is a solution to reduce the interconnections impact, without increasing power consumption or losing performance and higher number of gates can be tolerated.

REFERENCES

1. Diogo Brito and Taimur G. Rabuske, Student Member, IEEE, Jorge R. Fernandes, Paulo Flores and Jos Monteiro, Senior Member, IEEE, ”Quaternary Logic Lookup Table in Standard CMOS” IEEE Transactions On Very Large Scale Integration (VLSI) Systems, February 3, 2014.
2. R.C.G. da Silva, C. Lazzari, H. Boudinov, L. Carro, ”CMOS voltage mode quaternary look-up tables for multi-valued FPGAs”, Universidade Federal do Rio Grande do Sul, Brazil, Microelectronics Journal, Received 2 April 20 09 Received in revised form 15 July 20 09 Accepted 21 July 20 09, Available online 12 August 2009
3. Cristiano Lazzari and Paulo Flores and Jose Carlos Monteiro, ”Power and Delay Comparison of Binary and Quaternary Arithmetic Circuits”, International Conference on Signals, Circuits and Systems (SCS), pages 1-6, November 6-8, 2009
4. Vasundara Patel K S, K S Gurumurthy, ”Arithmatic Operations in Multivalued Logic”, International Journal of VLSI design & Communication Systems (VLSICS), Vol. 1, No. 1, March 2010.
5. Cristiano Lazzari, Paulo Flores, Jos e Monteiro, Luigi Carro, ”A New Quaternary FPGA Based on a Voltage-mode Multi-valued Circuit”, 9783-9810801-6-2/DATE10 2010 EDAA
6. Vasundara Patel K S, K S Gurumurthy, ”Design of High Performance Quaternary Adders”, International Journal of Computer Theory and Engineering, Vol.2, No.6, December, 2010 1793-8201
7. Diogo Brito, Jorge Fernandes, Paulo Flores, Jos e Monteiro INESCID / Instituto Superior T ecnico - TU Lisbon, Portugal, ”Design and Characterization of a QLUT in a Standard CMOS Process”, 978-1-46731260-8/12/$31.00 2012 IEEE
8. Ankita. N. Sakhare, M. L. Keote, ”Application of Galois Field in VLSI Using Multi-Valued Logic”, International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 1, January 2013, ISSN: 2319-5967, ISO 9001:2008 Certified.
9. Diogo Brito, Jorge Fernandes, Paulo Flores, Jose Monteiro, ”Standard CMOS Voltage-mode QLUT Using a Clock Boosting Technique”, INESC-ID / Instituto Superior Tecnico - TU Lisbon, Portugal, 978-14799-0620-8/13/$31.00 2013 IEEE.
10. Prashant Y. Shende, R. V. Kshirsagar,“Quaternary Arithmetic Logic Unit Design Using VHDL”, International Journal of Science and Research (IJSR), India, Online ISSN: 2319-7064, vol 2, issue 7, July 2013.