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Multiple Valued and Pass Transistor Logic Based 2 To 4 Decoders using MOS Like GNRFET

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***Abstract*— Additionally, this thesis uses GNRFET technology for line decoders 2 to 4, and 4 to 16 mode in addition to the fundamental transmission gate logic (FTG), the pass transistor dual-value logic, and the base CMOS logic. Constant and flexible 15T (high performance) designs (low power benefit) as well as constant and flexible 14T (low power) designs are analyzed and assessed. Graphene Nano Ribbon Field Effect Transistor, also known as GNRFET, is a viable alternative to bulk MOSFETs because of its superior performance compared to bulk MOSFETs.**

GNRFET's small channel has been demonstrated to have less impact, and the decoders' performances are on par with those of their MOSFET counterparts. Using 32nm as the number of technology nodes in the design results in power loss and unnecessary switching in the circuit. In general, the circuit performs better with smaller delays, larger amounts of power, power dissipation, and delay, and the same amount of power dissipation.

Keywords: GNRFET, 32nm, Decoder, Mixed Logic, TGL, DVL

I. INTRODUCTION

When a large number of transistor-based circuits are combined onto a single chip, this technique is known as "Large Scale Integration." To put it simply, the microchip is a VLSI device. Nowadays, the VLSI model is employed in the fabrication of all of the semiconductors. Current technology has moved from huge transistors on a chip to the production of a microchip with a large number of gates and billions of small transistors.

Because of this change in thinking, it may be used in areas such as superior registering and communication frameworks, nonpartisan systems, wafer-scale mix, microelectronic frameworks, and creative work. These chip-driven gadgets are thus in high demand now and into the future. The size, power, and effectiveness of the system must be decreased to fulfill these constraints. As a consequence, the design of both simple and sophisticated circuits has grown more concerned with dispersing power.

The lack of short out current in prior strategies for expanding the area of a fan-out tree has been proven to result in excessive power consumption. For example, the absolute dynamic mode power utilisation of the combinational circuits is lowered by up to 55 percent, 29 percent, and 53 percent when compared to circuits built in CMOS or GNRFET technology while preserving equivalent information security and speed. The overwhelming majority of logic gates in integrated circuits are static CMOS circuits. You can get great performance, noise reduction, device variety, and correlated nMOS/pMOS pull down/pull up with these systems. A dependable operation can be accomplished at low voltages and tiny transistor sizes thanks to CMOS logic's power versus voltage scaling and transistor estimation. Transistor gates are the sole links between information streams, reducing plan uncertainty and allowing for cell-based logic to be mixed and organised more freely. Many structural kinds were suggested in the 1990s as an alternative to CMOS logic in order to improve speed, power, and zone. Pass-transistor logic was one of them. Because of the fundamentally different layout, the inputs are connected to both the transistor gates and the source/drain dispersion terminals.

Pass transistor circuits are implemented using nMOS/pMOS pass transistors or transmission gates, which are parallel sets of nMOS and pMOS. A mixed-logic plan technique for line decoders is developed in this work, which combines several logic gates into a single circuit in order to obtain greater performance than single-style designs. [Eight] There are a variety of applications for line decoders, including memory displays, multiplexing systems, and the use of Boolean logic abilities. Only a tiny percentage of the writing time is devoted to simplifying them, with some steady improvement. A "normal decoder" is a non-inverting decoder, although

II. IMPLEMENTATION

The circuits were created using the HSPICE software programme, which used a library from the GNRFET Spice model (see link below). https://nanohub.org/resources/17074 In the 22nm model, the model file is utilized. Table 1 lists a few of the criteria that were taken into account to enhance the results and circuit performance.

TABLE I. GNRFET PARAMETER

Parameter	Value
Length of Channel	22nm
nRib	1
n	6
Tox	0.95nm
sp	2nm
dop	0.001
p	0

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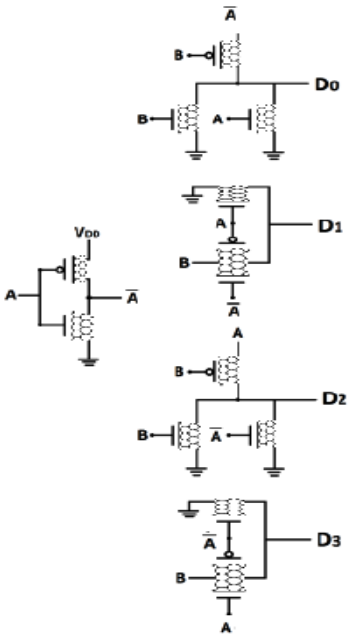

Fig. 1. GNRFET 14T Decoder proposed

Figure 1 depicts a 2 to 4 decoder fabricated in 22nm utilising GNRFET Technology in the MOS Like GNRFET Mode. Among the most essential characteristics in logic circuit design are Tox, which stands for dielectric thickness, sp, which stands for spacing between GNRs, p, which stands for edge roughness, and nrib, which stands for ribbon count. The GNRFET-based inverted type 14T decoder is seen in Fig. 2 as well.

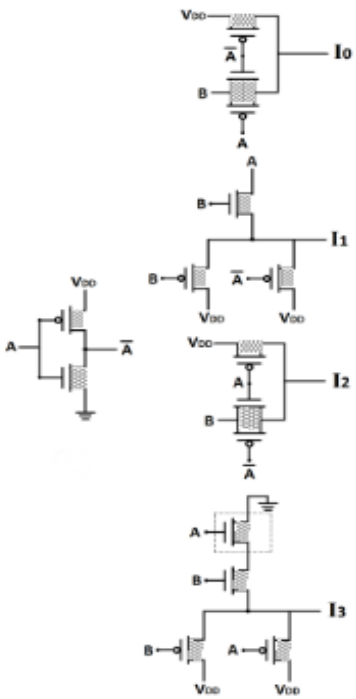

Fig. 2. Inverted 14T 2 to 4 decoder using GNRFET

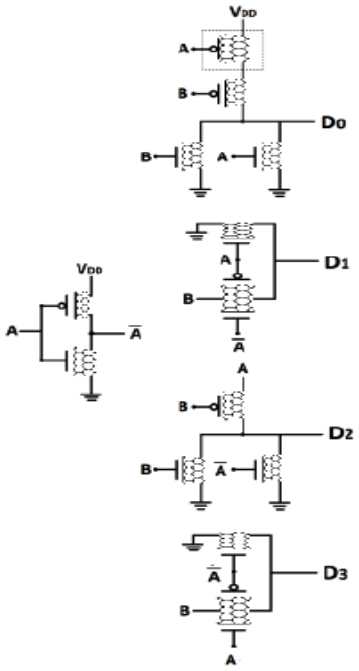

Fig. 3. GNRFET 15T Decoder proposed

In Fig. 3, a two-input 2 to 4-decoder using GNRFET Technology in 22nm is shown in MOS like GNRFET Mode, and in Fig. 4, it is shown in inverting mode. This figure depicts the 15 T, in which the DO portion is mostly implemented in CMOS logic and the remainder in DVL/TGL mixed valued logics.

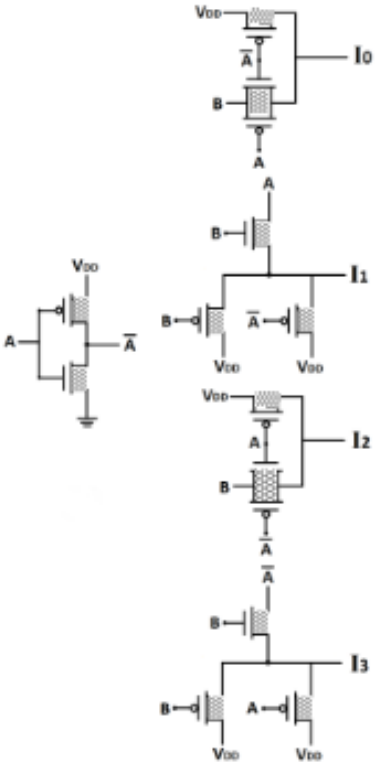

Fig. 4. GNRFET 15T inverted Decoder proposed

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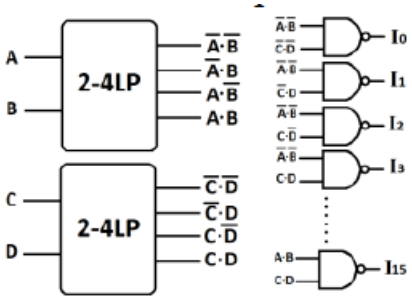

Fig. 5. GNRFET Proposed 4 to 16 inverting decoder (14T)

On the basis of the 14T standard, a proposed 4 to 16 inverting decoder using GNRFET technology is shown in Figure 5. The short gate decoders in 14t and 15t mode are then utilised to construct an inverted 4 to 16 decoder based on GNRFETs, as seen in Figs. 3 and 4. The NAND gates are employed in cmos logic for GNRFETs, as illustrated in Figs. 3 and 4. In order to acquire the 16 outputs I0 to I16, the following steps must be taken. Fig. 6 depicts a non-inverting circuit architecture in which NOR gates are also used in conjunction with a GNRFET device.

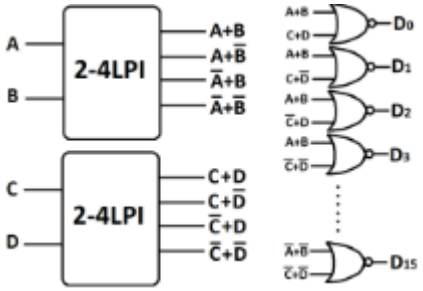

Fig. 6. GNRFET Proposed 4 to 16 normal (14T)

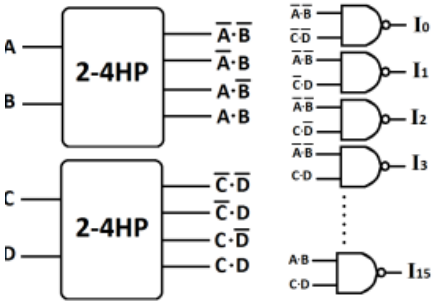

Fig. 7. Proposed 4 to 16 decoder based on GNRFET (15T)

Figure 7 depicts a proposed 4 to 16 decoder based on GNRFET Technology operating in High Performance mode; the operation is identical to that of the MOSFET counterpart previously addressed. Figure 8 depicts a non-inverting or normal decoder for the 15T signal.

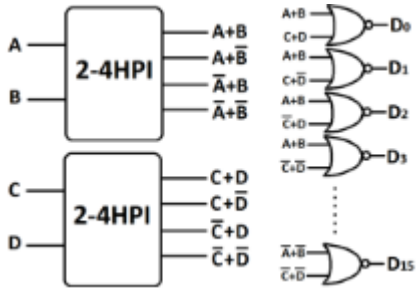

Fig. 8. GNRFET Proposed 4 to 16 normal (15T)

III. RESULT

The results of the simulation are reported in this section. When GNRFET-based circuits are compared to MOS-based decoders, the improvement in practically all parameters for GNRFET-based circuits is displayed in tabular form in Table 4.2. According to Table 1, the performance characteristics of MOSFET-based 2 to 4 normal decoders and the proposed GNRFET-based 2 to 4 normal decoders are compared. Average power, delay, power delay product, and power dissipation are all measured.

TABLE II. SIMULATION RESULTS TABLE FOR 2 TO 4 DECODERS AND 4 TO 16 INVERTED DECODERS

Normal Decoder	14T MOSFET Decoder 2to4	14T GNRFET Decoder 2to4 Proposed	15T MOSFET Decoder 2to4	15T GNRFET Decoder 2to4 Proposed
Average Power(w)	6.58E-08	2.46E-10	7.27E-08	2.79E-10
Delay(s)	8.23E-08	8.21E-08	8.22E-08	8.21E-08
PDP(J)	5.41E-15	2.02E-17	5.98E-15	2.29E-17
Power Dissipation(w)	2.12E-08	2.27E-11	2.12E-08	3.22E-11
Inverted	14T MOSFET Decoder 4to16	14T GNRFET Decoder 4to16 Proposed	15T MOSFET Decoder 4to16	15T GNRFET Decoder 4to16 Proposed
Average Power(w)	3.24E-07	1.45E-09	3.70E-07	1.50E-09
Delay(s)	8.17E-08	8.18E-08	8.17E-08	8.18E-08
PDP(J)	2.65E-14	1.19E-16	3.02E-14	1.23E-16
Power Dissipation(w)	9.30E-08	3.33E-10	9.30E-08	3.52E-10

Table 2, on the other hand, displays outcomes based on performance measures. The average power, delay, PDP, and power dissipation of the remaining circuits are shown in the table below

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TABLE III. RESULTS FOR 2 TO 4 INVERTED DECODERS AND 4 TO 16 NON INVERTED DECODERS

Inverted	14T MOSFET Decoder 2to4	14T GNRFET Decoder 2to4 Proposed	15T MOSFET Decoder 2to4	15T GNRFET Decoder 2to4 Proposed
Average Power(w)	1.47E-07	1.47E-08	1.78E-07	1.54E-08
Delay(s)	2.00E-08	2.00E-08	2.00E-08	2.00E-08
PDP(J)	2.95E-15	2.95E-16	3.57E-15	3.09E-16
Power Dissipation(w)	5.24E-08	5.09E-11	5.25E-08	4.98E-11
Normal Decoder	14T MOSFET Decoder 4to16	14T GNRFET Decoder 4to16 Proposed	15T MOSFET Decoder 4to16	15T GNRFET Decoder 4to16 Proposed
Average Power(w)	1.30E-05	2.54E-06	1.30E-05	2.55E-06
Delay(s)	3.02E-08	3.00E-08	3.04E-08	3.00E-08
PDP(J)	3.92E-13	7.61E-14	3.96E-13	7.63E-14
Power Dissipation(w)	1.57E-07	1.72E-10	1.57E-07	1.70E-10

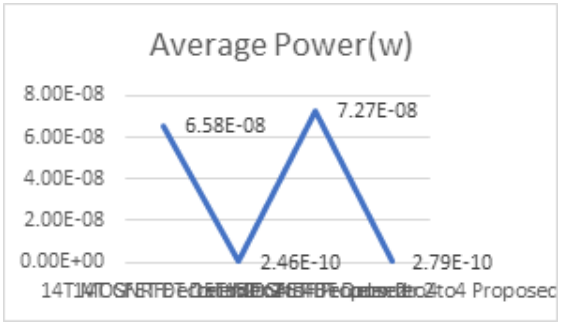

Fig. 9. Average Power Comparison with propose GNRFET Decoder

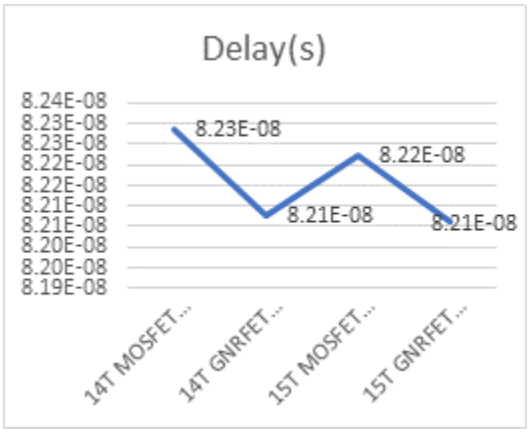

Fig. 10. Delay Comparison with proposed GNRFET based Decoder

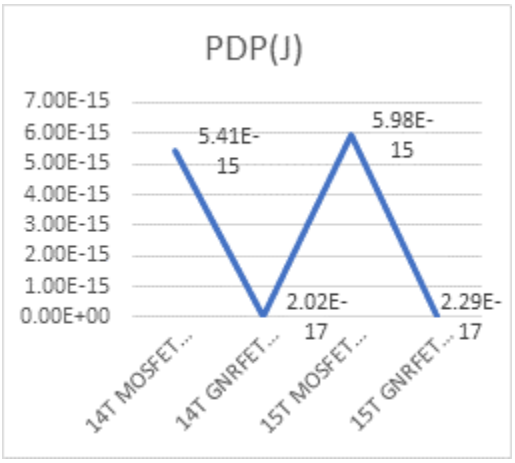

Fig. 11. PDP with proposed GNRFET based Decoder 2 to 4 mode

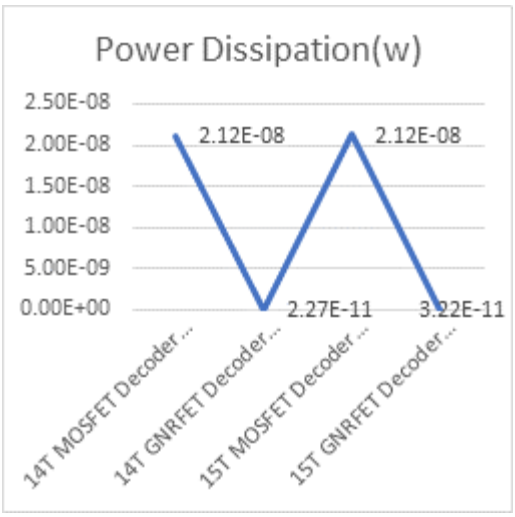

Fig. 12. Power Dissipation with proposed GNRFET based Decoder

The performance metrics findings for the decoder in 2 to 4 mode in non-inverting mode are shown in Fig. 9 to Fig. 12, respectively. It demonstrates that the parameters have been improved while maintaining about the same latency, extremely low power, and PDP.

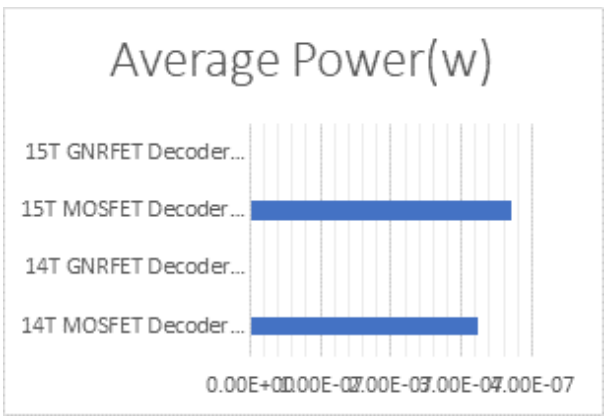

Fig. 13. Average Power Comparison with proposed GNRFET based Decoder

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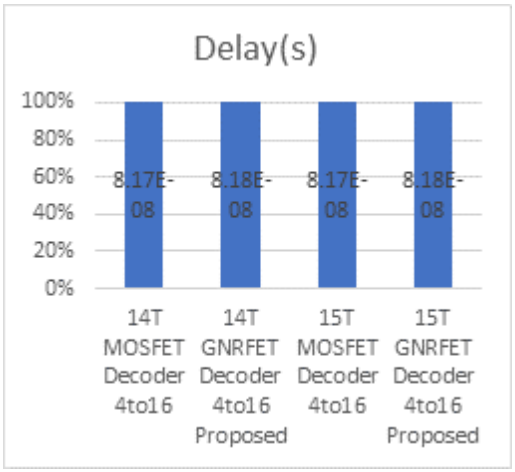

Fig. 14. Delay Comparison with proposed GNRFET based Decoder

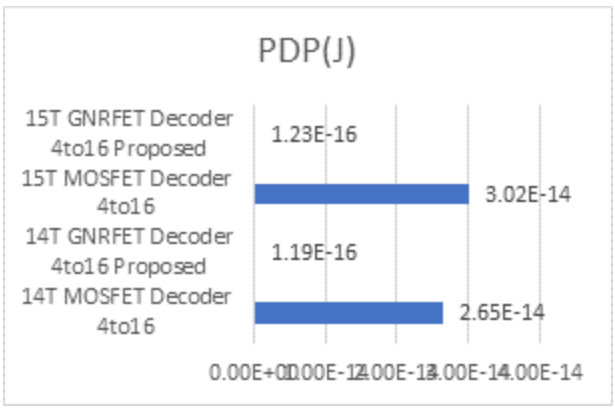

Fig. 15. PDP Comparison with proposed GNRFET based Decoder

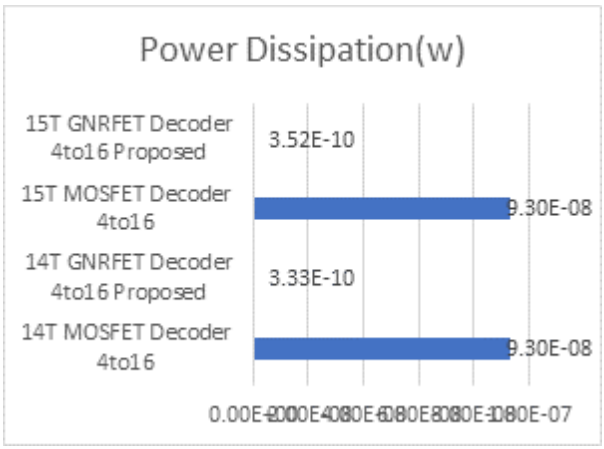

Fig. 16. Power Dissipation Comparison with proposed GNRFET based Decoder

The performance metrics findings for the decoder in 4 to 16 mode in inverting mode are shown in Fig. 13 to Fig. 16, respectively. It demonstrates that the parameters are improved with extremely low power dissipation and PDP, but that the latency is prolonged.

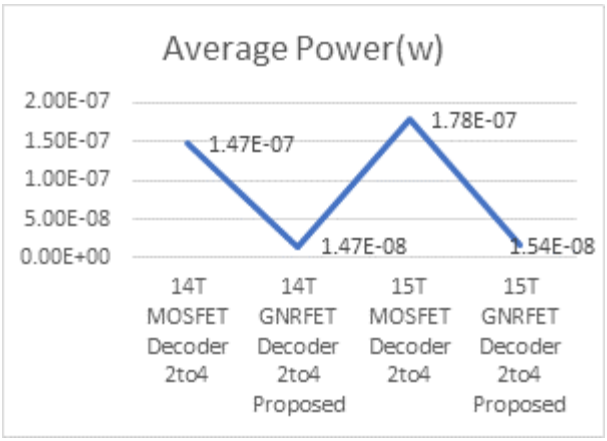

Fig. 17. Average Power Comparison with proposed GNRFET based Decoder

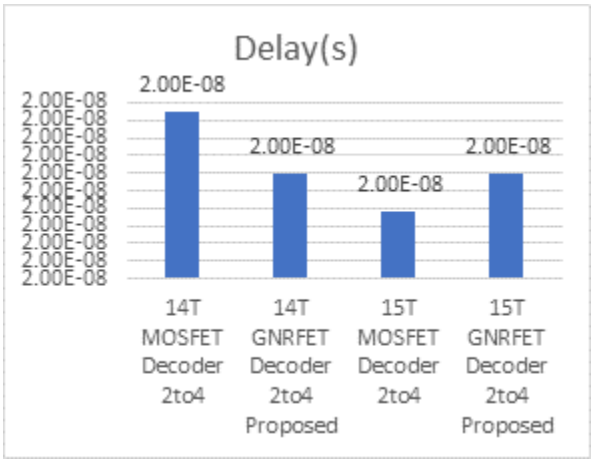

Fig. 18. Delay Comparison with proposed GNRFET based Decoder

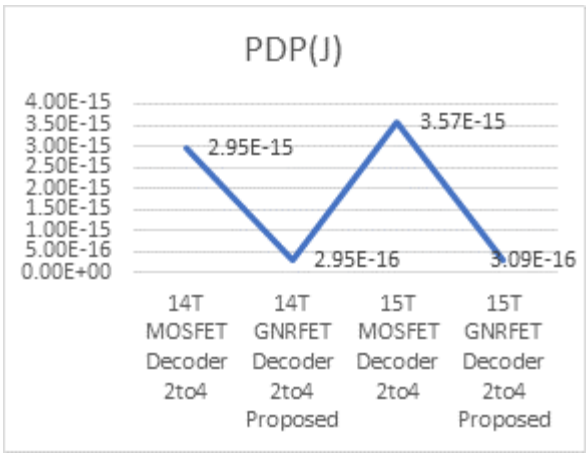

Fig. 19. PDP Comparison with proposed GNRFET based Decoder 2 to 4 inverting mode

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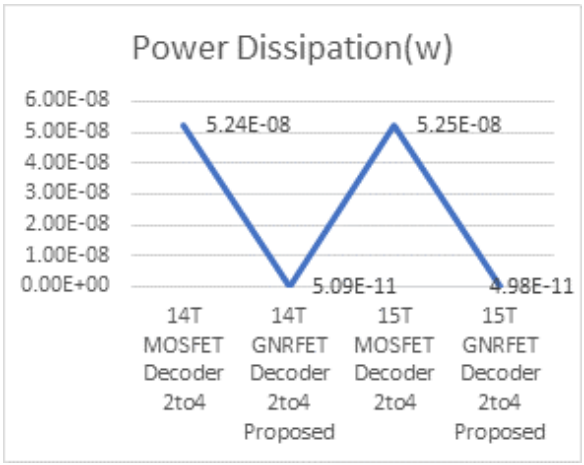

Fig. 20. Power Dissipation Comparison with proposed GNRFET based Decoder 2 to 4 inverting mode

The performance metrics findings for the decoder in 2 to 4 mode in inverting mode are shown in Fig. 17 to Fig. 20, respectively. Although the parameters are improved because to the low power dissipation and PDP, the latency is increased, and the delay is essentially same in both cases.

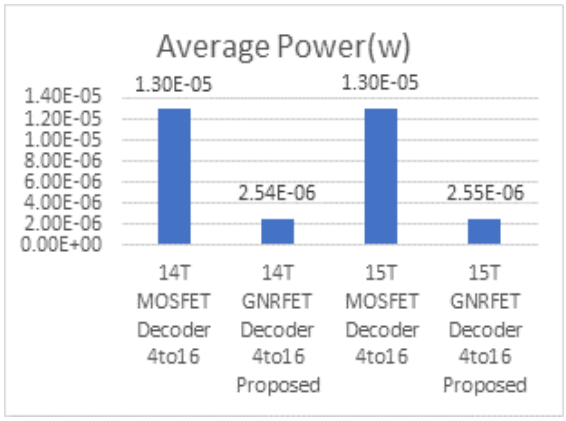

Fig. 21. Average Power Comparison with proposed GNRFET based Decoder 4 to 16 non inverting mode

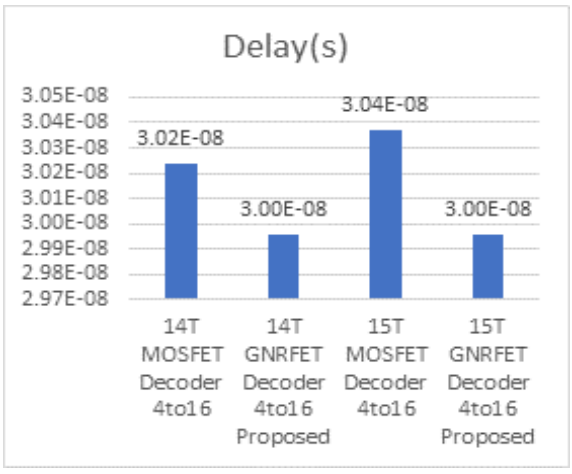

Fig. 22. Delay Comparison with proposed GNRFET based Decoder 4 to 16 non inverting mode

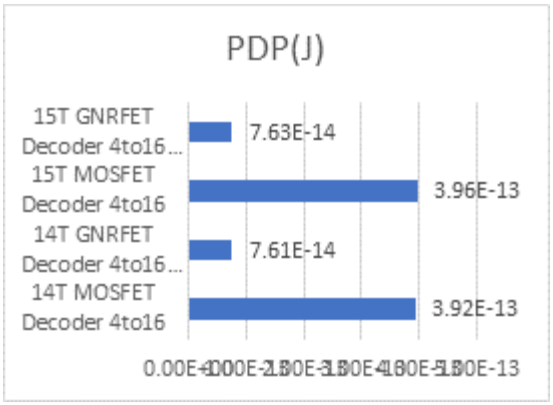

Fig. 23. PDP Comparison with proposed GNRFET based Decoder 4 to 16 non inverting mode

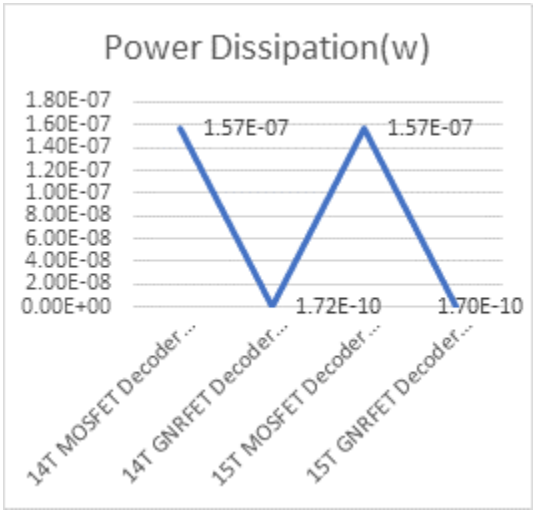

Fig. 24. Power Dissipation Comparison with proposed GNRFET based Decoder 4 to 16 non inverting mode

The performance metrics findings for the decoder in 4 to 16 mode in non-inverting mode are shown in Fig. 21 to Fig. 24, respectively. Although the parameters are improved because to the low power dissipation and PDP, the latency is increased, and the delay is essentially same in both cases.

IV. CONCLUSION

The aims of this thesis are met by providing a decoder with GNRFET that has better average power and latency over the previous decoders. In addition, the power dissipation is improved by using GNRFETs instead of MOS transistors. When employing MOS devices like as GNRFETs at 22nm, the short channel effects are decreased. Because of the ribbon shape of GNRFETs, they promise to be superior low-power devices and,

As a result, a great alternative for the traditional MOSFET in shorter technological lengths, notably beyond 22nm. When compared to its MOS equivalents in decoders, the average power circuit is improved by 93.9 percent, propagation latency is improved by 92.5 percent, and power dissipation is approximately the same but improved by 99.9 percent

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