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Multiple Comparative analysis of Reversible Gates for Designing Logic Circuits

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Abstract **- The Reversible Logic maps unique input to the output and ensure one to one mapping. This logic is used in emerging applications like low-power design, quantum computation, optical computing, bioinformatics and nanotechnologies. In communication between devices, the design of Parallel to Serial Converter plays an essential role as data bits in encoded form are transmitted serially rather than in parallel. This work understands and nurtures the necessity of reversible logic for future revolutionary computing and communication technologies. Among the reversible gates designed, Fredkin Gate is considered to be the universal gate which has a quantum cost of 5 and garbage outputs of 6. This work aims at reducing the quantum cost by using DRG4 Gates whose quantum cost is 4 and garbage outputs are 2. Using these reversible logic, the parallel to serial converter is designed to operate at 50MHz. The designs are coded in VHDL using structural modelling. These are synthesized and simulated in Xilinx ISE Design Suite 14.5. The results are compared for various parameters and the proposed design is found to be a better choice of implementing the parallel to serial converter practically due to less quantum cost, area, power dissipation, garbage outputs, etc.**

1.1 INTRODUCTION:

The Reversible logic is an attractive alternative for Boolean algebra based computations due to its lower power dissipation. As the basic computations are irreversible in nature by the use of silicon based semiconductor technology which is due to the mismatch of number of inputs and outputs; Reversible logic circuit maps unique input to the output and ensure one to one mapping. Also they have a unique feature of recovering the input from the outputs. The ever growing demand of high end computing applications has posed the challenge of continuous technology up gradation. The up gradation in technology has enabled the complex applications like Cloud computing, Real-time transitions on huge databases, Biotechnological computations a reality. Technological advancements in terms of higher operational frequency and miniaturization of chip in recent years have generated sufficient computing power to enable this growth. As predicted by Gordon Moore in 1960, popularly known as Moore's law, the transistor count in a chip will be double every one and half year on the average. Transistor growth is shown by Gordon Moore in figure 1. ITRS (International Technology Roadmap for Semiconductors) has also drawn a road-map of required feature size in future at atomic level in 2050. Shrinking in feature size resulted in a number of implementation and operational difficulties like heat dissipation, requirement of very thin laser beam, clock distribution etc.

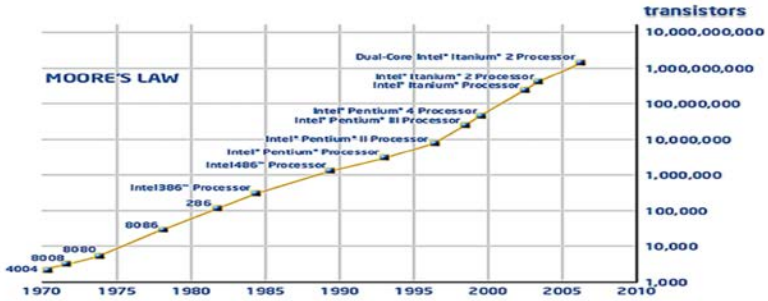

Figure 1: Moore Law's Graph for Transistors

Current technologies are finding it difficult to continue with the required level of growth. Alternative technologies are emerging to take place so that the growth momentum can be continued. Reversible computing is one of the computing system in which new generation computing system can be designed. Because of its basic nature of reversibility, it retains the old information and reduces dissipation of heat in its operation. This promise makes the technology as one of the possible alternative for future.

1.2 Limitations of Conventional Computing

Conventional technology has dominated the computing world for more than last three decades. Right from the basic gates like AND, OR, NOT, EXOR, NAND etc. multimillion gates circuits have become available as per the need of the applications. The great deal of success has come from the fact that CAD tools, and VLSI technology for miniaturization have enabled the developments of large number of circuits. As a result complete process of conceptualizations till productions of chip has been well established and developing combinational and sequential

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circuits with fault tolerance capability have become easier. The conventional computations by its nature are irreversible. The input cannot be reconstructed from its output. All the input lines do not propagate till output, resulting bit reversal or disappearance before output. This bit reversible causes a number of problems in high speed computations. That limits the viability of conventional computing for next generations. Important resources which are involved in computing are Time, Space, Manufacturing cost and Energy. With growing demand of computational speed in scientific applications, it has been observed that irreversible behaviour of classical gates may not be a technology rather it will lead to a number of problems. The Problems, which may arise in conventional computing system, can be classified in following types.

1. Physical problems
2. Computational problems
3. Economic problems

1.3 Literature Survey

Reversible computing is emerging as a potential development platform to replace conventional logic. This chapter represents previous work on reversible logic. We categorize our survey in the following categories.

- ✓ Reversible logic gates
- ✓ Circuit formats
- ✓ Reversible circuit design
- ✓ Parameters for Evaluation

1.4 Reversible Logic Gates

Right from the stored program architecture given by John Von Neumann in 1949, heat dissipation per computation of bit is being estimated. R. Landauer [1961] pointed out that the irreversible erasure of a bit of information consumes power and dissipates heat. While reversible designs avoid this aspect of power dissipation. Destruction of bits causes heat dissipation as per Landauer Principle. Bannett in 1973 proposed a Turing machine for loss-less computation by making it reversible. The development of reversible gates and circuits started after Toffoli proposed reversible logic gates in 1977. A number of gates have been proposed thereafter. The same has been described two categories namely basic gates and generalized gates.

Two constraints for reversible logic synthesis are:

(1) Feedback is not allowed

(2) Fan-out is not allowed (i.e., fan-out = 1).

A gate with k inputs and k outputs is called a k*k gate. Several reversible gates have been proposed over the last decades.

1.5 Design of Parallel to Serial Converter

1.5.1 Parallel to Serial Converter: With the advancement of technology, there has been more and more need for the gigabit rate link for storage application, data communication, computer networks and etc. To meet with the high processing multi-gigabit speeds and system performance, it becomes necessary to have prompt and efficient high-speed inter-connects. Traditional parallel link has been used in circuits for a long time, which let the data be sent over multiple channels simultaneously. But as the data rates gets higher and higher shown in the figure below, the parallel links can't keep up with the system performance due to cross-coupling noise and data skew especially in long distance transmission.

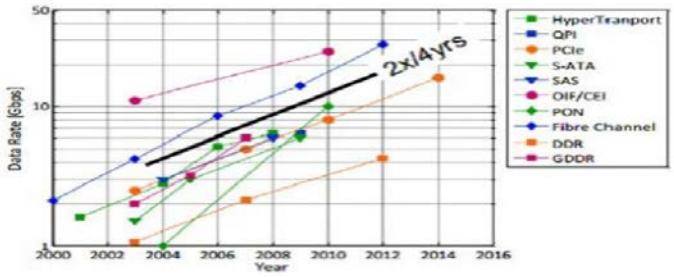

Figure 2: I/O Signalling Data Rate Trends

While serial communication has lots of advantages over the parallel links. In serial communication, the data is sent over a single channel sequentially. Because of that, there is no crosstalk noise, Furthermore, due to more interconnects, wires and ports are employed in parallel links, much more area, dynamic power and leakage power will be required. Therefore, there arises a need for SERDES. As the name suggests, is a serial transceiver that converts parallel data to serial data on the Transmitter side and serial data back to parallel data on the receiver side. A Serializer and Deserializer are to be designed to work with the SERDES in the research group to achieve the goal of high-speed serial data transmission with signal integrity.

Although data are processed in parallel in parallel in many digital systems to achieve faster processing speeds. When it comes to transmitting the data relatively long distances, this is done serially. The parallel arrangement in this case is highly undesirable as it would require a large number of transmission lines. Multiplexers can possibly be used for parallel to serial conversion.

1.5.2 Basic Design of Parallel to Serial Converter

A group of bits appearing simultaneously on parallel lines is called parallel data. A group of bits appearing on a single line in a time sequence is called serial data. The parallel to serial conversion is normally accomplished by the use of a counter to provide a binary sequence for the data select inputs of a multiplexer or by using a timer as shown in figure 3.2.

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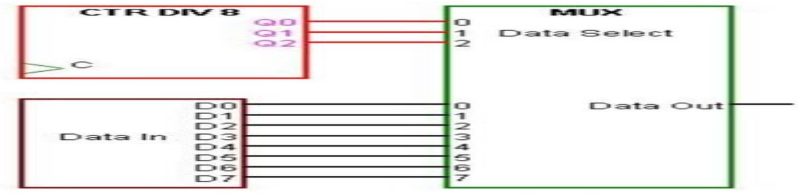

Figure 3: Parallel to Serial Data Converter

The design of internal circuit is shown in figure 3.3 for a 8-bit data transfer. This includes design of a counter whose binary output is connected to the select lines and the multiplexer is designed in terms of 2x1 multiplexers.

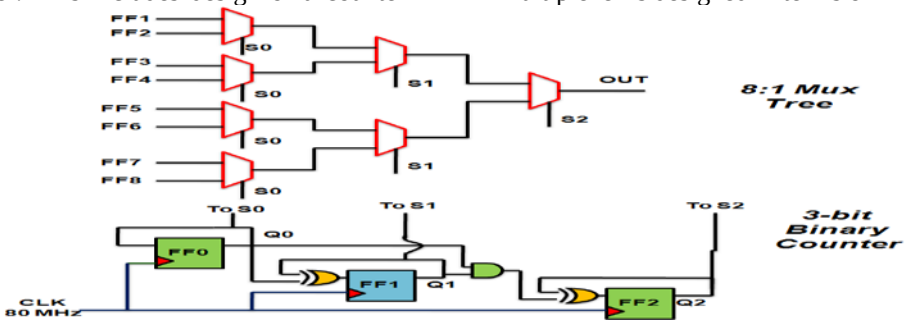

Figure 4: Internal Circuit of Parallel to Serial Converter

The figure 4 shows the arrangement of an 8 to 1 multiplexer used to convert eight bit parallel binary data to serial form. A three bit counter controls the selection inputs. As the counter goes through 000 to 111, the multiplexer output goes through I0 to I7. The conversion process takes a total of eight clock cycles. Then the counter recycles back to 0 and converts another parallel byte sequentially again by the same process.

1.5.3 Reversible Logic based Parallel to Serial Converter Design

The three bit counter is constructed with the help of three toggle flip-flops. A variety of counter circuits of various types of complexities are viable in IC form. The design of Reversible T-Latch is carried out the combination of Peres Gate and Feynman Gate as shown in figure 5.

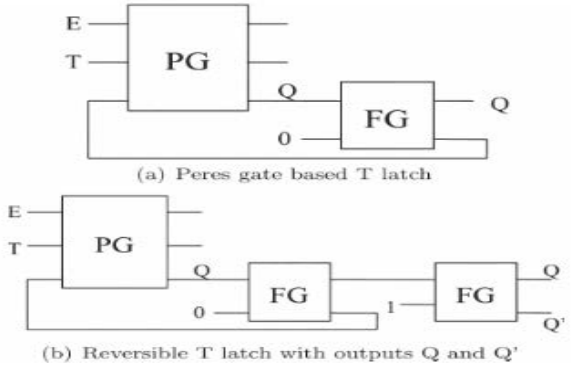

Figure 5: Design of Reversible T-Latch

The Existing Design of 4x1 multiplexer is considered as MUXLE as shown in figure 5. It acts as a logic element of the FPGA Configurable logic block. But this occupies more area than Fredkin Gate.

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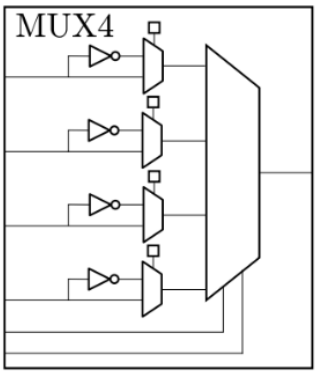

Figure 6: MUXLE Logic Element as 4x1 Multiplexer

The higher order design of 32-bit Parallel to Serial Bit conversion is performed in this work by using fredkin gate. The 32-bit multiplexer is designed as shown in figure 6.

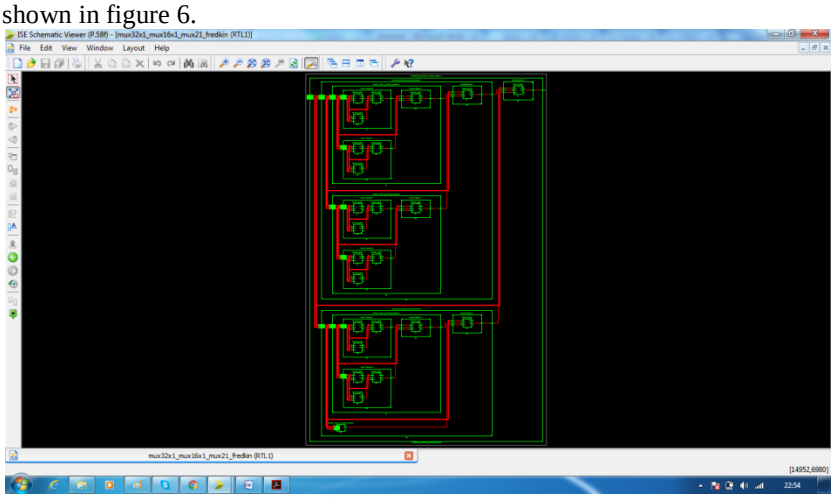

Figure 7: Design of 32-Bit Multiplexer using Fredkin Gate

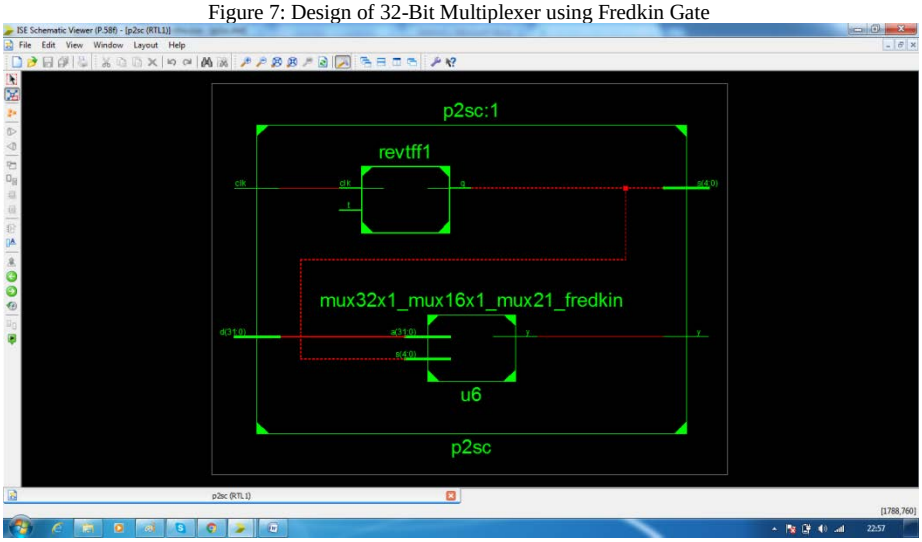

Figure 8: Design of Parallel to Serial Converter using Reversible T-Latches and Fredkin Gate based 32x1 Multiplexer. The design of finally implemented parallel to serial converter using the reversible logic based on Fredkin Gate, Feynman Gate, and Peres Gate is shown in figure 7.

1.6 Proposed Design

The proposed design includes the design of 32 - bit multiplexer using DRG4 gate. It is similar to Fredkin Gate in functionality but the quantum cost and garbage outputs are minimum.

1.6.1 DRG4 Gate

Dwivedi Rao Gate4 is a 3x3 gate capable of implementing ESOP (EXOR Sum of Product) and Code Conversion Operations. The DRG4 gate Inputs and Outputs are shown in figure 9 along with implementing equations. The corresponding truth table is shown in table 9, where all 8 combinations are evaluated for each and every output.

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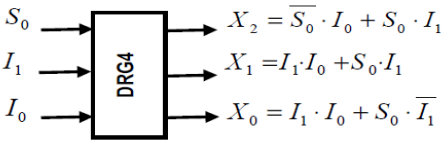
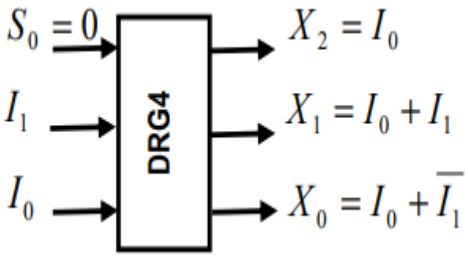


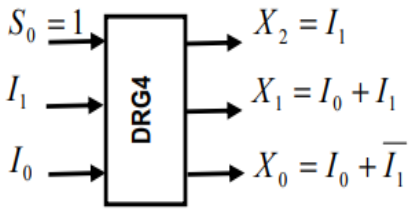
Figure 9: DRG4 Gate

Table 1: Truth Table of DRG4 Gate

Input			Output		
S_0	I_1	I_0	X_2	X_1	X_0
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	1	1	1



(a) DRG4 Gate as 2x1 Multiplexer Implementation – 1



(b) DRG4 Gate as 2x1 multiplexer Implementation - 2

Figure 10: Alternative implementations of DRG4 Gate as Multiplexer

The DRg4 gate can be implemented as 2x1 multiplexer in two ways as shown in figure 9. Based on the requirement to transmit either I0 or I1, the select line S0 is considered as logic 0 or logic 1 as shown respectively in figure 9 and figure 10. The quantum cost for DRG4 gate is 4 and the garbage outputs are 2.

1.6.2 Reversible Logic based Parallel to Serial Converter Design

The three bit counter is constructed with the help of three toggle flip-flops. A variety of counter circuits of various types of complexities are viable in IC form. The design of Reversible T-Latch is carried out the combination of Peres Gate and Feynman Gate as shown in figure 3.4.

The higher order design of 32-bit Parallel to Serial Bit conversion is performed in this work by using DRG4 Gate. The 32-bit multiplexer is designed as shown in figure 11.

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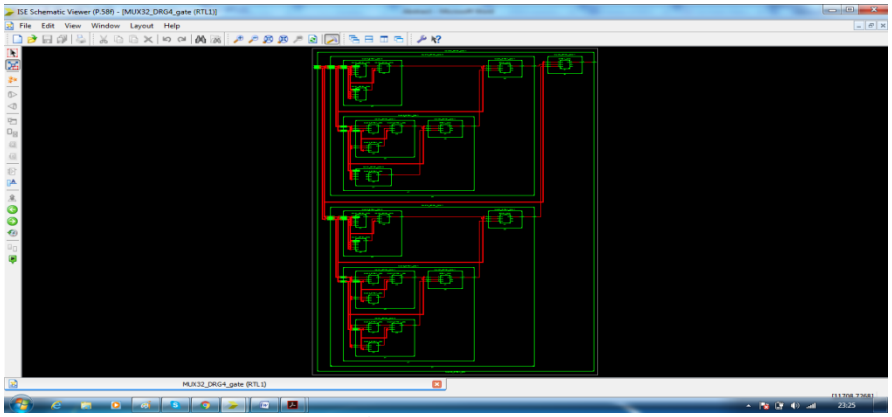

Figure 11: Design of 32-Bit Multiplexer using DRG4 Gate

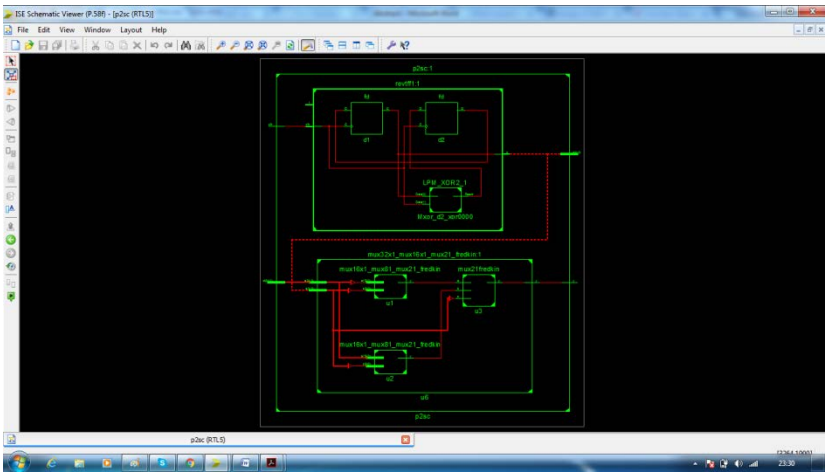

Figure 12: Design of Parallel to Serial Converter using Reversible T-Latches and DRG4 Gate based 32x1 Multiplexer.

The design of finally implemented parallel to serial converter using the reversible logic based on Fredkin Gate, Feynman Gate, and Peres Gate is shown in figure 12.

1.7 Results and Discussion

1.7.1 Simulation Results

- RTL Schematic: The synthesized design can be viewed as a schematic in the register transfer level (RTL) viewer. This schematic shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx® device. Viewing this schematic may help discovering design issues early in the design process.
- Test Bench: To simulate the design, you need both the design under test (DUT) or unit under test (UUT) and the stimulus provided by the test bench. A test bench is HDL code that allows us to provide a documented, repeatable set of stimuli that is portable across different simulators. A test bench can be as simple as a file with clock and input data or a more complicated file that includes error checking, file input and output, and conditional testing.

Design Summary: The Design Summary allows us to quickly access design overview information, reports, and messages. Figure 13 shows the simulation result of parallel to serial converters where the data input is of 32-bits with value 00110011111100111000101001010110. For the select lines of 10110, the output y is logic 1 as per requirement.

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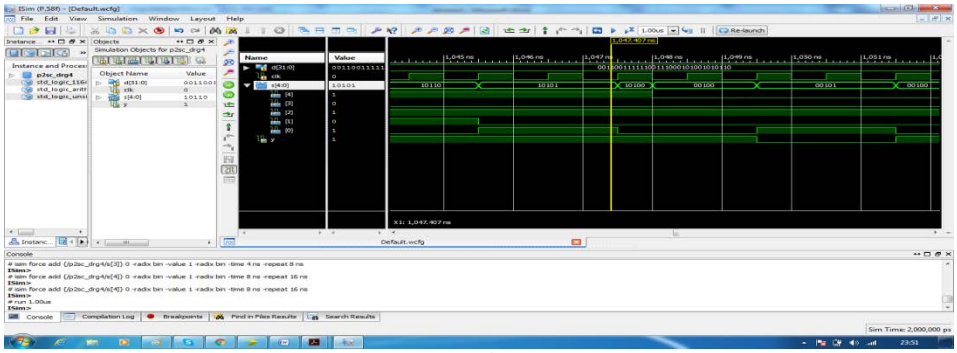

Figure 13: Simulation Result of Parallel to Serial Converter

Figure 13 shows the simulation result of 32x1 multiplexer used in the design for the data input of 00110011011101101100111000111010. For a select line of 01001, the output y is logic 1 as per requirement.

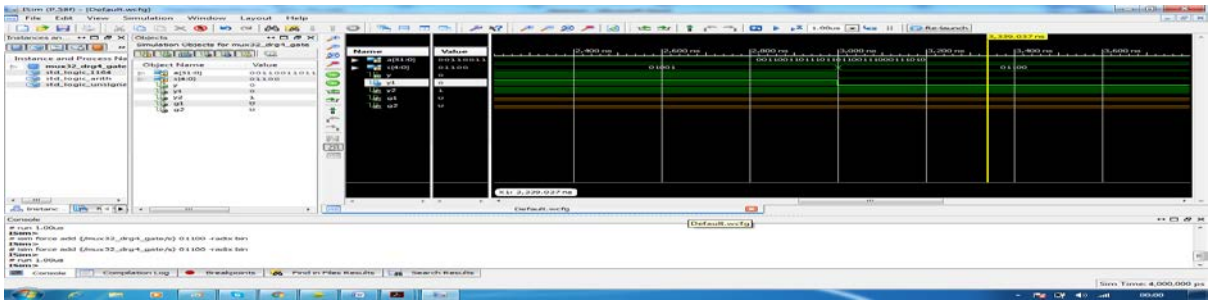

Figure 14: Simulation Result of 32x1Reversible Multiplexer

Figure 14 shows the simulation result of reversible T-latch used in the design for the toggle input of 1, the output q is logic 0 as per requirement.

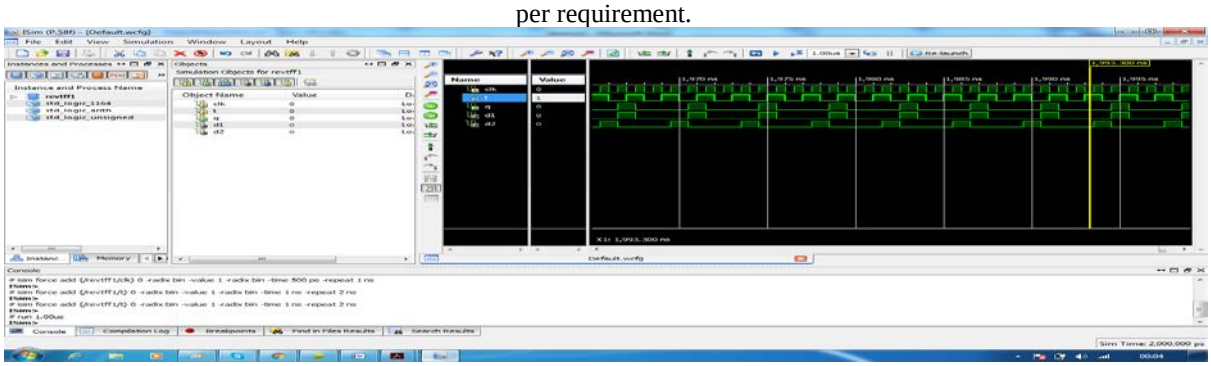

Figure 15: Simulation Result of Reversible T-Latch

1.7.2 Synthesis Results

The synthesis results include Design Summary, RTL Schematic, Technology Schematic, FPGA Floorplan and Routing and Power Analysis Report for Parallel to Serial Converter using DRG4 Gate as shown in figures 16 to 24.

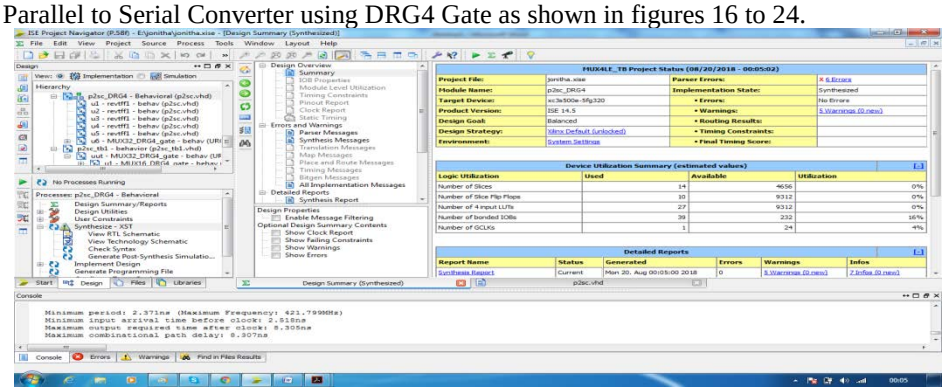

Figure 16: Design Summary of Parallel to serial converter using DRG4 gate

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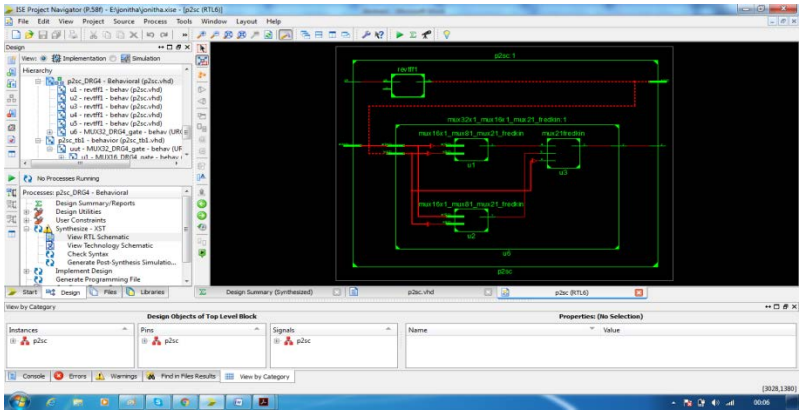

Figure 17: RTL Schematic of Parallel to Serial Converter using DRG4 gate

Figure 18: Technology Schematic of Parallel to Serial Converter using DRG4 gate

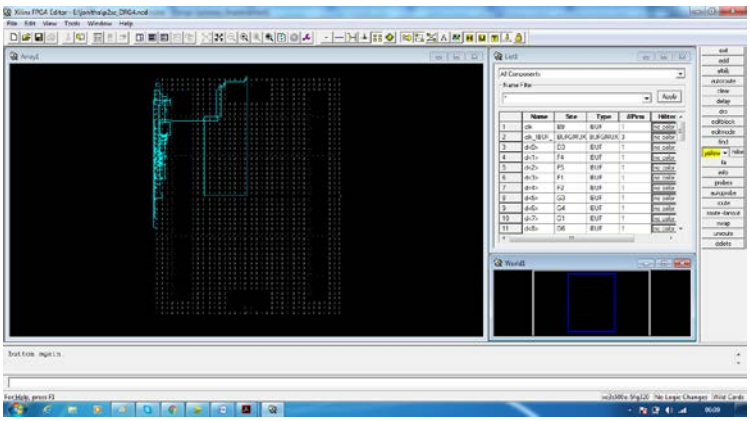

Figure 19: Floorplan and Routed Design of Parallel to Serial Converter using DRG4 gate

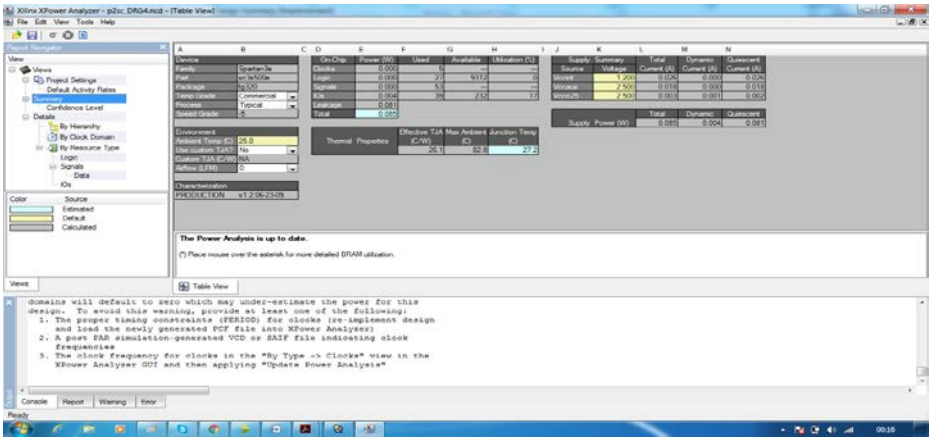

Figure 20: Power Report Summary of Parallel to Serial Converter using DRG4 gate

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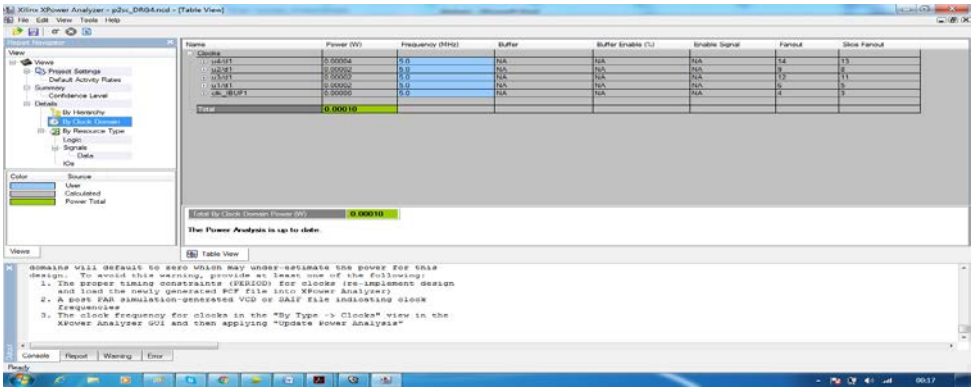

Figure 21: Clock domain Power of Parallel to Serial Converter using DRG4 gate

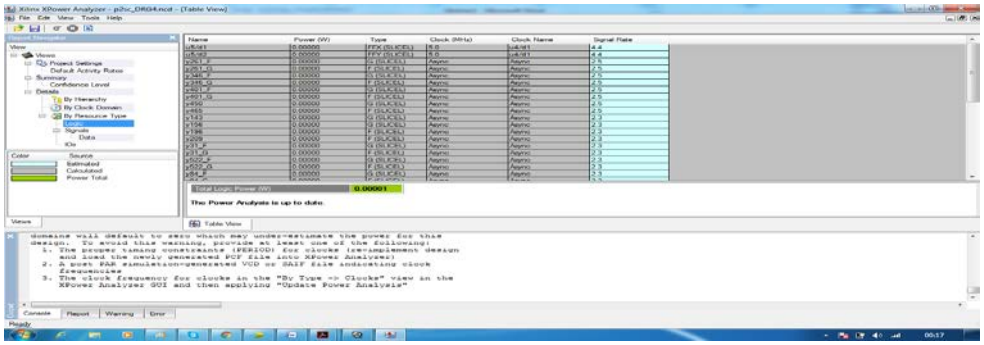

Figure 22: Logic Power of Parallel to Serial Converter using DRG4 gate

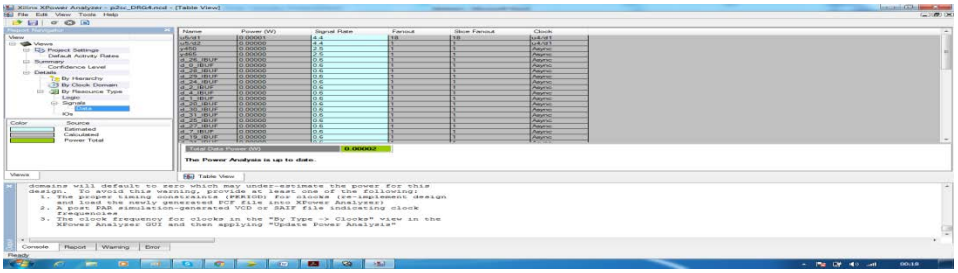

Figure 23: Data Power of Parallel to Serial Converter using DRG4 gate

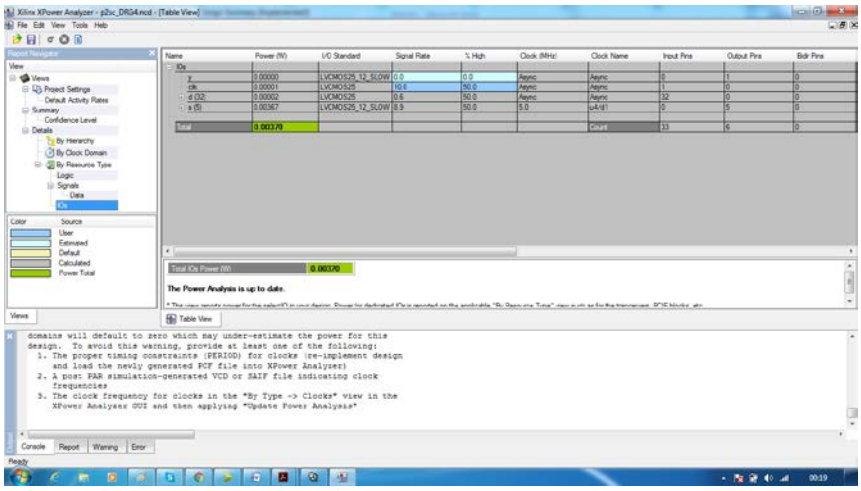

Figure 24: I/Os Power of Parallel to Serial Converter using DRG4 gate

The synthesis results include Design Summary, RTL Schematic, Technology Schematic, FPGA Floorplan and Routing and Power Analysis Report for Parallel to Serial Converter using Fredkin Gate as shown in figures 25 to 33.

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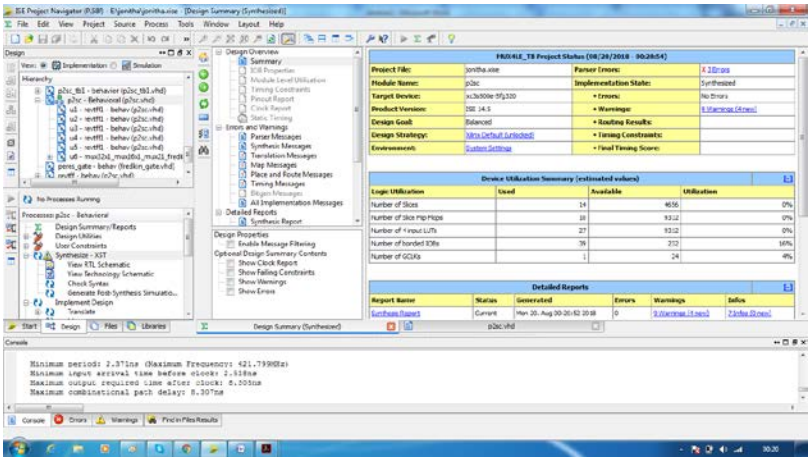

Figure 25: Design Summary of Parallel to Serial Converter using Fredkin Gate

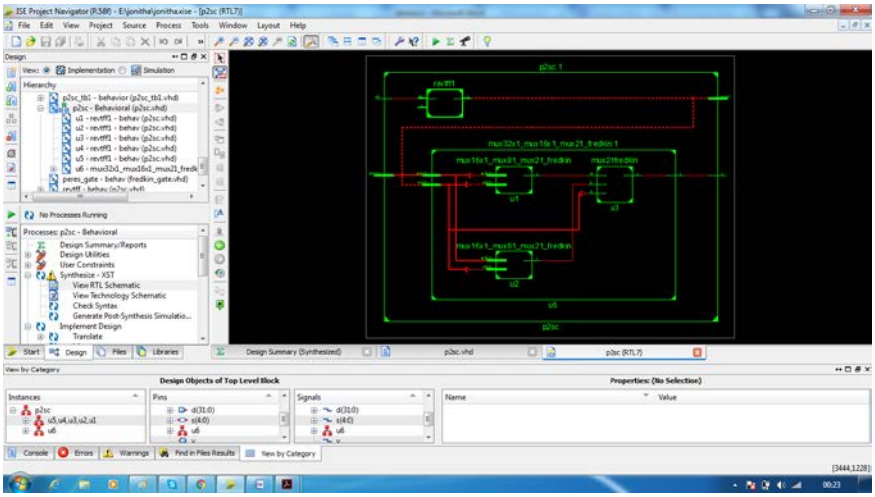

Figure 26: RTL Schematic of Parallel to Serial Converter using Fredkin gate

Figure 27: Technology Schematic of Parallel to Serial Converter using Fredkin gate

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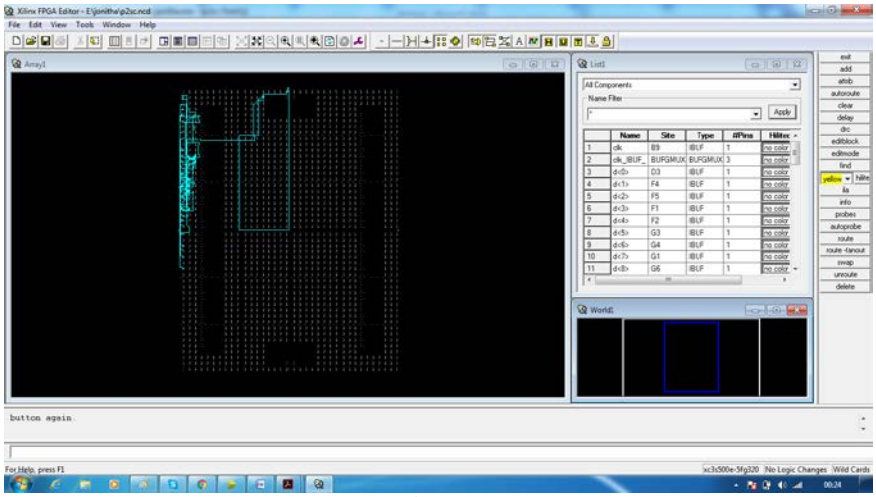

Figure 28: Floorplan and Routed Design of Parallel to Serial Converter using Fredkin Gate

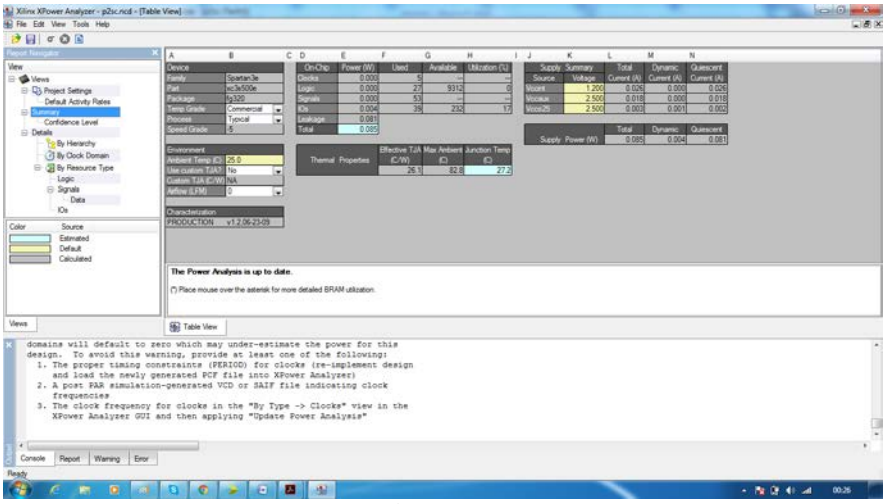

Figure 29: Power Report Summary of Parallel to Serial Converter using Fredkin Gate

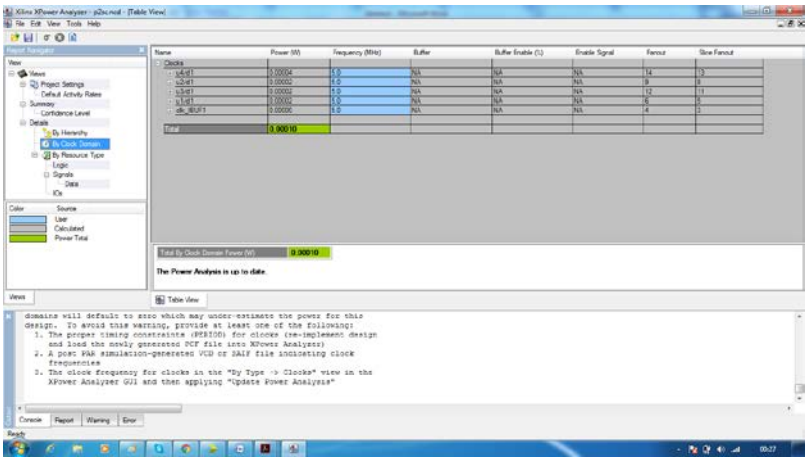

Figure 30: Clock Domain Power of Parallel to Serial Converter using Fredkin Gate

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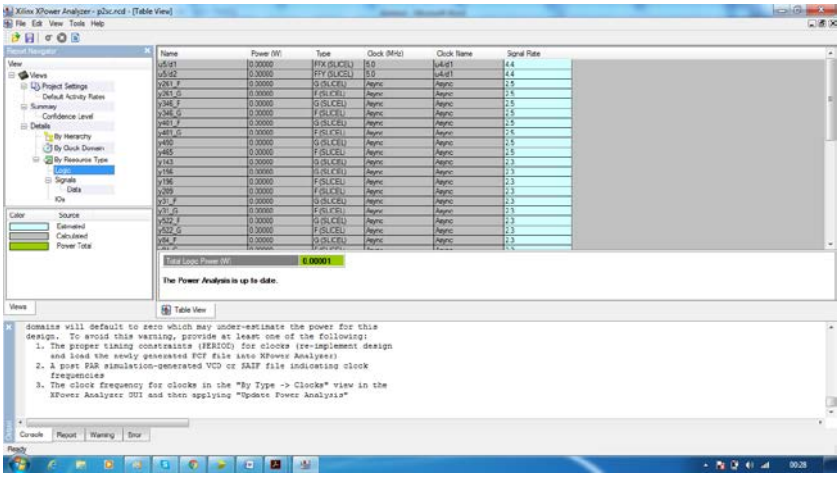

Figure 31: Logic Power of Parallel to Serial Converter using Fredkin Gate

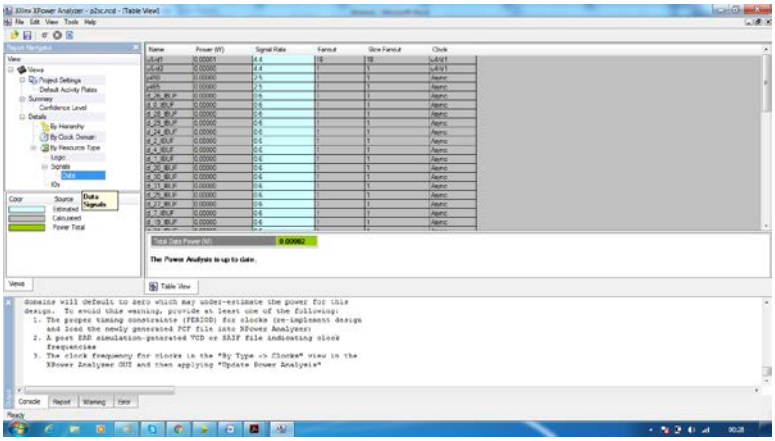

Figure 32: Signal Power of Parallel to Serial Converter using Fredkin Gate

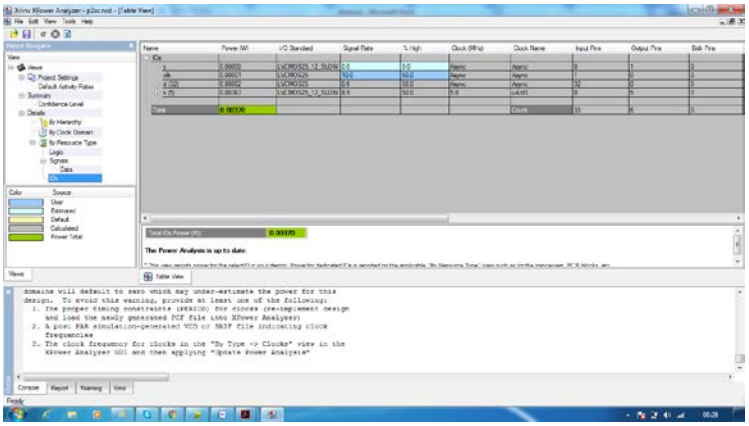

Figure 33: I/Os Power of Parallel to Serial Converter using Fredkin Gate

1.8 Comparative Results

Table 2 shows the comparison results of Existing designs of Multiplexer as logic element and Fredkin Gate. Table 2: Comparative Results of Existing MUXLE and Fredkin Gate

Designs	Existing Design (MUXLE)	Proposed Design (MUX41fredkin)
Number of Slices	2/4656	1/4656
Number of 4-input LUTs	4/9312	2/9312
Number of Bonded IOBs	11/232	7/232
Delay	7.003ns	6.054ns
Average Fanout of Non-Clock Nets	1.08	1.14
Logic Power	0.00001 Watts	0.00001 Watts
Data Signal Power	0.00003 Watts	0.00002 Watts
IOs Power	0.00115 Watts	0.00110 Watts

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From table 2, as the area occupied, delay and power are less reversible logic proves to be better choice. Also fanout is increasing which is a desirable quantity. Table 3 shows the comparison results of Multiplexer Design at various complexities by using Fredkin Gate.

Table 3: Comparative Results of Multiplexer Design at Various Complexities

Designs	Mux32x1	Mux16x1	Mux8x1	Mux4x1
Number of Slices	12	5	3	1
Number of 4-input LUTs	22	10	5	2
Number of Bonded IOBs	38	21	12	7
Delay	8.686ns	7.633ns	7.172ns	6.054ns
Average Fanout of Non-Clock Nets	1.62	1.58	1.33	1.14
Logic Power	0.00007	0.00003	0.00001	0.00001
Data Signal Power	0.00022	0.00010	0.00003	0.00002
IOs Power	0.00146	0.00125	0.00116	0.00110
Quantum Cost	25	20	15	10
Garbage Outputs	62	30	14	6

From table 2 and 4, the comparison results show that DRG4 Gate is a better choice than Fredkin Gate.

Table 4: Comparative Results of DRG4 Gate as 2x1 Multiplexer and 4x1 Multiplexer

Designs	4x1 MUX	2x1 MUX
Number of Slices	1/4656	1/4656
Number of 4-input LUTs	2/9312	1/9312
Number of Bonded IOBs	7/232	4/232
Delay	6.054ns	5.753ns
Average Fanout of Non-Clock Nets	1.14	1.00
Logic Power	0.00001 Watts	0.00000 Watts
Data Signal Power	0.00002 Watts	0.00000 Watts
IOs Power	0.00110 Watts	0.00107 Watts
Quantum Cost	8	4
Garbage Outputs	6	2

From table 5, both the quantum cost and garbage outputs are reduced with proposed DRG4 Gate which is a desirable for reducing the heat dissipation in quantum computing.

Table 5: Comparative Results of Parallel to Serial Converter using Fredkin Gate and DRG4 Gate

Designs	Existing Parallel to Serial Converter Design (using Fredkin Gate)	Proposed Parallel to Serial Converter Design (using DRG4 Gate)
Quantum Cost	100	85
Garbage Outputs	42	40

1.9 Conclusion: With the advancement of technology, there has been more and more need for the gigabit rate link for storage application, data communication, computer networks and etc. To meet with the high processing multi-gigabit speeds and system performance, it becomes necessary to have prompt and efficient high-speed inter-connects. Traditional parallel link has been used in circuits for a long time, which let the data be sent over multiple channels simultaneously. A Serial Data link is preferred for long distance communication. This work verifies the design of parallel to serial converter using reversible logic gates like Fredkin Gate, Peres Gate, Feynman Gate and DRG4 Gates. The designs are coded in VHDL using structural modelling. These are synthesized and simulated in Xilinx ISE Design Suite 14.5. The results are compared for various parameters and the proposed design i.e., by using DRG4 gate is found to be a better choice of implementing the parallel to serial converter practically due to less quantum cost, area, power dissipation, garbage outputs, etc. As it reduces the quantum cost by 15% and Garbage outputs by 5%.

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