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Multilevel Voltage Source Inverter with Reduced Number of Circuit Devices to Maximize the Number of Output Voltage Levels

Robin Roy
Department of EEE, Trinity College of Engineering, Thiruvananthapuram

Bindu
Department of EEE, CSI Institute of Technology, Thovalai

***Abstract*—Nowadays multilevel inverters are developing generally due to reduced voltage stress on power switches and low total harmonic distortion (THD) in output voltage. However, for increasing the output voltage levels the number of circuit devices are increased and it results in increasing the cost of converter. In this paper, a novel multilevel inverter is proposed. The suggested topology uses less number of power switches and related gate drive circuits to generate the same level in output voltage with comparison to traditional cascaded multilevel inverter. With the proposed topology all levels in output voltage can be realized. As an illustration, a symmetric 13-level proposed inverter have been simulated and implemented. The total peak inverse (PIV) and power losses of presented inverter are calculated and compared with conventional cascaded multilevel inverter. The presented analyses show that the power losses in the suggested multilevel inverter are less than the traditional inverters. Presented simulation and experimental results demonstrate the feasibility and applicability of the proposed inverter to obtain the maximum number of levels with less number of switches.**

I. INTRODUCTION

Multilevel inverters have been attracting growing interest since introduced at early 80s [1], particularly because of the higher power rating and quality, higherefficiency, lower total harmonic distortion and lower switching losses [2] & [3]. The mentioned advantages are achieved while the multiple dc sources are used to generate the output voltage waveform [4]. In recent years, MULTILEVEL inverters are one of the most versatile and powerful components that are utilized in many industrials such as FACTS devices [5] & [6], HVDC [7] & [8], etc. Various topologies for multilevel inverters have been introduced over the past 20 years, the most popular topologies are the diode-clamped [9], flying capacitor [10] and cascaded H-bridge topologies [11]. Also, many modulation techniques such as different pulse width modulation (PWM) techniques and space-vector PWM schemes are proposed to improve the output voltage harmonic spectrum [12] & [13]. To synthesize multilevel output, voltage clamping is one of the most important concerns. The definition of clamping is to limit the switchs terminal voltage in a proper range by using clamping devices. In the three mentioned multilevel-inverter structures, voltages are clamped by diodes, by capacitors and by separated voltage sources in the diode-clamped, the flying capacitor and the cascaded multilevel structures, respectively [14]. One property that distinguishes the cascaded H-bridge from the other multilevel structures is the capability of utilizing various dc voltages on the separate H-bridge cells. This property causes to split the power conversion amongst highervoltage lower-frequency and lower-voltage higher-frequency inverters [15]. Increasing the number of DC voltage sources causes to increase the number of levels in output voltage waveform and thereby the inverter voltage output waveform reaches a nearly sinusoidal waveform while operating at a fundamental frequency switching scheme [16]. Also to provide a large number of output levels instead of increasing the number of DC sources, asymmetric topologies of multilevel inverters can be used [17] & [18]. Unfortunately, multilevel inverters have some drawbacks. One of their disadvantages is the great number of required components especially power switches and gate drivers. This increases the cost, complexity and size of inverter [3]. It is a good idea to suggest new multilevel-inverter topologies with higher performance by reducing the number of required components [19]. In new multi-level inverter topologies with reduction of switches total PIV will increase, e.g. semi cascaded inverter uses almost half number of switches compared with cascaded converter, but this reduction results that the PIV values is as much as 1.5 times in semi-cascaded converter compared with cascaded converter [20]. This paper proposes a novel topology based on connected several independent units. Compared to traditional cascaded inverter, the proposed topology reduces the number of switches. Simulation and experimental results are given. Presented results show the feasibility and good performance of proposed topologies

II. CONVENTIONAL CASCADE MULTILEVEL INVERTERS CONFIGURATION

Fig. 1 shows a single-phase cascaded multilevel inverter with separated DC voltage sources. The output voltage of cascaded multilevel inverter is synthesized by summing the output voltages of bridges. Each H-bridge generates a threelevel square-wave voltage associated with four switches and one DC voltage source. In a cascaded inverter with 2n DC voltage sources with n different values (a set of single phase cascaded inverter shown in Fig. 1).In a cascade multilevel inverter with 2n-DC sources, always 4n switches must be turn on in various operation modes, so the maximum output voltage can be defined as:

$$V_{0_{max}} = 2\sum_{i=1}^{n} V_i - 4nV_d \quad (1)$$

Where V_d is the on-state voltage drop of a switch.

To attain a large number of output levels, the asymmetrical

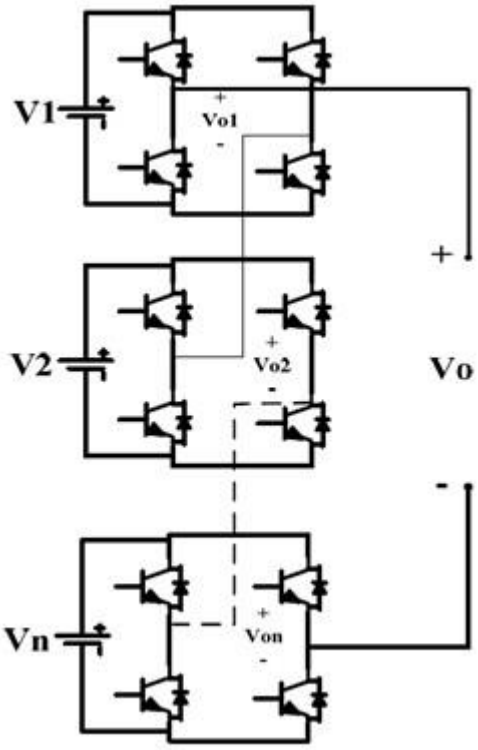

Fig. 1. A single phase cascaded multilevel inverter

DC sources can be employed in cascaded multilevel inverter instead of increasing the number of H–bridges. The major sufficiency of cascaded topology is the modularity of control and protection requirements of each H-bridge, but the higher amount of required switches is the major it's disadvantage. In the proposed topology the number of circuit devices is substantially reduced.

III. PROPOSED TOPOLOGY

The proposed topology includes several independent units which have been combined properly. Each unit consists of DC sources with the different value and five switches and related gate drive. In the proposed topology Vi can set to adjust the output voltage level to a desired value instead of manipulating the inverter circuit. In this case the proposed multilevel inverter is known as asymmetric topology, which increases the number of the output voltage levels without adding any DC voltage sources and switches. The asymmetric topology of 13-level proposed inverter is shown in Fig. 2

IV. COMPARISON STUDY

The main goal of this paper is to present a new topology which the amount of the required components is lower than the conventional cascaded multilevel inverters. The number of required switches and also the ratings of them are the great importance in multilevel inverter structures. Its apparent that the number of switches in proposed topology is noticeably lower than the conventional cascaded inverter in a same output level. Also, voltage and current ratings of the power switches play important roles on the overall cost of the system and realization of the inverter. The total PIV of proposed inverter

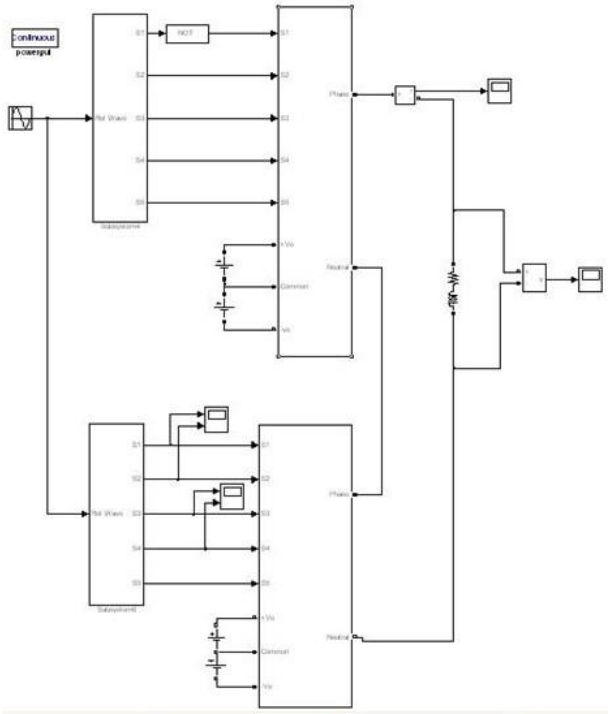

Fig. 2. A single phase cascaded multilevel inverter

is lower than the traditional cascaded multilevel inverter with same number of DC voltage sources. Also the number of onstate switches is lower in the proposed topology compared to conventional cascade and so the output voltage drop is reduced. The major sufficiency of cascaded topology is the modularity of control and protection requirements of each Hbridge, but the higher amount of required switches is the major it's disadvantage. In the proposed topology the number of circuit devices is substantially reduced. he proposed topology requires less number of switches and gate driver circuits for realizing the output voltage levels. Therefore, this achievement reduces the installation area and cost of the proposed topology in comparison with the conventional cascaded inverter for realizing the same output voltage levels. The number of on state switches results in output voltage drop and conduction losses of converter. Therefore, it is considered as a substantial factor to compare the conventional cascaded inverter and proposed topology. The number of on-state switches for proposed topology is less.

V. SIMULATION RESULTS

To validate the good performance of the proposed multilevel inverter, a single phase 13-level proposed topology is considered, and the simulation results are obtained. The MATLAB/Simulink software has been used for simulation. The prototype of proposed topology which includes 4-DC

sources and 10 switches generating staircase waveform with the maximum 30 V in output is considered. The voltage waveform of proposed asymmetric 13-level inverter is shown in Fig. 3.

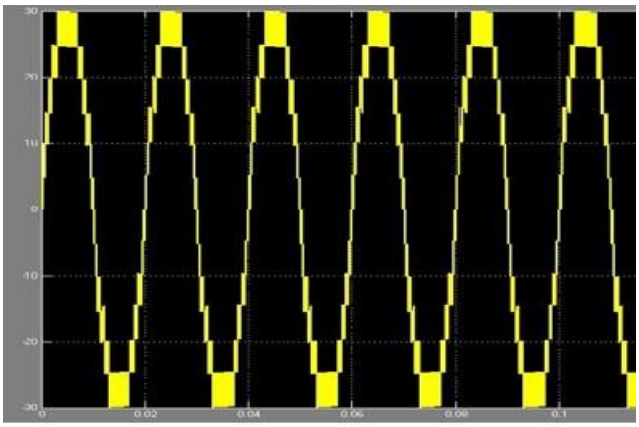

Fig. 3. The voltage waveform of proposed 13-level inverter

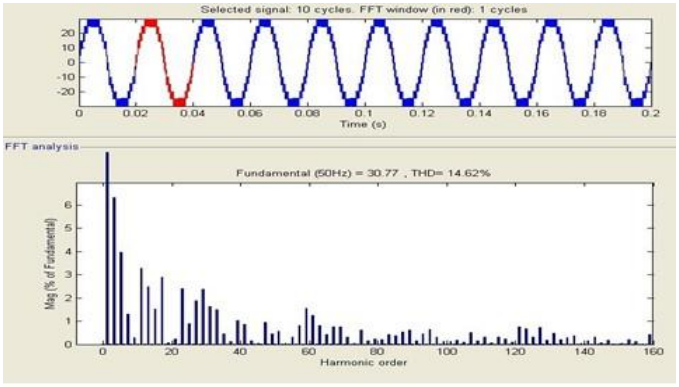

Fig. 4. The FFT harmonic spectra in harmonic order of proposed 13-level Inverter

VI. CONCLUSION

A new multilevel inverter with a reduced number of power components has been suggested to increase the number of output voltage levels. With the suggested inverter the same level in output voltage is generated with fewer numbers of switches and related gate drive circuits compared to traditional cascaded inverter. Also the number of on-state switches is lower in the proposed topology compared to conventional cascade, so the output voltage drop is reduced and conduction power loss is decreased. The simulation results are provided to submit the good performance and applicability of proposed inverter. The Total Harmonic Distortion (THD) of the proposed 13-level asymmetric topology is 14.62

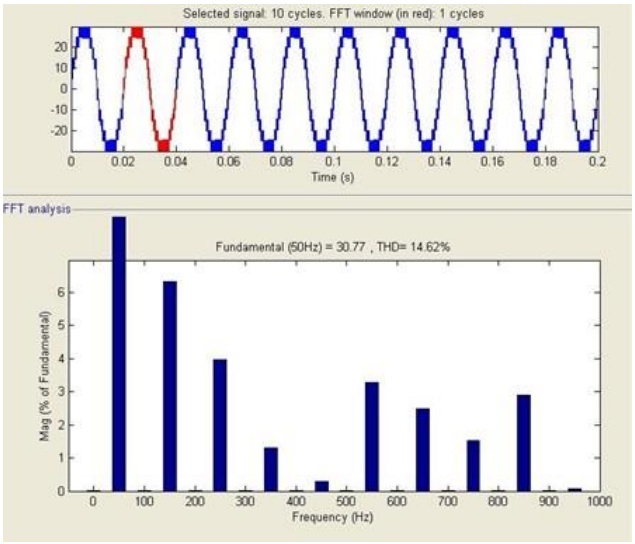

Fig. 5. The FFT harmonic spectra in harmonic order of proposed 13-level inverter

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