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Multilevel Inverter using Switch Reduction Technique

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***Abstract*- With a unique pulse width-modulated (PWM) control technique, this research presents a single-phase fifteen-level inverter employing seven switches. The output voltage level of the proposed multilayer inverter is increased by employing fewer switching cycles driven by multicarrier modulation techniques. The inverter is capable of producing fifteen levels of output-voltage (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage. The proposed system was verified through simulation.**

Keywords-Multilevel Inverter, Multi carrier modulation system, Pulse Width-Modulation (PWM), total harmonic distortion (THD).

I. INTRODUCTION

Multilevel inverters are used to reduce error by providing nearly sinusoidal output-voltage waveforms, output current with a better harmonic profile, less stressing of electronic components due to lower voltages, lower switching losses than conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact.

Over the years, various topologies for multilayer inverters have been developed. Diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel are some of the most common. This work presents a modified H-bridge single-phase multilevel inverter with one diode embedded bidirectional switch and a novel pulse width modulation (PWM) approach.

II. MULTILEVEL INVERTER

A multilevel inverter generates high voltage by connecting devices with lower voltage ratings in series. It also has the capability of generating many output voltage levels, which could result in a high-quality output voltage. It does, however, increase the number of switching devices and other components, which leads to more complexity issues and higher system costs.

Many multilayer inverter topologies have been investigated in order to provide a sinusoidal wave-like output voltage wave with the fewest circuit components possible. A multilayer inverter has various advantages over a traditional two-level converter that uses pulse width modulation with a high switching frequency (PWM).

The nice features of a multi-level inverter can be briefly summarized as follows below.

- Multilevel inverters not only can generate the output voltages with low distortion, but also can reduce the dv/dt stresses
- Staircase waveform quality
- electromagnetic compatibility (EMC) problems can be reduced by reduce the dv/dt stresses.
- Multilevel inverters produce small Common mode voltage, therefore the stress in the bearings of a motor connected to a multilevel motor drive can be reduced
- Input current Multilevel inverters can draw input current with low distortion.
- Switching frequency Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM, which mean means lower switching loss and higher efficiency.

Flexible AC transmission systems (FACTS) Controllers, HVDC, Train Traction, Automotive applications, renewable energy power conversion and transmission, and other multilayer converters are often used for high power applications.

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The seven-level inverter was used to construct the proposed fifteen-level inverter. A single phase conventional H-bridge inverter, three switches.

And three voltage sources make up this system. This H-bridge topology has a number of benefits over other topologies for inverters with the same number of levels, less power switches and power diodes are used.

The inverter can provide fifteen output voltage levels with proper switching. (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage.

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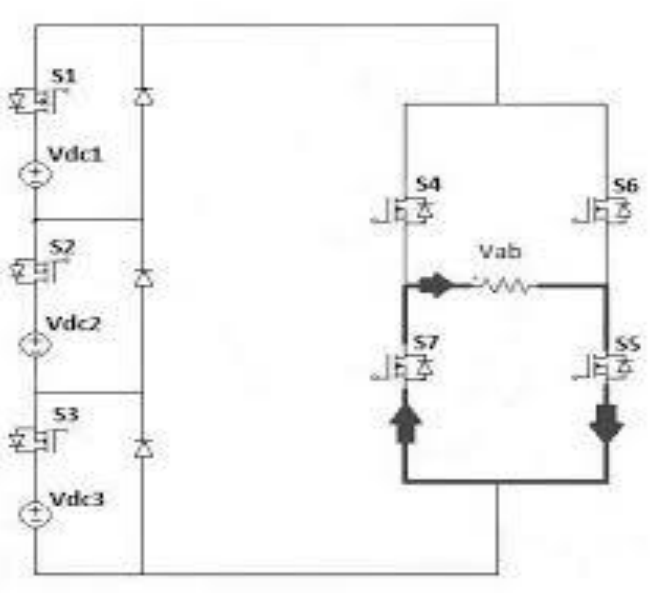

Fig 1- Fifteen Level Inverter Circuit diagram

The proposed inverter's operation can be divided into fifteen switching states; the required fifteen levels of output voltage were generated as follows.

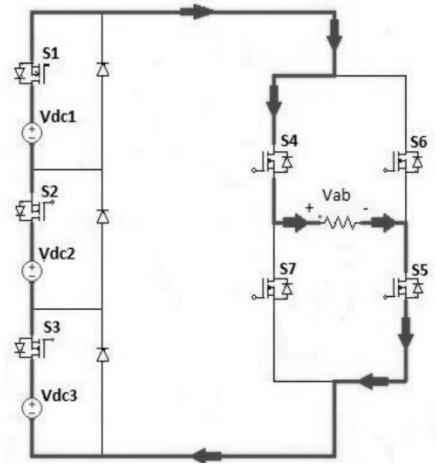

Fig 2-mode 1

Switch S1, S2, S3 & S4, S5 is ON, the voltage is maximum +Vdc across the load which is shown in Figure 2

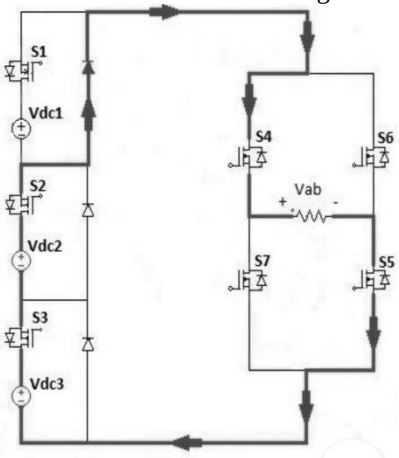

Fig 3-mode 2

Switch S2, S3 & S4, S5 is ON and the voltage is +6Vdc/7 across the load which shown in Figure 3.

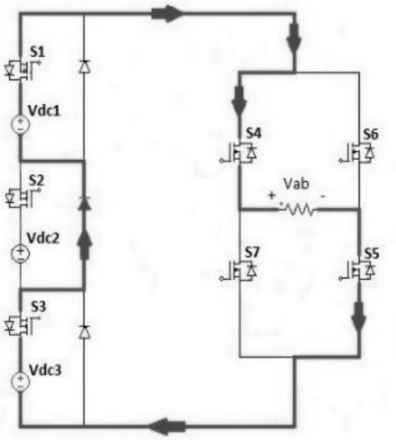

Fig4- mode 3

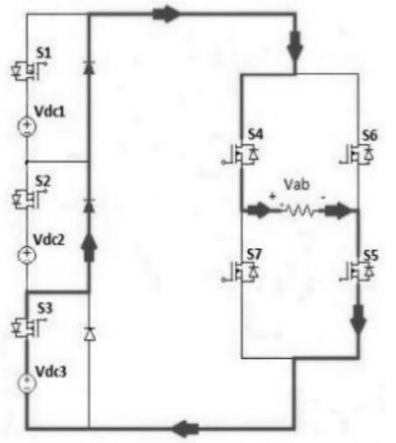

Fig5- mode 4

Switch S1, S3 & S4, S5 is ON and the voltage +5Vdc/7 across the load which shown in Figure 4

Switch S3 & S4, S5 is ON and the voltage is +4Vdc/7 across the load which is shown in Figure 5

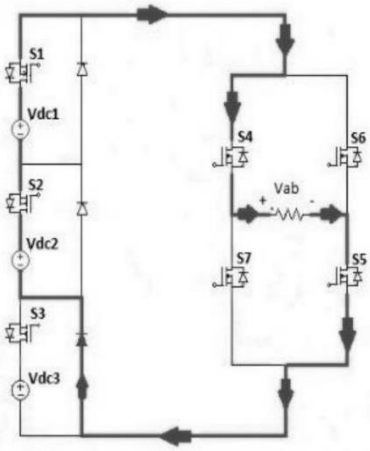

Fig6- mode 5

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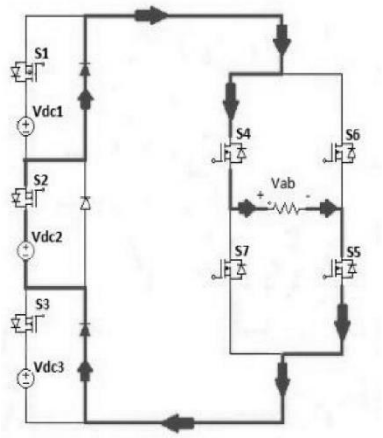

Fig7- mode 6

Switch S1, S2 & S4, S5 is ON and the voltage is +3Vdc/7 across the load which is shown in Figure 6
Switch S2 & S4, S5 is ON and the voltage +2Vdc/7 across the load which is shown in Figure 7.

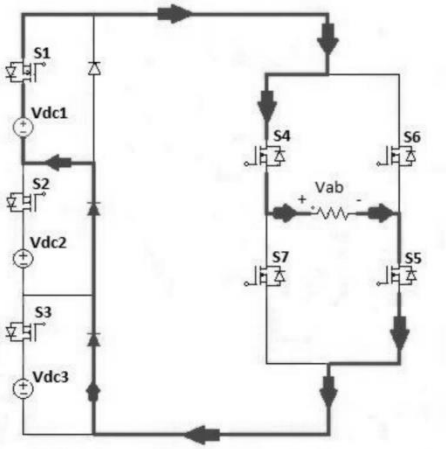

Fig8- mode 7

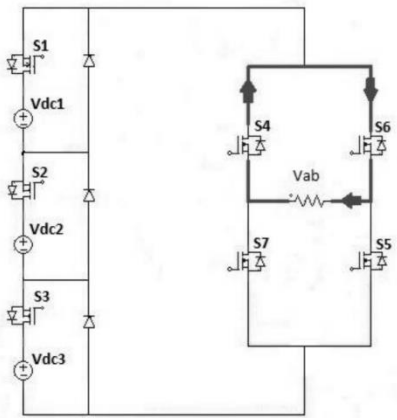

Fig9- mode 8

S1 & S4, S5 are turned on, and the voltage across the load is +Vdc/7, as illustrated in Figure 8.
Turning on MOSFETs produces the Zero Output voltage level. Figure 9 shows the switches S4 and S6.

Switches S1 and S6, as well as S7, are turned on, and the voltage across the load is –Vdc/7, as illustrated in Figure 10.
Switches S2 and S6, as well as S7, are turned on, and the voltage across the load is -2Vdc/7, as illustrated in Figure 11.

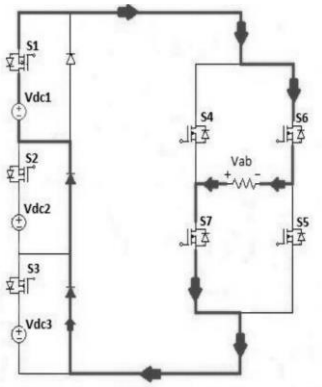

Fig10- mode 9

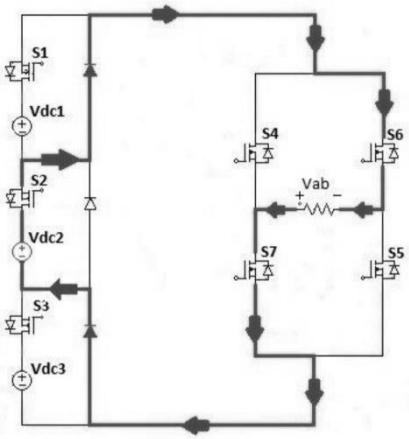

Fig11- mode 10

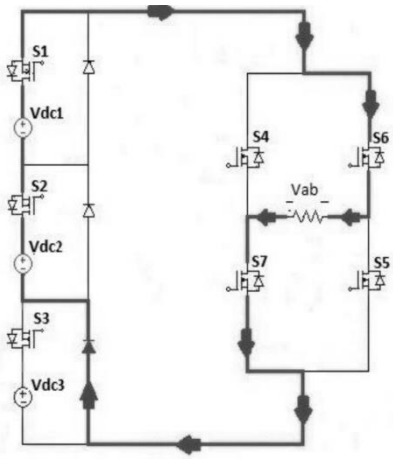

Fig12- mode 11

Switches S1, S2 & S6, S7 are turned on, and the voltage across the load is -3Vdc/7, as illustrated in Fig12.

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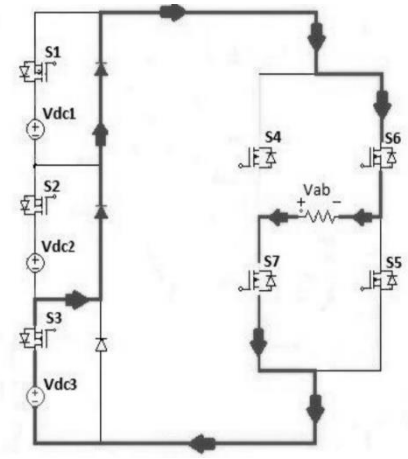

Fig13- mode 12

Switch S3 & S6, S7 is ON and the voltage -4Vdc/7 across the load as illustrated in Figure 13.

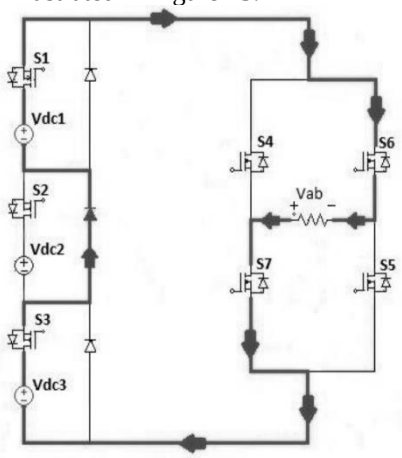

Fig14- mode 13

The switches S1, S3, S6, and S7 are all turned on, and the voltage across the load is -5Vdc/7, as illustrated in Figure 14..

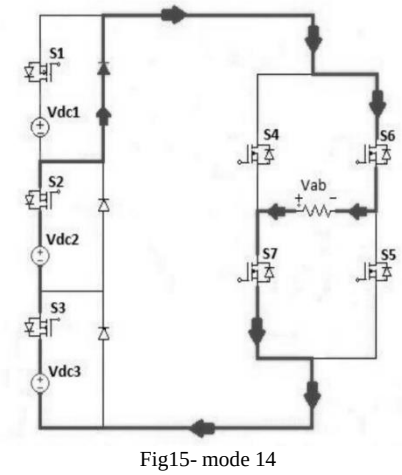

Fig15- mode 14

The switches S2, S3, and S6, S7 are all turned on, and the voltage across the load is -6Vdc/7, as illustrated in Figure 15.

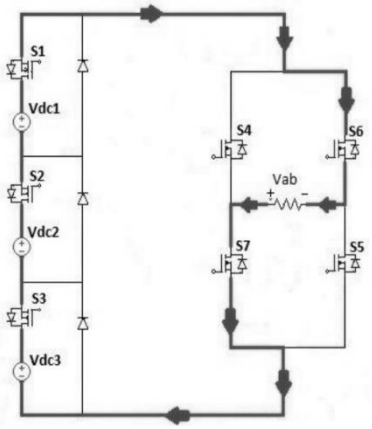

Fig14- mode 13

Switch S1, S2, S3 & S6, S7 is ON and the voltage –Vdc (negative maximum) across the load which is shown in Figure 17.

IV. PWM GENERATION

In this study, a multi-carrier pulse width modulation technique is used to generate the fifteen-level output voltage. Seven equal amplitude carrier triangle signals with offset are compared to the sinusoidal reference signal.

The switches S1, S2, and S3 receive these PWM signals. The two sinusoidal signals with 180 degree displacement signals are then compared to the carrier triangle signal; these PWM pulses have a dead band, which prevents the two devices from shooting each other. The single phase inverter circuit switches S4, S5, S6, and S7 receive these PWM pulses.

In this case, the switching device is a MOSFET, which is less expensive than an IGBT. FPGA is the processor in use here. It's classified as a Very large scale integration system. Many of the pins in FPFA are multiplexed pins.

Voltage level	S1	S2	S3	S4	S5	S6	S7
Vdc	ON	ON	ON	ON	ON	OFF	OFF
6/7Vdc	ON	ON	ON	ON	ON	OFF	OFF
5/7Vdc	ON	ON	OFF	ON	ON	OFF	OFF
4/7Vdc	ON	OFF	ON	ON	ON	OFF	OFF
3/7Vdc	ON	OFF	OFF	ON	ON	OFF	OFF
2/7Vdc	OFF	ON	OFF	ON	ON	OFF	OFF
1/7Vdc	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF
-1/7Vdc	OFF	OFF	ON	OFF	OFF	ON	ON
-2/7Vdc	OFF	ON	OFF	OFF	OFF	ON	ON
-3/7Vdc	ON	OFF	OFF	OFF	OFF	ON	ON
-4/7Vdc	ON	OFF	ON	OFF	OFF	ON	ON
-5/7Vdc	ON	ON	OFF	OFF	OFF	ON	ON
-6/7Vdc	ON	ON	ON	OFF	OFF	ON	ON
-Vdc	ON	ON	ON	OFF	OFF	ON	ON

Fig 15. Switching sequence for 15 level inverter

International Journal of Engineering Research & Technology (IJERT)
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V. SIMULATION RESULTS

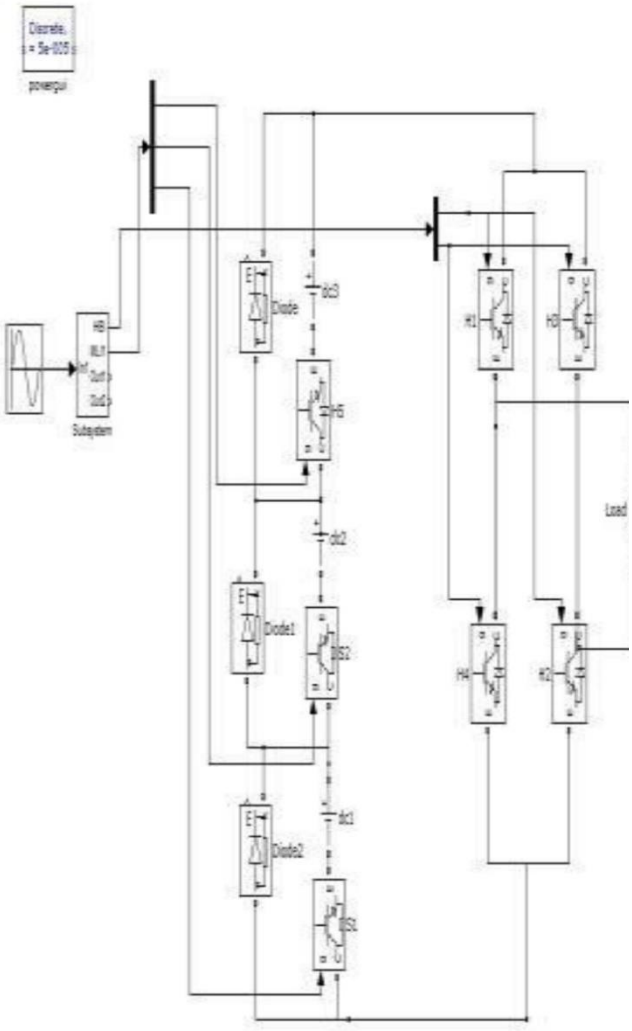

Fig 16. Mat lab Simulink model

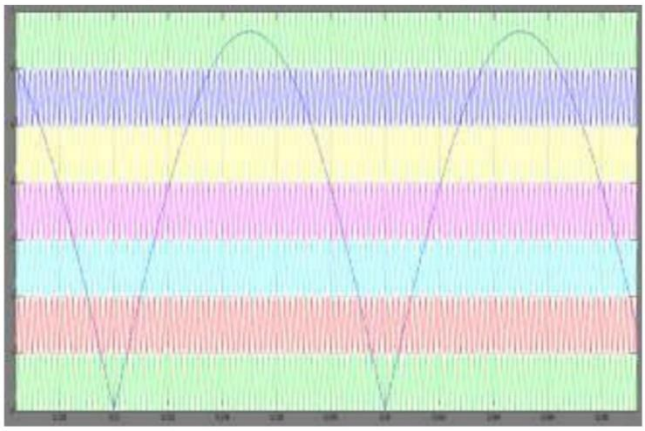

Fig 17. Mat lab Simulink model for Multi carrier PWM generation

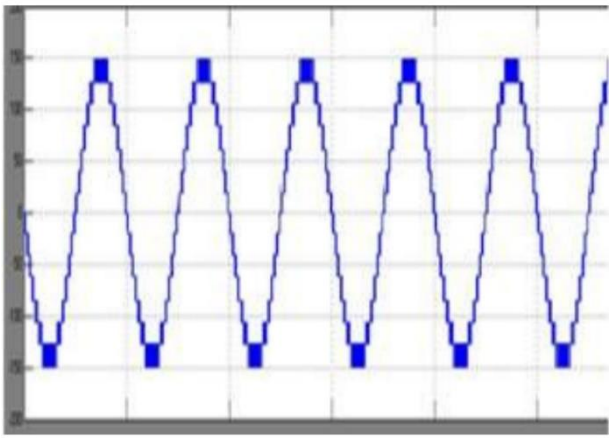

Fig 18. Fifteen level inverter simulation output voltage

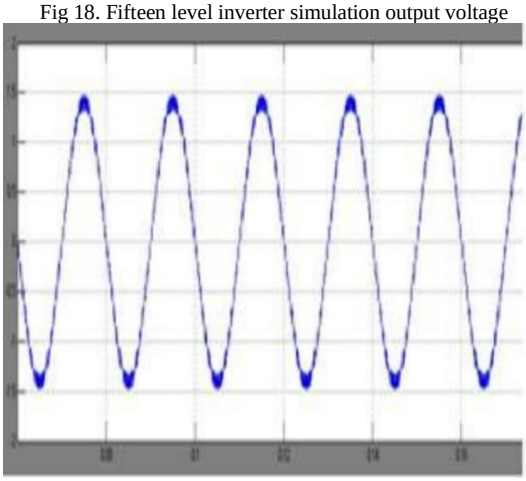

Fig19. Fifteen level inverter simulation output current

VI. CONCLUSIONS

Multilevel inverters provide better output waveforms and reduced THD than single-level inverters. For the recommended multilevel inverter, this paper has provided a unique PWM switching mechanism. To create the PWM signals in this paper, only one reference signal is compared to a triangular wave signal. In this multi level inverter, there are three separate DC voltage levels utilised. As a result, this design method is referred to as asymmetrical cascaded inverter. The fifteen levels of output voltage are obtained by changing the modulation index and varied levels of DC voltages. The THD level of this fifteen level inverter is 3.530 %

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