Multilevel Inverter Topology with Self Voltage Balancing Technique

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***Abstract*: In the realm of DC/AC converters, Multi-Level Inverters (MLI) have become trend & one of the most important requirements in many industrial applications. The main goal of this project is to obtain the number ofvoltage level at the output while reducing the power circuit complexity. The suggested topology has the important benefits of self-voltage balancing of its capacitor voltage regardless of load type, load dynamic or modulation index. Here the technique pulse width modulation is adopted for simulating the output voltages and currents of the MLI. Finally, a prototype is created and tested to ensure that the concept is feasible and performs well.**

Keywords: DC-AC Converter, MLI, CHB.

I.INTRODUCTION

The current situation of electricity demand is rapidlyincreasing, resulting in a depletion of conventional energy resources, while the global concern is how to meet future electricity demand using sustainable andreliable energy sources such as non-conventional or renewable energy resources. As a result, researchers are concentrating their efforts on the power generation source, which is based on traditional energy resources [1]. Alternating current is the most common way to transmit and use electrical electricity. Direct current is produced by various types of electrical generation and storage equipment,such as PV modules and batteries. Inverter is a device that converts direct current electricity to alternating current for use in stand-alone systems or to supply electricity to a power grid [2]. A multilayer inverter is a power electrical device that uses numerous lower-level DC voltages as an input to provide a specified alternating voltage level at the output. To generate AC voltage from DC voltage, most people utilize a two-level inverter.

Since 1975, the concept called MLI has been introduced. Three level converters are where thename “multilevel inverter” came from. Initially, the inverters were primarily utilized to power the lighting load when the grid went down. However, thanks to recent technological advancements, inverters are now being employed in motor drives, UPS, and power system utilization [3]. Multilevel inverters are made up of a series of power semiconductors and dc voltage sources, the outputs of which produce stepped waveform voltages [4]. The MLI can provide a near-sinusoidal output voltage; however, the output voltage quality is dependent on the how many voltage levels in the inverter [2]. It provides a viable method for synthesizing an output voltage in medium and high-power systems, allowing for a decrease of harmonic content in voltage and current waveforms. Multilevel inverters work on the premise of dividing the inverter's operational voltage between power electronic switches, allowing low-voltage switches to process high-voltage outputs.

CHB is the most appealing solution among these topologies because to its basic structure, adaptability,and ease of control. To achieve a large number of voltage levels, the other two MLIs, Neutral Point Clamped (NPC) and Flying Capacitor (FC), require a greater number of clamping diodes and floating capacitors. The Vo levels in CHB are determined by the number of cascaded units as well as the amount of each unit's dc-voltage sources.

II.METHODOLOGY

Two novel topologies are described in this study thatmay be used in both symmetrical and asymmetrical arrangements. The designed architecture has a modular design since it is cascaded and allows system reliability for symmetrical and asymmetricalcombinations while putting reduced overvoltage on the semiconductor switches. Because of its self- voltage regulating capacity, it should not require an additional circuit to balance the capacitor voltage. The capacitor's capacity to sustain a constant voltagewithout any of the assistance of an open circuit, independent of load dynamics, modulated signal, or transients, is referred to as “self-voltage balancing”.The suggested architectures' symmetric and asymmetric layouts provide the more current output while using the fewest switches. In the suggested structures, the number of two-directional switches also decreases dramatically. In addition, the suggested topologies offer the benefit of balanced DC source use and lower losses.

In the paper [6], a topology of MLI, that minimizes the number of materials used. Because the switch in its H-bridge must handle the maximum load voltageat the output, it cannot be used at high dc voltages, which is a significant drawback.

Similar MLI design is given in [5], although the usage of switchingdevices, a diversity of switches, and restrictions on high-voltage operations are the primary limitations. Alternative symmetrical MLI architecture has already been described in [7], which uses fewer switches and reduces flipping economic loss significantly in comparison to standard MLI. Unfortunately, one significant disadvantage is the lack of complexity. In comparison to the suggested design, the [8, 9] configurations need more switches. Configurations for both symmetrical and asymmetrical MLIs have already been described in [10], although the biggest disadvantage is the limited range of potential power factors. only sources with a voltage level near to uniformity can be used in provided. Two architectures depending onconstructed H-bridges are shown in [11,12]. The fundamental disadvantage of these architectures is that they generate a greater variety of distinct Dc voltage sources, which doubles their price.According to the previous research previous paragraph, to acquire a larger set of output stages including fewer devices, significant compromiseswere created in terms of total quantity of switching states, symmetric switches, Voltage sources, wide range of switches, different kinds of heating elements, variation of DC sources, efficiency, modifiability, straightforwardness, additivity, and switching failures.

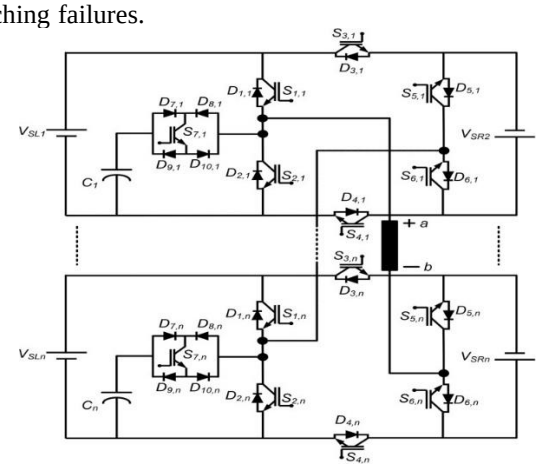

Fig. 1: Simulink model of Inverter

Here the paper [12] describes a symmetrical design that employs a one DC source is connected in seriesswith capacitors which are connected in series. The fundamental drawback is it can always be configured symmetrically. However, 4 of its switches must withstand the overall inverter voltage, limiting applicability to moderate voltage. Because its comment section is linked in a cascaded way, the architecture of [13] suggests a cascaded form of the configuration of [12] which can be performed at extreme supply voltages. To obtain optimum set of available levels, the topological of [12] was changed to an asymmetrical variant in [14]. The primary disadvantage of this architecture is the development of several switching devices. The topology was provided in [15] including symmetric MLI with larger amount of voltage levels. The biggest disadvantage is demand for a significant series of separate DC sources, that significantly drives up the price.

Table 1: Switching chart for 9-level invertermethod

Output level	Switch in g states	Impact level	
		ı>0	iı<0
*C*V	S4, S6, S7	discharging	Charging
*V*SR	S2, S4, S5	no effect	no effect
CV+VSR	S4, S5, S7	discharging	charging
VSL+VSR	S1, S4, S5	no effect	no effect
OV	S2, S4, S6	no effect	no effect
- (VSL+VSR)	S2, S3,S6	no effect	no effect

A phase angle modification approach is used to manage the capacitor voltage of a few of the CHB blocks in this architecture, that minimizes the chances of isolated DC sources by halves. The fundamental drawback of this design is whether its own major H-bridge switches must restrict the inverter's complete output voltage, limiting its use ingreater voltage applications. [16–19] suggest a filledU-cell structure, which significantly lowers the amount of discrete DC sources when compared to standard CHB. The fundamental benefit of such configurations is that they often not need any extra circuits to achieve a steady capacitor voltage. In [20],a new switching strategy for four leg NPC inverter is constructed by integrating harmonic distortion remediation and current harmonic abolition strategies, which somewhat minimizes power dissipation and yet also keeps the DC voltage level balanced with reduced voltage pulses even at reduced switching frequency range. [21] presentsMLI topologies that minimize the DC source demand by employing capacitors without any of the aid of an open circuit, that is the configurations of [21,22] possess balancing of its own voltage possibilities, number of switches are necessary for both topologiesin comparison to suggested configurations.

III.PROPOSED MLI TOPOLOGIES

Figure 1depicts the symmetrically arranged modified construction of architecture. Topology cells are made up of 7 regulated switches, 10 power diode, 2 DC supply, and a capacitor. The direct current sources on the left are labelled VSL1, VSL2..., VSLn,while the DC sources on the right are labelled VSR1,VSR2, VSRn.

Symmetrically arranged topology for 'N' cells, expressed mathematically.

1. Number of cells required for 9 level

N=(m-1)/8=(9-1)8=1 cell

2. Number of direct current sources

= 2*N = 2*1 = 2

3. Number of capacitors required = N = 1

4. Number of switches required

= N*7 = 1*7 = 7

5. Number of diodes =10 *N = 10*1= 10Where m = no. of levels = 9

9-level topological switching technique and the capacitor charging and discharging stages are shown above. The capacitor discharge voltage levels 'CV' and 'CV + VSR' for simple resistive loads, while charging occurs at voltage ranges 'CV' and '(VSL + VSR CV)'. The capacitor voltages are unaffected byanything else.

3.1Voltage Balancing

Regardless of the element, modulated signal or loadconditions, the capacitor voltage in the designedsystem is indeed equal. In addition, the suggested architecture does not necessitate any sophisticated ways for sustaining a healthy capacitor voltage. The capacitor amps balancing formula may be used to describe this behavior quantitatively; including this formula, the net difference in capacitor voltage more than a single switching cycle should be neutralgiven steady - state conditions. The instantaneous capacitor current flowing through the capacitor is calculated as follows.

$$I_c(t) = c\frac{dvc(t)}{dt} \quad (1)$$

$$\int_0^{Ts} Ic(t)dt = C\int_0^{Ts}\frac{dv_C(t)}{dt} \quad (2)$$

$$\int_o^{Ts} Ic(t)dt = Vc(t) - Vc(0) \quad (3)$$

From equation 3, the net difference in capacitor voltage during a one switching cycles equivalent to the sum of capacitor current across the same switching cycle.

Hence,

Average capacitor current= $\frac{1}{Ts}\int_o^{Ts} Ic(t)dt=0$ (4)

IV. SIMULATION RESULTS

In case of sinusoidal pulse width strategies for 9 levelinverters, every carrier waveform is in out of phase with its neighbor carrier by 180 degrees (Fig a). Our main objective was to reduce the number of devices (switches and dc sources) as compared withconventional and newly developed topologies so wedesigned a circuit as given above. It consists of seven IGBT switches which are arranges as shown in figure5.5 the gating sequence is given in table abovewhich determines the output waveform. The load used is 40,80 ohms. The multicarrier signals with logic control pulse width modulation signal, this pulse signal triggers the gate of IGBT and the nine-step output voltage waveform can be obtained.

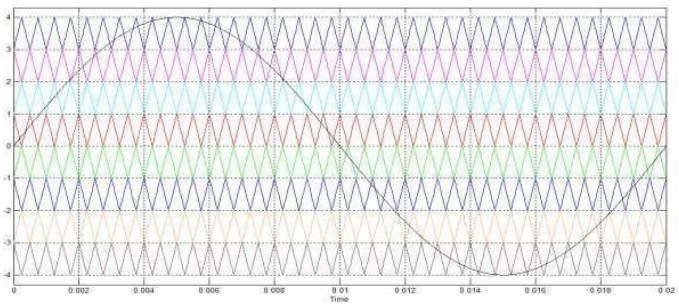

Fig 2: Sinusoidal pulse width strategies for 9 level inverters.

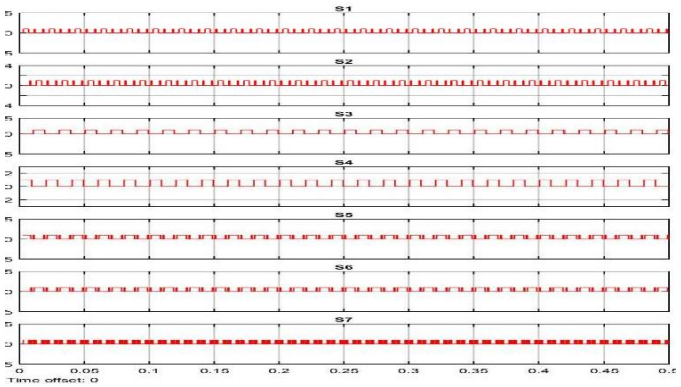

Fig 3: Gate pulses for respective switches for 9level.

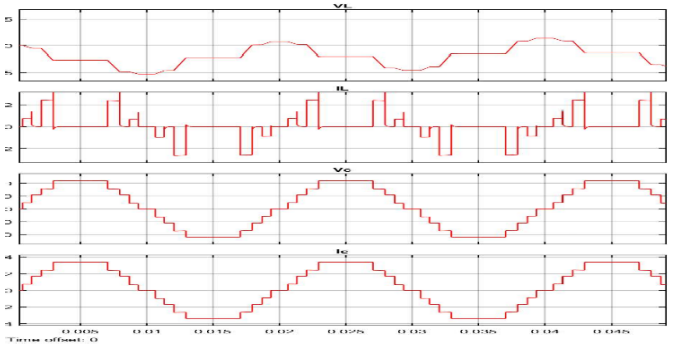

Fig 4:Simulink result for 9 level inverter for proposed method

V.CONCLUSION

The output is obtained in steps by applying 90V dc to each different voltage source used in the circuit. So, the first step is of 45V second step is of 90V andthird step is of 135V and the fourth step is of 180V as shown in figure 5.7. Similarly in the negative sidewe geta total of 180V. So, the voltage in each step is 45V for first step, 90V for second step, 135V for the third, 180V for fourth step and the final step is in the negative section.

Using go to label the gate signal is sent to the main circuit. And after running the programmed get our expected output in Scope block.

REFERENCE

[1] Mohd.Sami, M.A.Mallick. “Cascaded H-Bridge 11-level Multilevel Inverter “International Journal of Engineering Research & Technology (IJERT) Volume 10, Issue 06 (June 2021).

[2] Stephen, P. Moses, M. Ponraj, N. Sathesh, K. Balamurugan, and K. Karthikeyan. "Modified cascaded H-bridge multilevel inverter for household appliances." *power* 5, no. 03 (2018)

[3] Aditya Vardhan Singh, Ravi Shankar Singh, “A Comparative Study of Multilevel Inverter Topologies”. International Journal of Engineering Research & Technology (IJERT)Volume 5.Issue 03 (March 2018).

[4] M. F. Kangarlu and E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Submultilevel Inverters," in IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 625-636, Feb. 2013.

[5] Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., et al.: ‘Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components’, IEEE Trans. Ind. Electron., 2014, 61, (10), pp. 5300–5310

[6] Najafi, E., Yatim, A.H.M.: ‘Design and implementation of a new multilevel inverter topology’, IEEE Trans. Ind. Electron., 2012, 59, (11), pp. 4148–4154

[7] Gupta, K.K., Jain, S.: ‘A novel multilevel inverter based on switched DC sources’, IEEE Trans. Ind. Electron., 2014, 61, (7), pp. 3269–3278

[8] Babaei, E., Gowgani, S.S.: 'Hybrid multilevel inverter using switched capacitor units', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4614–462
[9] Mokhberdoran, A, Ajami, A: 'Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology', IEEE Trans. Power Electron., 2014, 29, (12), pp. 6712–6724
[10] Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., et al.: 'Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components', IEEE Trans. Ind. Electron., 2014, 61, (10), pp. 5300–5310
[11] Babaei, E., Alilu, S., Laali, S.: 'A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge', IEEE Trans. Ind. Electron., 2014, 61, (8), pp. 3932–3939
[12] Babaei, E., Laali, S., Alilu, S.: 'Cascaded multilevel inverter with series connection of novel H-bridge basic units', IEEE Trans. Ind. Electron., 2014, 61, (12), pp. 6664–6671.
[13] Rahim, N.A., Elias, M.F.M., Hew, W.P.: 'Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing', IEEE Trans. Ind. Electron., 2013, 60, (8), pp. 2943–2956.
[14] Elias, M.F.M., Abd Rahim, N., Ping, H.W., et al.: 'Asymmetrical cascaded multilevel inverter based on transistor-clamped H-bridge power cell', IEEE Trans. Ind. Appl., 2014, 50, (6), pp. 4281–4288.
[15] Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., et al.: 'Reduction of power electronic elements in multilevel converters using a new cascade structure', IEEE Trans. Ind. Electron., 2015, 62, (1), pp. 256–269.
[16] Vahedi, H., Labbé, P.A., Al-Haddad, K.: 'Sensor-less five-level packed U-cell (PUC5) inverter operating in stand-alone and grid-connected modes', IEEE Trans. Ind. Inf., 2016, 12, (1), pp. 361–370.
[17] Vahedi, H., Al-Haddad, K.: 'Real-time implementation of a seven-level packed U-cell inverter with a low-switching-frequency voltage regulator', IEEE Trans. Power Electron., 2016, 31, (8), pp. 5967–5973.
[18] Vahedi, H., Al-Haddad, K., Ounejjar, Y., et al.: 'Crossover switches cell (CSC): a new multilevel inverter topology with maximum voltage levels and minimum DC sources. 39th Annual Conf. IEEE Industrial Electronics Society (IECON 2013), Vienna, 2013, pp. 54–59.
[19] Vahedi, H., Al-Haddad, K., Kanaan, H.Y.: 'A new voltage balancing controller applied on 7-level PUC inverter'. 40th Annual Conf. IEEE Industrial Electronics Society (IECON 2014), Dallas, TX, 2014, pp. 5082– 5087.
[20] Sharifzadeh, M., Vahedi, H., Sheikholeslami, A., et al.: 'Hybrid SHM–SHE modulation technique for a four-leg NPC inverter with DC capacitor self-voltage balancing', IEEE Trans. Ind. Electron., 2015, 62, (8), pp. 4890–4899.
[21] Wang, K., Li, Y., Zheng, Z., et al.: 'Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter', IEEE Trans. Ind. Electron., 2013, 60, (5), pp. 1943–1954.
[22] Chattopadhyay, S.K., Chakraborty, C.: 'A new multilevel inverter topology with self-balancing level doubling network', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4622–4631.
[23] N.B M and P. V, "IoT as a Platform for State-of-the-Art Load Modeling in Domestic Utility," 2021 Innovations in Power and Advanced Computing Technologies (i-PACT), 2021, pp. 1-6, doi: 10.1109/i-PACT52855.2021.96970