Multi Switching Techniques of Z Source Inverter based PMSM Drive

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Abstract:
This paper presents a modelling of permanent Magnet synchronous motor with Z-Source inverter, switched inductor (SL) Z-Source Inverter and switched capacitor (SC)Z-Source Inverter. Compared with classical ZSI, the proposed inverters (SLZSI and SCZSI) increases the voltage boost inversion ability and also very short through zero state is required to obtain high voltage conversion ratios and modified vector controlled scheme of the PMSM drive is developed by considering DC-link voltage boosting in order to reduces line harmonics, improves power factor and reliability, and extends output voltage range. Several simulation results obtained to verify the feasibility and effectiveness of the proposed system.

1. INTRODUCTION

HIGH-PERFORMANCE voltage- and current-source inverters (VSI and CSI) are widely required in various industrial applications such as servomotor drives, special power supplies, distributed power systems, and hybrid electric vehicles. However, the traditional VSI and CSI have been seriously restricted due to their narrow obtainable output voltage range, shoot-through problems caused by misgating and some other theoretical difficulties due to their bridge-type structures. The topology of the Z-source inverter [3] was proposed to overcome the problems in the traditional inverters in which the functions of the traditional dc–dc boost converter and the bridge-type inverter have been successfully combined. As shown in Fig. 1, the impedance network of the Z-source inverter consists of split inductors L_1 and L_2 and capacitors $C_1$and C_2 connected in X-shape. An extra shoot-through zero state of the top and bottom arms is thus introduced into the switching actions, and results in a boost factor *B*, by which the conversion

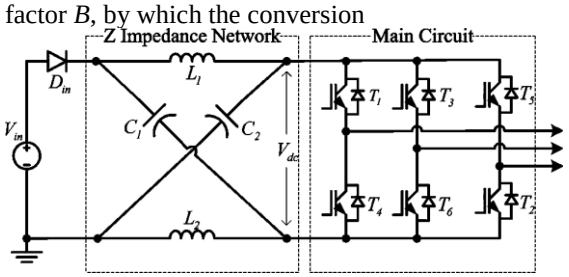


Fig-1 Z-Source inverter

From (1), it is seen that D is limited to the range from minimum value zero to the maximum value 0.5 in which the impendence network can perform the step-up dc–dc conversion from V_{in} to V_{dc}. For the practical applications, in order to provide a very high boost factor for the low-voltage dc energy source, usually a large value of D needs to be taken, i.e., the Z-source converter would have to be operated under the extreme condition of a long interval of the shoot-through zero state. Here, we take the classical synchronized pulse width modulation (SPWM) control strategy as the example for the brief discussion on the output power quality, and consequently, the modulation index of the main circuit M will be decreased to a very low level, and the numerical relation can be expressed by

$$M \leq 1 - D \quad (2)$$

Where

M= (Amplitude of the modulation waveform/Amplitude of the carrier waveform)

Unfortunately, the constraint of low M and high D will cause a new conflict of the output power quality and system boost inversion ability. M has a linear relation to the magnitude of the output voltage at the fundamental frequency. Beside M, the modulation ratio p, defined as the ratio of the carrier frequency over the modulation frequency, is also related to the power quality. The harmonics usually appear in clusters with main components at frequencies of n_p (n = 1, 2, 3, . . .). Therefore, on performing the harmonics computation by Fourier series, we can draw the harmonics spectra as shown in Fig. 2 for a qualitative observation.

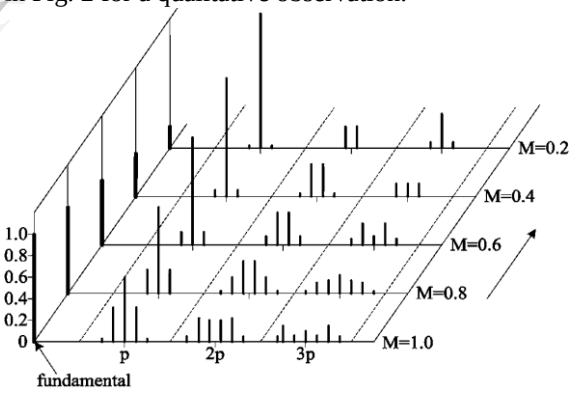


Fig:2 Normalized harmonic amplitudes for SPWM Z-source inverters.

According to the results in Fig. 2, the condition of low M will result in a poor inversion ability at the fundamental frequency with high total harmonic distortion values, and consequently, the final ac output performance will be degraded significantly. For an optimum system design of the Z-source inverter, the practical values of M have to be made close to 1, and D has a small upper limit according to (2). Therefore, the practical boost factor of Z-source impedance network is usually restricted seriously by (1). With the fast development of modern technologies, the aforementioned disadvantage might be obvious and will limit the further applications of the Z-source inverter in some areas that require the strong boost inversion abilities

for low-voltage energy sources such as fuel cells, batteries, and photovoltaic systems [6].

In recent years, advanced dc-dc conversion enhancement techniques such as switched capacitor (SC), switched inductor (SL), hybrid SC/SL, voltage multiplier cells and voltage lift techniques have been greatly explored [12]–[19], which are used to get the high step-up capacity in transformer less and cascade structures. The main objective is to reach a high efficiency, high power density, and simple structures. Therefore, the combination with the Z-source inverter and advanced dc–dc enhancement techniques could be a good solution for improving impedance-type inverters' performance and promoting their further industrial applications. It is necessary for the drive system of EV to have wide operation range that is from stand still to high speed running. Although motors with different structures have been used to propel the vehicles, the permanent magnet synchronous motors (PMSM) have become more and more attractive because of their high efficiency, high power density, and high reliability [1-2]. However, these motors inherently have a short constant-power region due to their rather limited field weakening capability. In order to increase the speed range, two main control schemes have been discussed in past works. The most popular one is the field weakening control in the high-speed region [1], but it needs additional current to reduce the magnet flux of the motor. The other one is a DC-link voltage control method. In references [3]-[4], PMSM drive system with a boost converter in series with the PWM inverter to change the DC-link voltage above the rated speed has been discussed.

However, this two-stage system increases not only the complexity of circuitry and control but also the cost and the space requirement. Meanwhile there are several defects in the traditional voltage source inverter.

In this paper, a complete PMSM drive system with bidirectional ZSI, SLZSI and SCZSI has been proposed. Then, the steady state operating principle of Z-Source inverter ,switched inductor(SL)Z-Source Inverter and switched capacitor (SC)Z-Source Inverter, the voltage boosting control scheme and modified vector controlled scheme for the PMSM drives are presented. Comparing the speed –torque results to obtain a effective technique to reduce the line harmonics increase the boosting factor and modulation ratio.

In this paper, the concept of the SL and SC techniques has been integrated into the classical Z-source impedance network, and consequently, a new SL and SC Z-source impedance network with PMSM is proposed. The newly obtained topology is then termed the SL Z-source inverter and the SC Z-source inverters are shown in Fig. 3 and Fig 4 respectively. This topology is totally different from any other existing Z-source inverters from the viewpoint of circuit structures and operation principles. The main characteristics are summarized in the following.

1) The basic X-shape structure is retained.
2) As for the high power quality and high boost inversion ability, their conflict caused byM and D has got an initial solution.
3) Only six diodes and two inductors are added compared to the classical Z-source inverter.

All reference directions of currents and voltages can be referred to in the corresponding figures. For any component *X*, its instantaneous current and voltage are expressed as *iX* and *vX* . Its average current and voltage during a switching cycle in the steady state are expressed as *IX* and *VX* . The corresponding peak value is represented by the small letter with a hat symbol.

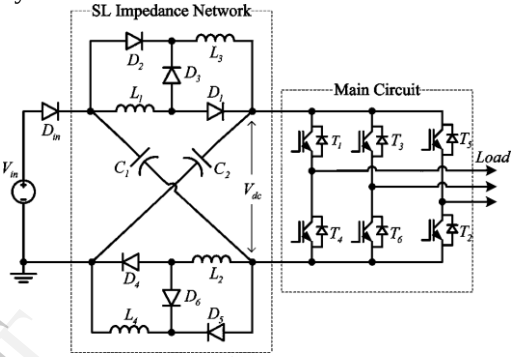


Fig3: Topology of proposed SL Z-Source Inverter

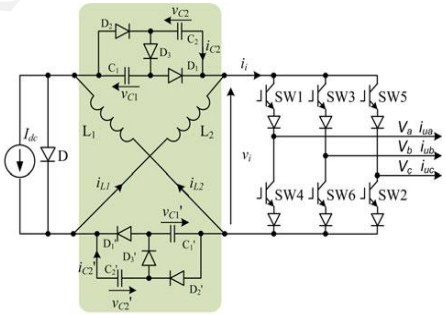
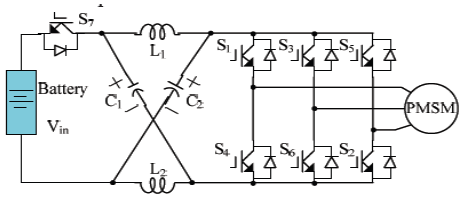


Fig4: Topology of proposed SC Z-Source Inverter

2. ZSI WITH PMSM DRIVE

a)Principle of operation:

Fig.4 shows the configuration of the proposed drive system, which consists of a battery pack, an impedance network, a conventional voltage-source inverter and a PMSM. The impedance network consists of two identical inductors and two identical capacitors connected in a specific manner to achieve the desired properties. The additional switch S7 is installed anti parallel to the input diode to eliminate the undesirable operation modes caused by inductor current discontinuous, and enables the system have the ability of bidirectional power flow.



Z-source inverter can be operated in two modes, one is shoot through mode and another one is non-shoot through mode. the basic difference between VSI and ZSI is VSI has only 8 switching states where as in ZSI has 9 switching states. Fig. 2 shows the equivalent circuit of the Z-source inverter shown in Fig. 1 when viewed from the dc link. The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Fig. 3, whereas the inverter bridge becomes an equivalent current source as shown in Fig.4 when in one of the six active states. Note that the inverter bridge can be also represented by a current source with zero value (i.e., an open circuit) when it is in one of the two traditional zero states. Therefore, Fig. 4 shows the equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight non-shoot through switching states.

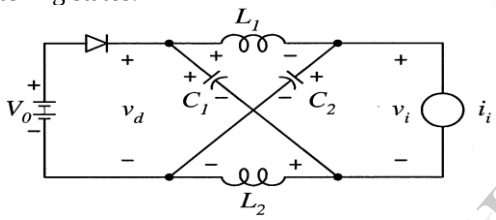


Fig-5Equivalent circuit of the Z-source inverter viewed from the dc link.

In shoot through state

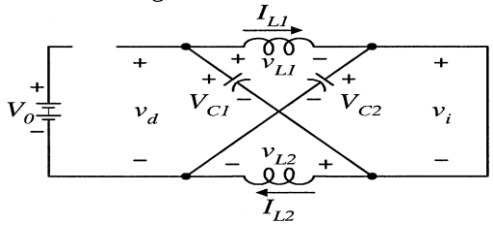


Fig.6. Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight shoot-through switching states Vdc

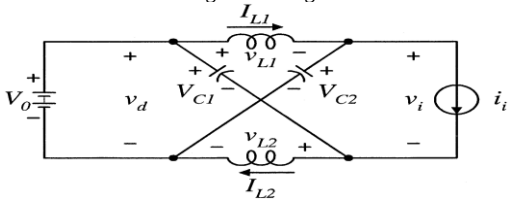


Fig.7. Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight nonshoot-through switching states.

b) Circuit analysis :

Assuming that the inductors L_1 and L_2 capacitors $C_1$and C_2 have the same inductance and capacitance, respectively, the Z-source network becomes symmetrical. From the symmetry and the equivalent circuits, we have

$$V_{C1}=V_{C2}=V_C;\ VL1=V_{L2}=V_L$$

Given that the inverter bridge is in the shoot-through zero state for an interval T_O , during a switching cycle T, and from the equivalent circuit, Fig. 6, one has

$$v_l= v_c \quad V_d=2\ v_c \quad V_i=0$$

Now consider that the inverter bridge is in one of the eight non-shoot through states for an interval of T1, during the switching cycle, T . From the equivalent circuit, Fig.7, one has

$$V_L=V_0-V_C\ ;\ V_d=V_0;\ V_i=V_C-V_L=2V_C-V_0$$

The average voltage of the inductor over one switching period is zero.then,we have

$$V_L=\overline{v_L}=\frac{T_o.V_C+T_1(V_O-V_C)}{T}=0$$

$$\frac{V_C}{V_O}=\frac{T_1}{T_1-T_o}$$

Where Do is the shoot through time duty ratio And B is the boosting factor Vin is the source voltage V_{dc} is peak DC link voltage across the inverter bridge

3. SLZSI WITH PMSM DRIVE

a. Principle of operation:

The proposed SL Z-source inverter consists of four inductors (*L*1, *L*2, *L*3 , and *L*4), two capacitors (*C*1 and *C*2), and six diodes (*D*1,*D*2,*D*3,*D*4,*D*5 , and *D*6). The combination of *L*1–*L*3–*D*1–*D*3–*D*5 and the combination of *L*2–*L*4–*D*2–*D*4–*D*6 performs the function of the top SL cell and the bottom SL cell, respectively. Both of these two SL cells are used to store and transfer the energy from the capacitors to the dc bus under the switching action of the main circuit.

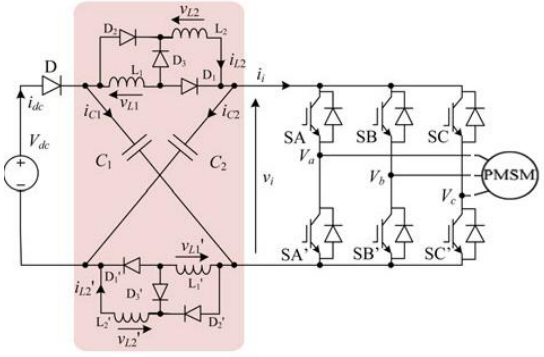


Fig-8 SL ZSI with PMSM Drive

b. Operation Principles

From the viewpoint of the switching states of the main circuit connected with SL impedance network, the operation principles of the proposed impedance network are similar to those of the classical Z-source impedance network. For the convenience of analysis, the equivalent circuit of the proposed impedance network viewed from the dc bus is shown in Fig. 4 in which a virtual active switch *S* and a passive switch *Do* are introduced to simulate the practical shoot-through actions of the top and bottom arms. Therefore, the substates of the proposed impedance network are classified into the shoot-through state and the non-shoot through state, respectively.

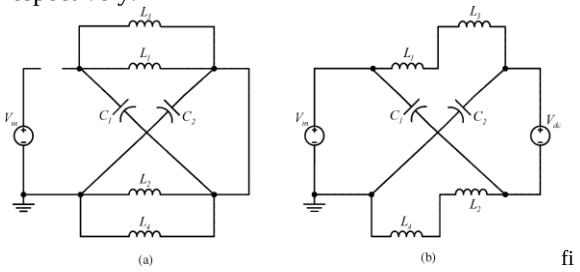


fig:9 Equivalent circuits. (a) Shoot-through zero state (i.e., switching ON). (b) Non-shoot-through states (i.e., switching OFF).

1) Shoot through state

During this sub state, *S* is ON, while both *D*in and *Do* are OFF. For the top SL cell, *D*1 and *D*2 are ON, and *D*3 is OFF. *L*1 and *L*3 are charged by *C*1 in parallel. For the bottom SL cell, *D*4 and *D*5 are ON, and *D*6 is OFF. *L*2and *L*4 are charged by *C*2 in parallel. This state corresponds to the additional zero state produced by the shoot-through actions of the top and bottom arms, and its equivalent circuit is shown in Fig. 5(a). It is seen that both the top and bottom SL cells perform the same function to absorb the energy stored in the capacitor

2) Non-Shoot-Through State:

This state corresponds to the six active states and two zero states of the main circuit and the equivalent circuit is shown in Fig. 5(b). During this substate, *S* is OFF, while both *D*in and *Do* are ON. For the top SL cell, *D*1 and *D*3 are OFF, and *D*5 is ON. *L*1 and *L*2 are connected in series, and the stored energy is transferred to the main circuit. For the bottom SL cell,*D*4 and*D*5 are OFF, and*D*5 is ON. *L*3 and *L*4 are connected in series, and the stored energy is transferred to the main circuit. At the same moment, to supplement the consumed energy of *C*1 and *C*2 during the shoot-through state, *C*1 is charged by *V*in via the bottom SL cell, and *C*2 is charged

c. Circuit analysis of SL Z-Source impedance

For the convenience of mathematical derivation, all inductors and capacitors are assumed to have the same inductance (*L*) and capacitance (*C*), respectively; therefore, both the equivalent circuits in Fig. 5 show the symmetry characteristics. In addition, since *C*1 and *C*2 are sufficiently large, thus, in the steady state, we have

$$VC1 = VC2 = VC \quad (3)$$

The inductor current *iL*1 increases during switching ON and decreases during switching OFF. During switching ON, the corresponding voltage across *L*1, *VL*1-ON is equal to V_C . Applying the volt–second balance principle to *L*1, we can get the corresponding voltage across *L*1 during switching OFF, *VL*1-OFF, which is expressed by

$$VL1\text{-OFF} = -(D/(1-D))VC = VL3\text{-OFF}$$

The inductor current *iL*3 increases during switching ON and decreases during switching OFF. The corresponding voltages across *L*3 are equal to *VC*1 and −(*VC*2 − *V*in + *VL*1-OFF).

Applying the volt–second balance principle to *L*3, we have

$$DTVC1 = (1-D)T(VC2 - Vin + VL1\text{-OFF}) \text{ or}$$
$$DTVin = (1-D)T(VC - Vin - (D/1-D)VC)$$

Hence,

$$VC = (1-D/1-3D)Vin = VC1 = VC2 .$$

During switching OFF, *C*1, *L*1, *L*3, and the voltage source *V*dc form a close loop; therefore we have

$$VC = Vdc + VL1\text{-OFF} + VL3\text{-OFF}.$$

Therefore, averaging v_L over a switching period to zero then gives rise to the following governing expressions for the capacitor voltage V_c, peak dc-link voltage $\hat{v}_i$, and peak ac output voltage $\hat{v}ac$, in terms of the source voltage V_{dc}:

$$V_C = \frac{1-d_{ST}}{1-3d_{ST}} V_{dc}$$

$$\hat{v}_i = \frac{1+d_{ST}}{1-3d_{ST}} V_{dc}$$

$$\hat{v}_{ac} = \frac{M(1+d_{ST})}{1-3d_{ST}} \frac{V_{dc}}{2}$$

where M ≤ 1.15 and dST < 1/3 represent the VSI modulation ratio after adding triplen offset and normalized shoot through time per switching period, respectively. The boost ratio B can then be written as $B = (1 + dST)/(1-3d_{ST})$, which is larger than B = 1/(1 − 2dST) of the traditional Zsource inverter.

4. SCZSI WITH PMSM DRIVE

The proposed SC Z-source inverter consists of four capacitors (*C*1, *C*2, *C*3 , and *C*4), two inductors (*L*1 and *L*2), and six diodes (*D*1,*D*2,*D*3,*D*4,*D*5 , and *D*6). The combination of *C*1–*C*3–*D*1–*D*3–*D*5 and the combination of *C*2–*C*4–*D*2–*D*4–*D*6 performs the function of the top SC cell and the bottom SC cell, respectively. Both of these

two SC cells are used to store and transfer the energy from the capacitors to the dc bus under the switching action of the main circuit

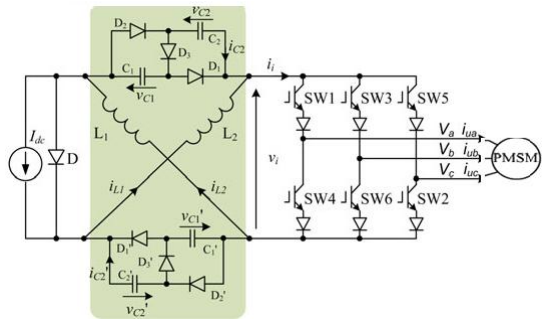


Fig-10 SCZSI with PMSM Drive

The resulting SC topology can still assume two distinct states, whose operating features and expressions are written as follows:

1) Open Circuit:

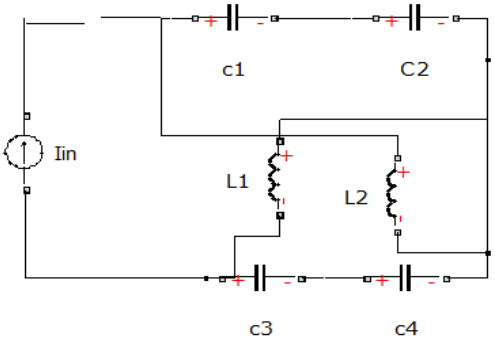


Fig-11 shoot through state

Introduced by turning OFF all switches of the CSI bridge, causing diodes D, D_3 And D_3 to conduct naturally on the contrary, diodes D1, D2, D1, and D2 block naturally. The resulting circuit consists of two series-connected capacitors per SC cell with their currents indicated as

$i_C = i_{C1} = i'_{C1} = i_{C2} = i'_{C2} = I_{L1} = I_{L2} = I_L$.

2) Non open Circuit:

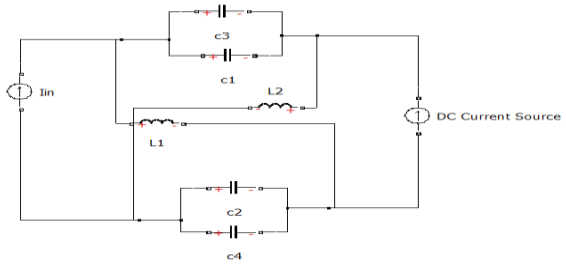


Fig-11 Non-Shoot through

Averaging the capacitive current to zero per switching cycle then results in the following equations for relating the network inductive current IL , peak dc-link current ˆıi , and peak ac output current ˆıac with the input current I_{dc}:

$$I_L = \frac{1-d_{OC}}{1-3d_{OC}} I_{dc}$$

$$\hat{i}_i = \frac{1+d_{OC}}{1-3d_{OC}} I_{dc} \cdots$$

$$\hat{I}_{ac} = \frac{M(1+d_{OC})}{1-3d_{OC}} \frac{I_{dc}}{2}$$

where M' ≤ 1.15 and d_{OC} < 1/3 represent the CSI modulation ratio and normalized open-circuit duration per switching period, respectively. The computed current boost factor of B'= (1 +d_{OC})/(1 − 3d_{OC}) is again larger than that of B'= 1/(1−2d_{OC}) of the traditional current-type Z-source inverter

5. COMPARISION OF ZSI WITH PROPOSED *TECHNIQUES*

The current stresses of the impedance-type power converters are different under different control and load conditions. For the purpose of comparison, both the proposed inverter and the classical Z-source inverter are represented by the simplified equivalent circuit as shown in Fig. Different from Fig. 4, an inductive load impedance (Z_l=R_l+ sL_l) is paralleled with S directly in As for the proposed inverter, the inductor currents IL1–

TABLE I: STRESS COMPARISON IN THE CASE OF THE SAME *D* AND *Vin*

	SL Topology	Classical Z-source inverter
V_{dc}	$\frac{1+D}{1-3D}V_{dc}$	$\frac{1}{1-2D}V_{in}$
V_c	$\frac{1-D}{1+D}V_{dc}$	$(1-D)V_{dc}$
V_{oc}	V_{dc}	V_{dc}
I_{oc}	$2I_L - I_1$	$2I_L - I_1$
I_1	$(1-D)\frac{V_{dc}}{R_1}$	$(1-D)\frac{V_{dc}}{R_1}$
I_L	$\frac{(1-D)^2}{1-3D}\frac{V_{dc}}{R_1}$	$\frac{(1-D)^2}{1-2D}\frac{V_{dc}}{R_1}$

TABLE II: STRESS COMPARISON IN THE CASE OF THE SAME *D* AND *Vin*

	Switched capacitor topology	Classical Z-Source inverter
Idc	$\hat{I}_{dc} = \frac{M(1+d_{OC})}{1-3d_{OC}} \frac{I_{dc}}{2}$	IL = $\frac{M}{1\text{-}2D} \cdot \frac{Idc}{2}$
IL	$I_L = \frac{1-d_{OC}}{1-3d_{OC}} I_{dc}$	IL = $\frac{1}{1\text{-}2D}$ Idc
Idin	$\hat{i}_i = \frac{1+d_{OC}}{1-3d_{OC}} I_{dc}$	Ii = $\frac{1}{1\text{-}2D} \cdot \frac{Idc}{2}$
VDin VC Vi	2VC-Vin (1-D)Vdc $\frac{(1\text{-}D)^2 Vdc}{1\text{-}3D}$	2VC-Vin (1-D)Vdc $\frac{(1\text{-}D)^2 Vdc}{1\text{-}2D}$

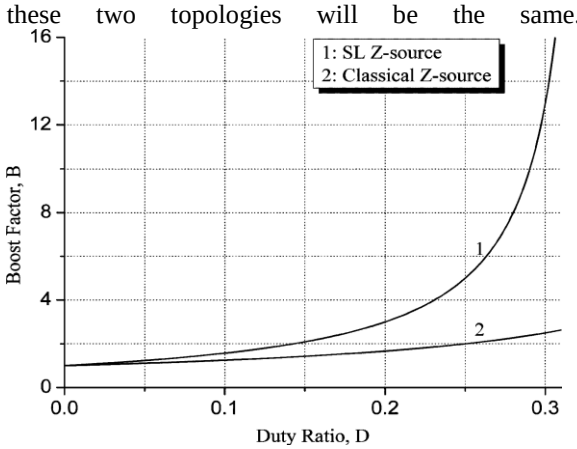
*IL*4 are the same and can be expressed by *IL* for the convenience of analysis. The tedious computation is thus avoided.

Applying the steady-state analysis method i to Fig. 1 we can obtain the voltage and current stresses of the main components (passive power switch *D*in , *L*, *C*, and dc link) and tabulated them in Table I. The results in Table I are based on the assumption that both of these two inverters are working in the case of the same *D* and *V*in. Consequently, it can be known that the proposed inverter has the higher voltage and current stresses due to its stronger voltage boost ability. When the proposed inverter is used to replace the classical Z-source inverter in a particular case, V_{dc} and V_{in} are usually fixed. If we assume that the detailed value of *D* in the classical Z-source inverter is *k*, the corresponding *D* in the proposed inverter should be *k*/(2 − *k*) so as to obtain the same V_{dc}. Correspondingly, the voltage and current stresses are tabulated in Table III.

TABLE III: STRESS COMPARISON IN THE CASE OF THE SAME *D* AND *V*in

	Proposed Topology	Classical Z-source Inverter
V_{dc}	$\frac{1}{1-2k} V_{in}$	
V_C	$(1-k)V_{dc}$	
V_{Din}	V_{dc}	
I_{Din}	$2I_L$-I_I	$2I_L$-I_I
I_I	$\frac{2}{(2-k)} I_{in}$	I_{in}
I_L	$\frac{2}{2-k} I_{Lin}$	I_{Lin}

It is seen from Table III that the voltage stresses of the proposed inverter are the same to those of the classical Z-source inverter. The current stresses have a rise for the same load impedance, which indicates that the proposed inverter has a stronger power processing capability. If the condition of the same load currents is considered, the current stresses of these two topologies will be the same.



Boost ability comparison of the classical Z-source impedance network and the proposed SL Z-source impedance network

TABLE IV: COMPARISION OF SL & SC TOPOLOGY

SL TOPOLOGY		SC TOPOLOGY	
Boost Factor = $\frac{1+Nd_{ST}}{1-(N+2)d_{ST}}$		Boost Factor = $\frac{1+Nd_{OC}}{1-(N+2)d_{OC}}$	
Conventional Capacitor voltage= $\frac{1-d_{ST}}{1-(N+2)d_{ST}} V_{dc}$	Embedded Capacitor voltage= $\frac{1+Nd_{ST}}{1-(N+2)d_{ST}} \frac{V_{dc}}{2}$	Conventional Inductor Current= $\frac{1-d_{OC}}{1-(N+2)d_{OC}} I_{dc}$	Embedded Inductor Current= $\frac{1+Nd_{OC}}{1-(N+2)d_{OC}} \frac{I_{dc}}{2}$
Output Peak Voltage= $\frac{M[1+Nd_{ST}]}{1-(N+2)d_{ST}} \frac{V_{dc}}{2}$		Output Peak Voltage= $\frac{M[1+Nd_{OC}]}{1-(N+2)d_{OC}} \frac{I_{dc}}{2}$	
Diode Voltages: Diode D: $V_D = -\hat{g}_i = \frac{1+Nd_{ST}}{1-(N-2)d_{ST}} \frac{V_{dc}}{2}$ Diodes D_{2n-1}, D_{2n-2}: $V_{D1} = \frac{d_{ST}}{1-(N+2)d_{ST}} V_{dc}$ Diode D_{2n}: $V_{D2} = \frac{1-d_{ST}}{1-(N+2)d_{ST}} V_{dc}$		Diode Currents: Diode D: $V_D = -\hat{g}_i = \frac{1+Nd_{OC}}{1-(N-2)d_{OC}} \frac{V_{dc}}{2}$ Diodes D_{2n-1}, D_{2n-2}: $V_{D1} = \frac{d_{OC}}{1-(N+2)d_{OC}} V_{dc}$ Diode D_{2n}: $V_{D2} = \frac{1-d_{OC}}{1-(N+2)d_{OC}} V_{dc}$	

6. PMSM DRIVE SYSTEM

For a PMSM, the steady state voltage equation in the rotor reference frame is

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} R+pL_d & -\omega_e L_q \\ \omega_e L_d & R+pL_q \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \lambda_{pm} \end{bmatrix}$$

where v_{sd} , v_{sq} , i_{sd} and i_{sq} are d- and q-axis voltages and currents respectively, R , L_d , and L_q are motor armature resistance, d- and q-axis inductances respectively, and ω_e and λ_{pm} are electrical angular frequency and PM flux linkage respectively. In practice, considering the motor maximum line current amplitude and maximum available voltage, one can form the following constraints

$$i_{sd}^2 + i_{sq}^2 \le i_{s\max}^2$$

$$v_{sd}^2 + v_{sq}^2 \le v_{s\max}^2$$

Substituting above equations, the derivative operator becomes zero in the steady state, and neglecting the armature resistance drop for high-speed operation, one can obtain an equivalent voltage constraint as

$$(L_q i_{sd})^2 + (L_d i_{sq} + \lambda_{pm})^2 \le v_{s\max}^2 / \omega_e^2$$

Generally, as the DC-link voltage of inverter keeps constant, will also keep constant. As is larger than the rated speed of motor, a field weakening strategy should be used to provide the motor a high speed operation as the constant is used. However, the corresponding current amplitude will increase such that the copper loss will increase.

a. Parks Transformation and Dynamic d q Modelling

The dynamic d q modelling is used for the study of motor during transient and steady state. It is done by converting the three phase voltages an currents to d_{qo} variables by using Parks transformation

Converting the phase voltages variables v_{abc} to v_{dqo} variables in rotor reference frame the following equations are obtained

$$\begin{bmatrix} V_q \\ V_d \\ V_o \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta_r & \cos(\theta_r - 120) & \cos(\theta_r + 120) \\ \sin\theta_r & \sin(\theta_r - 120) & \sin(\theta_r + 120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} + \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Convert V_{dqo} to V_{abc}

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \cos\theta_r & \sin\theta_r & 1 \\ \cos(\theta_r - 120) & \sin(\theta_r - 120) & 1 \\ \cos(\theta_r + 120) & \sin(\theta_r + 120) & 1 \end{bmatrix} \begin{bmatrix} V_q \\ V_d \\ V_o \end{bmatrix}$$

7. SIMULATION AND EXPERIMENTAL VERIFICATION

Simulations in MATLAB/Simulink were next performed for classical, Voltage type SL, current type SC Z-source inverters. Input voltage to each inverter was set to 100V for eventually powering a Permanent Magnet Synchronous Motor Drive. The same control parameters of d_{ST}=0.15 and M =0.8×1.15 were used for all four cases with their results shown from Fig. . Observations noted from these figures is Peak dc-link voltages of the SL inverters are higher. Z-source inverter, while not overstressing any of its components. Similar observations would be applicable to the generalized SC inverter even though its comparison with other techniques is not possible because of either nonexistent or different operating principles.

Simulations were next repeated for all the 3 inverters to produce a graph for efficiency comparison. Relevant parameters read from datasheets and websites (Magnetics Inc., BHC Aerovox Ltd., Infineon Technologies AG, and International Rectifiers) and used for the loss computation were tabulated in Table II with some clarifications provided as follows:

1) topological parameters of the inverters were still kept as

$N_{Cas}=N + 1=\gamma_{TL}+1=\gamma_{TZ} = 3$;

2) inductors of the 3 inverters were wound with the same total number of turns to give roughly the same combined (magnetizing) inductance;

3) lower rated capacitors were used for the alternate cascaded inverter. Depending on how much cheaper the lower rated capacitors can be, their capacitances can be increased appropriately if needed (higher capacitance has lower equivalent series resistance);

4) losses of insulated gate bipolar transistors in the inverter bridge were obtained through simulation based on the method introduced in

The obtained plots are shown in Fig. 13-15, where it can be seen that efficiencies at higher gain with the generalized SL inverter have the highest and the trans-Z-source inverter having the lowest efficiency. The reason is likely due to the higher stresses tolerated by the latter, which can cause higher semiconductor switching losses and other resistive losses.

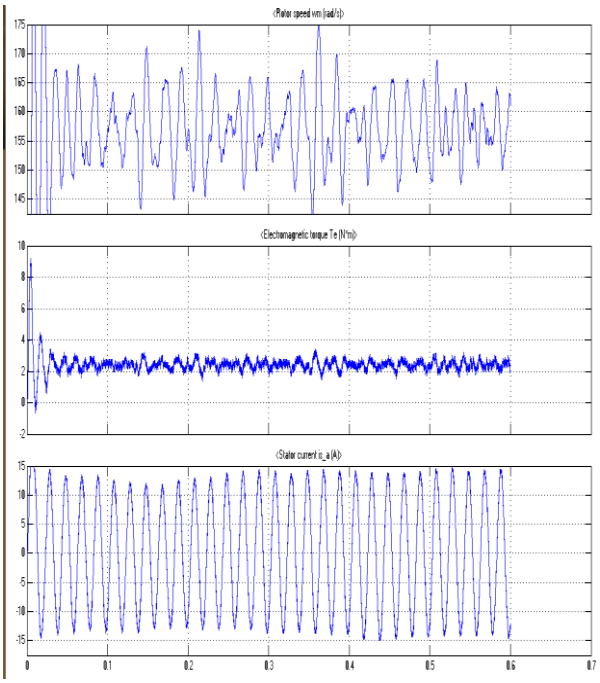


Fig13: OUTPUT FOR PMSM USING CLASSICAL Z_SOURCE INVERTER

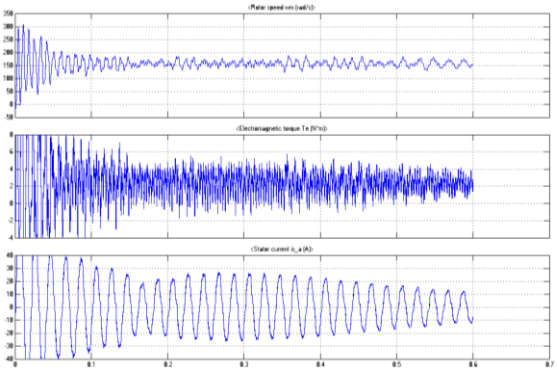
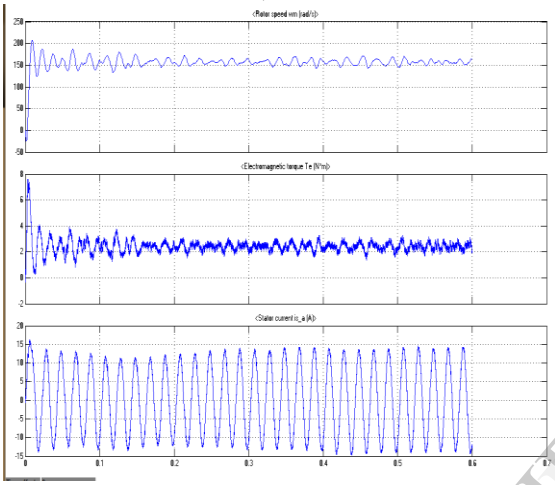
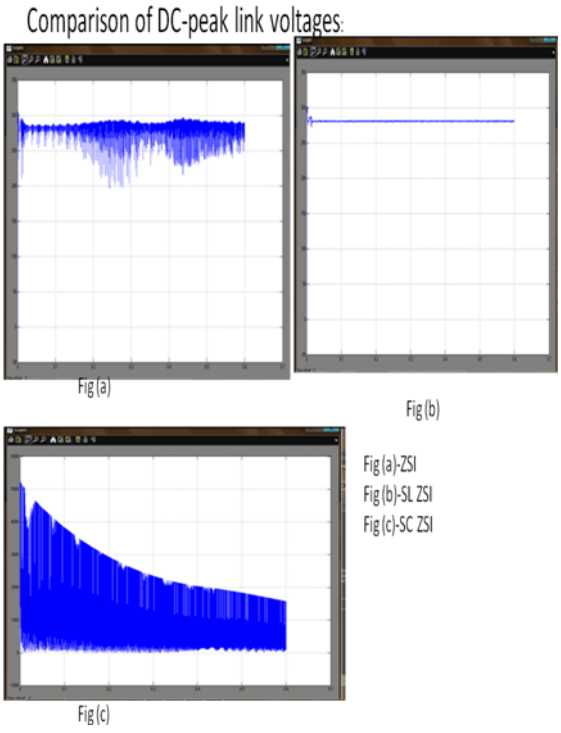


Fig14: OUTPUT FOR PMSM USING SC Z_SOURCE INVERTER



F

Fig15: OUTPUT FOR PMSM USING SL Z_SOURCE INVERTER



8. EXPERIMENTAL RESULTS

Experiments were first performed with the classical Z-Source inverter and compared with generalized SL Z-source inverter and SCZ-Source inverter shown in Fig.13 to 15. In total, four generic cells with six 3-mH inductors and two 2200-μF capacitors in SLZSI and two 3-mH inductors and six 2200-μF capacitors in SCZSI were used. The cells were inserted equally to the upper and lower dc rails, giving N = 2 and a computed boost factor of 3.25 according to (3) and a shoot-through duration of d_{ST}=0.15. The inverter was supplied from a 100-V dc source, and was connected to a PMSM Drive. Corresponding experimental waveforms are shown in Figs. 15 and 16 for a modulation ratio of M = 0.85x1.15 (1.15 introduced by the triplen offsets). Fig. 15 shows a dc-link voltage that switches between 0 and 300V, representing shoot through and non shoot-through states, respectively. The measured boost factor is thus 3, which is slightly lower than the computed value of 3.25 due to switching and component parasitic.

With comparing these dc-link voltages of ZSI, SLZSI and SCZSI is shown in fig 16.comparing with zsi peak dc link voltages in SLZSI and SCZSI the peak dc link voltages are ripple free. the measured ac peak current is 3 A, which again matches well with the computed value 0, where Z Load is the load impedance.

9. CONCLUSION

To understand the elementary SL topology, the generalized SL and SC Z-source inverters are derived. Their operating principles are explained with their gains proven to be much higher than those of the traditional Z-source inverters. Their modulation ratios can be set higher to better utilize their dc links, and to keep their component stresses lower. Simulations have confirmed these advantages, and experiments have verified the inverter practicalities.

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