Multi-Carrier PWM Strategies for Single Phase Asymmetric Cascade Binary Multilevel Inveter

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Abstract

This paper proposes a novel multi carrier pwm strategies based Single Phase asymmetric cascade binary DC source 7-level inverter topology which is capable of additive and subtractive combinations of input DC levels in output waveform. Though all such levels can be obtained using the proposed topology, the actual number of levels depends on the DC source arrangement .The Comparative analysis of Multi Carrier Pulse Width Modulating (MCPWM) strategies like Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy,and Alternate Phase Opposition Disposition (APOD) strategies are used for harmonic mitigation in proposed inveter. The performance measures like Total Harmonic Distortion (THD), VRMS (fundamental), crest factor (CF) and form factor (FF) are evaluated for various modulation indices. Simulation using Matlab Simulink used to verify the performance and result simulation shown than this proposed scheme can reach the goals.

Keywords: APOD, CF,FF,PD,POD, MCPWM,THD

1.Introduction

Recently multilevel inverters are gaining popularity and it has many attractive features. In particular, high voltage capability, reduced common mode voltages near sinusoidal outputs,lower value of dv/dt, smaller or even number output filters make multilevel inverter is a suitable topology for variable frequency induction motor drives and have recently been explored for low voltage renewable grid interfacing applications efficiency [1]. Krishna Kumar Gupta and Shailendra Jain [2] Introduced new concept in all additive and subtractive combinations of input DC levels in the multi level inveter output waveform. R.Seyezhai [3] introduced the variable frequency PWM techniques for asymmetric cascade multi level inverter. Mohamed Yousuf and P.Vijayadeepan Dr.S.Latha[4] developed modulation control techniques for single phase asymmetric multilevel inverter. Zahra Bayat, Ebrahim Babaei [5] proposed introduced number of switches reduced in cascade multi level inverter. C. R. Balamurugan,S. P. Natarajan, R. Bensr[6] proposed multi carrier control freedom angle (CFD) for multi level inveter.C.Govindaraju and Dr.K.Baskaran [7] designed A hybrid PDPWM controller for generate optimum gate pulses for power switches. M. R. Banaei and E. Salary [8] developed Cascaded Sub-Multilevel Cells for improve the output voltage quality of asymmetric multi level inverter Bambang, Sujanarko, Mochamad Ashar [9] proposed advanced carrier based pwm technique for multi level inverter.D.Balaji and R. Karthikeyan[10] designed less number of switches in multi level inverter.This paper presents a single phase binary seven level inverter topology for investigation with various MCPWM switching techniques. Simulations were performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

2.Basic Operation of Multilevel Inveter

Fig. 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing binary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 2Vdc, it can synthesize seven output levels; -3Vdc, -2Vdc, -Vdc, 0, Vdc,

2Vdc, 3Vdc.The lower inverter generates a fundamental output voltage with two levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$Vout = VHB1 + VHB2 \quad (1)$$

In the proposed circuit topology, if *n* number of H-bridge module has dependent input DC sources, an expected output voltage level is given as (2)

$$Vn = 2n + 1 \qquad n=1,2,3,.. \quad (2)$$

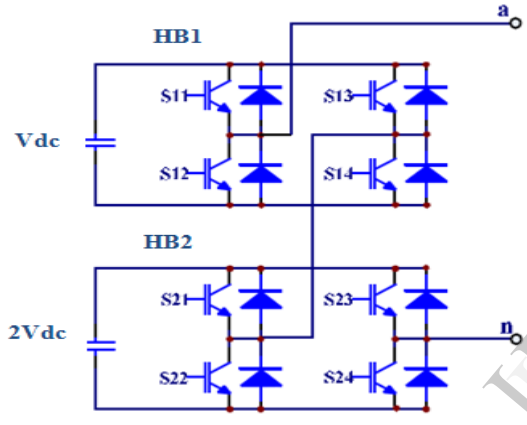

Fig.1. Binary 7 Level Inveter

3.Carrier Based PWM Methods

In this proposed work level shift Multi carrier PWM is used to generate firing pulses for a seven level inverter. For an m-level inverter using multi-carrier technique, (m-1) carriers with the same frequency fc and same peak-to-peak amplitude Ac are used. The reference waveform has amplitude Am and frequency fm and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off. There are many alternative strategies are possible, some of them are tried in this paper and they are:

a. Phase disposition PWM strategy.

b. Phase opposition disposition PWM strategy.

c. Alternate phase opposition disposition PWM strategy.

The formulae to find the a modulation indices are as follows:

The frequency modulation index

$$mf = fc/fm \quad (3)$$

The amplitude modulation index

$$ma = 2Am/ (m-1) Ac \quad (4)$$

where

fc – Frequency of the carrier signal

fm – Frequency of the reference signal

Am –Amplitude of the reference signal

Ac – Amplitude of the carrier signal

3.1.Phase Disposition PWM Strategy

This technique employs (m-l) carriers which are all in phase for a m level inverter. In seven level converter all the six carrier waves are in phase with each other across all the bands as described in Fig2. for a phase leg of a seven level cascaded Binary structure with ma = 1.

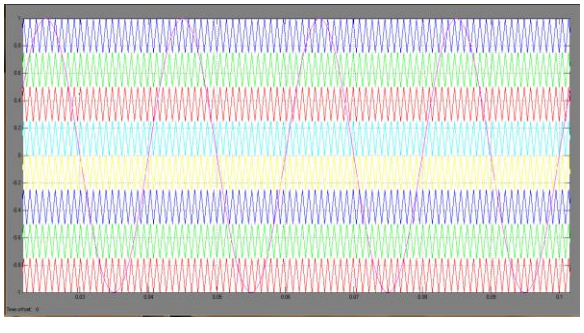

Fig.2.Reference and Carrier arrangement form PDPWM Strategy(Ma-1,Mf-40)

3.2.Phase Opposition Disposition PWM Strategy

This technique employs (m+1) carriers which are all in phase above and below the zero reference. In seven level converters all the six carrier waves above zero reference are phase shifted by 180 degrees

with the ones below zero reference. The PODPWM is explained in the Fig.3

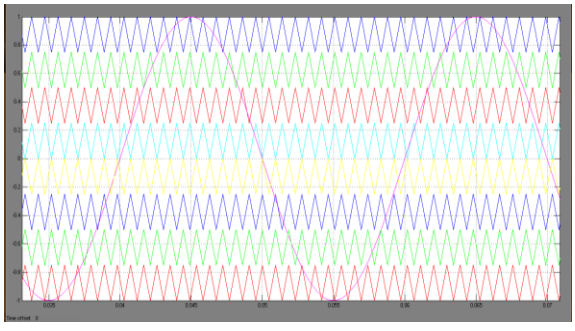

Fig.3.Reference and Carrier arrangement form PODPWM Strategy(Ma-1,Mf-40).

3.3.Alternate Phase Opposition Disposition PWM Strategy

This technique requires each of the m-l carrier waveforms for an m-level phase waveform to be phase displaced from each other by 180 degrees alternatively. The APODPWM is explained in the Fig.4.

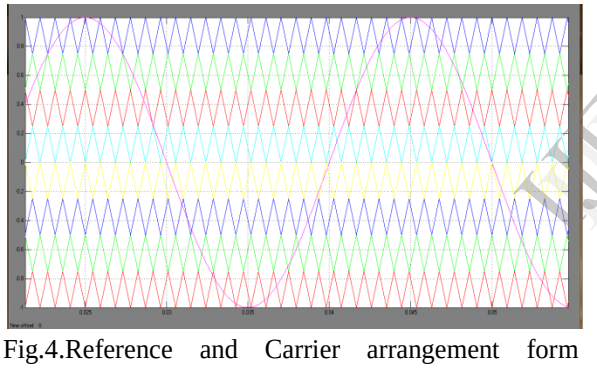

Fig.4.Reference and Carrier arrangement form APODPWM Strategy(Ma-1,Mf-40).

4. Simulation Results

The single phase Binary DC source seven level inverter is modeled in SIMULINK using power system block set. Switching signals for binary multilevel inverter using MCPWM strategies are simulated. Simulations were performed for different values of mI ranging from 0.8 to 1 and the corresponding %THD,Vrms,CF and FF are measured using the FFT block and their values are shown in Table (1 to 4). Figure 5 to11 show the simulated output voltage of binary MLI and their corresponding harmonic spectrum. Figure 5 displays the simulink model of the system. Figure 6 displays seven level output voltage generated by PDPWM strategy and its FFT plot is shown in Figure 7. Figure 8 shows the seven level output voltage generated by PODPWM strategy and its FFT plot is shown in Figure 9. Figure. 10 shows the seven level output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 11. For ma= 1.

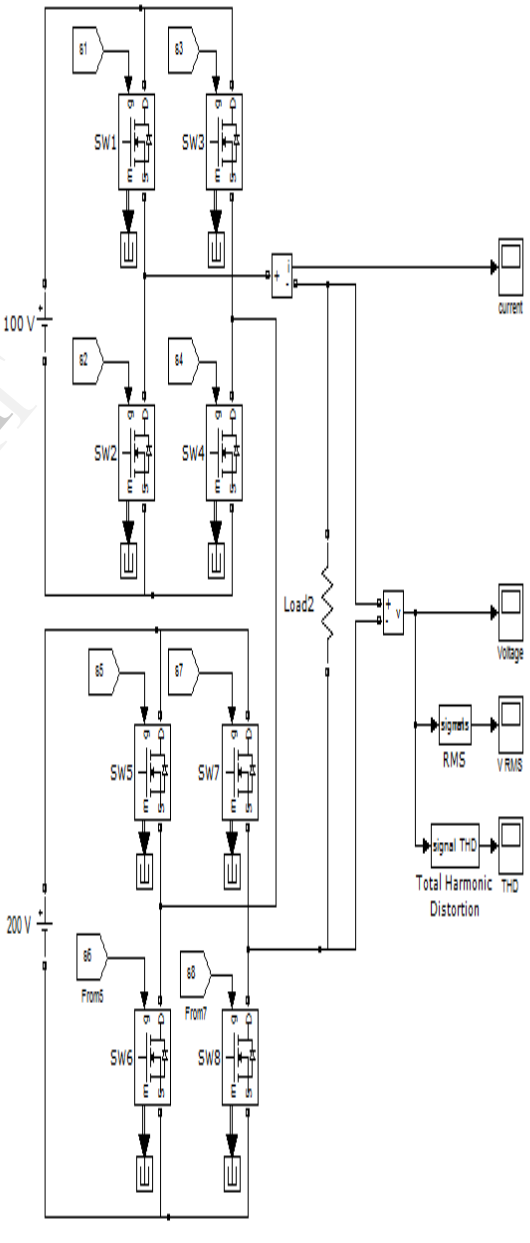

Fig.5.Simulink Model of the System.

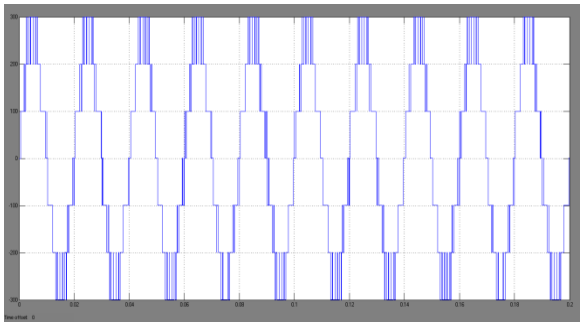

Fig. 6. Output voltage generated by PDPWM strategy

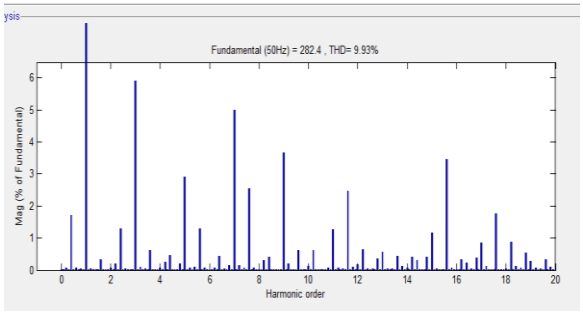

Fig. 7. FFT plot for output voltage of PDPWM strategy.

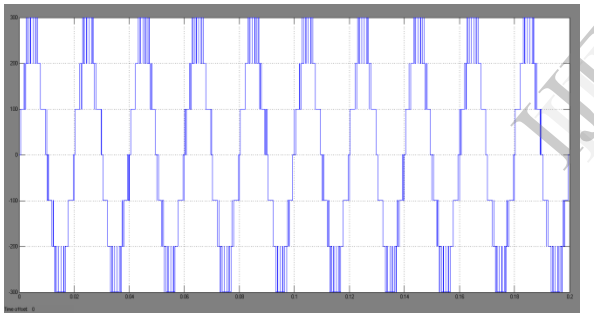

Fig. 8. Output voltage generated by PODPWM strategy.

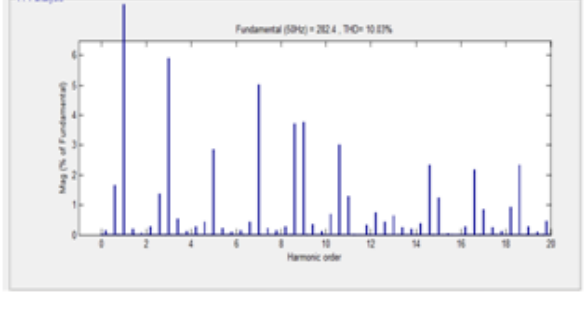

Fig. 9. FFT plot for output voltage of PODPWM strategy

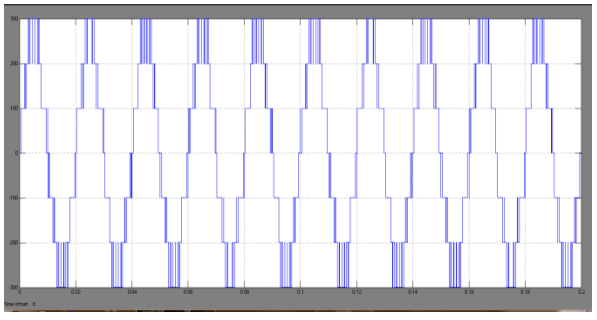

Fig. 10. Output voltage generated by APODPWM strategy.

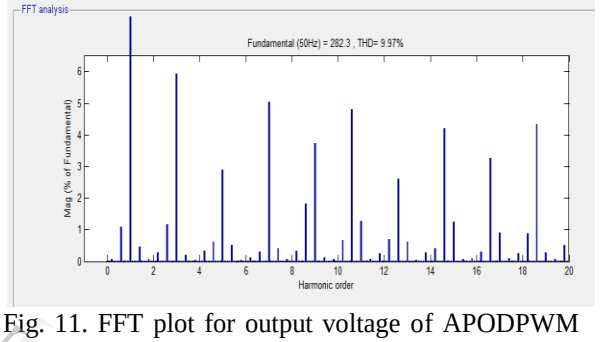

Fig. 11. FFT plot for output voltage of APODPWM strategy.

TABLE 1 .% THD FOR DIFFERENT MODULATION INDICES

MI	PD	POD	APOD
1	9.93	10.03	9.97
0.95	10.31	10.29	10.3
0.9	10.67	10.72	10.72
0.85	11.15	11.20	11.18
0.8	11.91	11.98	11.99

TABLE 2. VRMS FOR DIFFERENT MODULATION INDICES

MI	PD	POD	APOD
1	199.7	199.7	199.7
0.95	186.3	186.4	186.3
0.9	173.1	173	173.1
0.85	160.1	160.1	160.1
0.8	147.3	147.3	147.3

TABLE 3. CF FOR DIFFERENT MODULATION INDICES

MI	PD	POD	APOD
1	1.414	1.414	1.414
0.95	1.414	1.414	1.414
0.9	1.414	1.414	1.414
0.85	1.414	1.414	1.414
0.8	1.414	1.414	1.414

TABLE 4. FORM FACTOR FOR DIFFERENT MODULATION INDICES

MI	PD	POD	APOD
1	1.110	1.110	1.110
0.95	1.110	1.110	1.110
0.9	1.110	1.110	1.110
0.85	1.110	1.110	1.110
0.8	1.110	1.110	1.110

5.Conclusion

In this paper, Multi carrier PWM techniques for Binary DC source Seven level inverter have been presented. Binary DC source multilevel inverter gives higher output voltage with low harmonics. Performance factors like %THD, Vrms, CF and FF have been evaluated presented and analyzed. It is found that the PDPWM strategy provide lower %THD. Depending on the performance measure required in a particular application of chosen MLI based on the output quality appropriate PWM have to be employed.

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