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Multi Bit Error Tolerant SRAM based TCAM for High Performance Network Operations

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***Abstract*— Ternary Content Addressable Memory (TCAM) be a special kind of memory utilized in high-speed searching applications. Classical TCAMs are implemented in application-specific integrated circuits (ASIC) and SRAM-based TCAMs are implemented in Field Programmable Gate Arrays (FPGA). CAM provides access to the stored data by its content rather than the address. Normally CAM is claimed to be binary CAM that stores 0's and 1's. a complicated version of CAM, referred to as Ternary CAM (TCAM) could be a memory that may also store don't care bit together with 0's and 1's. When FPGA works for high-speed applications, there could also be an opportunity of getting soft errors. The occurrence of such errors affects the functionality of the system. The protection of SRAM-based TCAMs against soft errors is challenging without compromising high search performance. the prevailing technique employs the detection and correction of single-bit upsets, that's single parity is added with each word for fault detection. The proposed technique presents a low-cost error detection and correction of multi-bit upsets (MBU). For the detection of multi-bit errors three parities are used, that's together with the row parity, column parity, and diagonal parity are added. The error-correction process is administrated within the background to take care of a high search performance.**

Keywords*— *Field-programmable gate array (FPGA), soft errors, static random access memory (SRAM)-based ternary content-addressable memory (TCAM).

I. INTRODUCTION

A memory is just type of a personality's brain. It's accustomed store data and instructions. Memory is that the space for storing within the pc, where data is to be processed and directions required for processing are stored. The memory is split into an oversized number of small parts called cells. Each location or cell encompasses a singular address, which varies from zero to memory size minus one. Data access memories are classified into four types. Random Access Memory (RAM), Sequentially Accessible Memory (SAM), Direct Access memory (DAM) and Content Addressable Memory (CAM). RAM is additionally called as read-write memory or the foremost memory. It is a volatile memory because the information loses when the ability is turned off. SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory) are further classifications of RAM. SAM read stored data during a sequence. It is in contrast to random access memory (RAM) where data is accessed in any order. Sequential access devices are usually a sort of magnetic medium or optical storage. The data in DAM is arranged as blocks. These blocks are accessed directly. But the data within these blocks are accessed sequentially. This memory includes magnetic and blind spot drivers and tape memories. CAM is additionally noted as Associative memory. It's of two types Binary CAM and Ternary CAM.

Content-addressable memory (CAM) allows the stored content to be searched in parallel during a very single cycle, achieving a high search performance. A binary CAM stores and searches data in just two states: "0" s and "1" s. A ternary CAM (TCAM) represents data in three different states: "0," "1," and do not care state "x." states. TCAMs are extensively employed in network systems for packet classification and filtering [1], [2]. The figure 1 shows a diagram of a simplified 4 x 5-bit ternary CAM with a NOR-based architecture. The CAM contains the routing table parenthetically how a CAM implements address lookup. The CAM core cells are arranged into four horizontal words and each word are five bits long. Core cells contain both storage and comparison circuitry. The search lines run vertically within the figure and broadcast the search data to the CAM cells. Across the array the match lines run horizontal and indicate whether the search data matches the row's word. A match is indicated by an activated match line and a non-match is indicated by a deactivated match line called a mismatch within the CAM literature. The match lines are inputs to an encoder that generates the address such as the match location.

Modern static random-access memory (SRAM)-based field programmable gate array (FPGA) technology offers the flexibleness and reconfigurability with high performance required in software defined networking (SDN) and OpenFlow network accelerators for big data [2]. Owing to the disturbances from high-energy neutron particles, circuits on SRAM-based FPGAs are susceptible to single-event upsets (SEUs) [3]. The on-chip embedded memory has been known as the most at risk of SEUs in advanced process technologies due to their small size and highly compact memory cells [4], [5]. An SEU in embedded memory generates a transient error until the corrupted data is overwritten [5].

Single event upsets may find in either single-bit upsets (SBUs) or multiple-bit upsets (MBUs). A low-cost solution for implementing efficient binary CAMs on FPGAs is offered by Cuckoo hashing [6]. In most of the SRAM-based FPGA solutions the TCAM function is defined by the content of the configured embedded memories [i.e., block RAM (BRAM), distributed RAM (distRAM)] [7], and a transient error may cause a false match/mismatch and returns an incorrect match address. Accordingly, within the case of a soft error, the affected word of SRAM should be overwritten to retrieve the correct matching information during lookups. However, the

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protection of SRAM-based TCAM solutions is a challenging one, without compromising the critical path delay and maintaining high search performance.

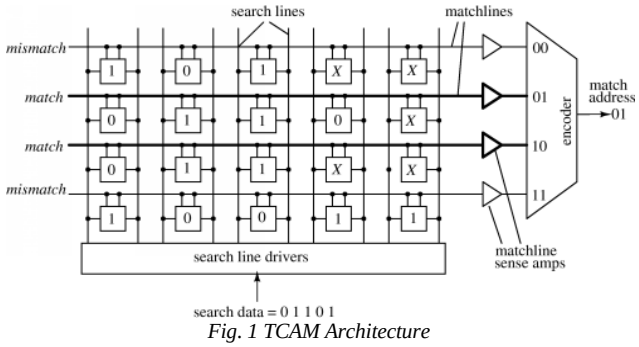

Fig. 1 TCAM Architecture

This brief presents a low-cost, low-response time and easy for integration technique for the protection of SRAM-enabled TCAMs without compromising the search performance. The proposed technique presents a low-cost error detection and correction of multi bit upsets (MBU). For the detection of multi bit errors three parities are used, that is along with the row parity, column parity and diagonal parity are added. The error-correction process is carried out in the background to maintain a high search performance. In the existing system it presents a low-cost, low-response time and easy for integration technique for the protection of SRAM-enabled TCAMs without compromising the search performance. The error detection is carried out in a simple way using single-bit parity checking at a minimal delay and logic overhead. The error-correction technique exploits the redundant binary-encoded TCAM table maintained in SRAM-based TCAM solutions for update purposes to correct soft errors. It maintains a high search performance while the error-correction mechanism is carried out in the background, allowing search operations to be performed simultaneously.

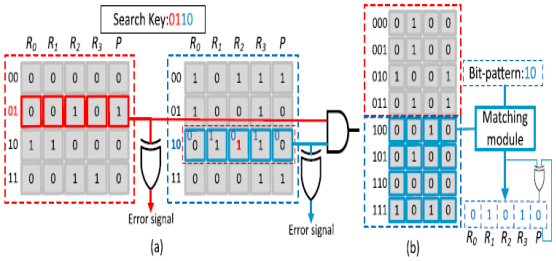

Fig. 2 Simplified example for existing ER-TCAM (a) Error detection (b) Error correction

The basic idea of the ER-TCAM technique is illustrated in this figure 2. The two SRAMs, implements the TCAM table partitions and shows an 8 × 4 size SRAM storing binary-encoded contents of the TCAM table, providing redundancy of the matching information in SRAMs realizing TCAM. To detect an SBU in SRAMs, the ER-TCAM adds a parity bit for each SRAM word as shown in figure 2 (a). Error detection is performed on the words of SRAMs accessed during lookups. Once an error is detected in a word, the ER-TCAM uses the redundant information stored in the binary-coded TCAM table for correction. For example, when a search key (0110) is applied to SRAMs shown in figure (a), accesses the second (00101) and third words (01110) of the first and second SRAMs, respectively. The calculated parity for the match bits of the second SRAM word (01110) does not match the parity stored, indicating the occurrence of an SBU in SRAM as shown in figure 2 (a). The ER-TCAM accesses the words of SRAM storing the binary-encoded contents of the related TCAM partition one by one. The SRAM words read are matched with the corresponding bit pattern (10) to compute match bits and associated parity (01010) collectively called error-correction vector (ECV). The computed ECV is further written over the corrupted SRAM word.

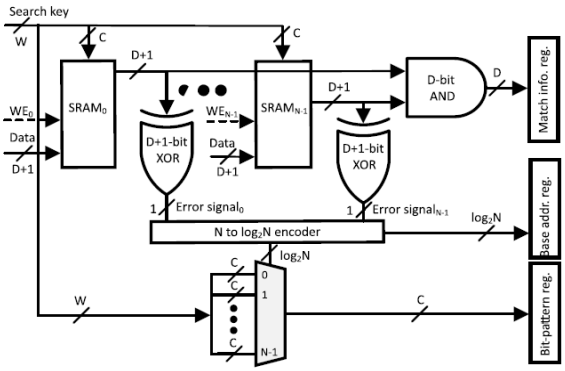

Fig. 3 Existing ER-TCAM architecture for error detection

The figure 3 shows ER-TCAM error-detection architecture. When an input search key is applied for lookup, the bits of the SRAM words read are EX-ORed to get an error signal. In the TCAM design the error signals from the N SRAMs are encoded to get a log2N-bit error code. This code uniquely identifies respective corrupted SRAM. The error code and related search-key bit patterns are forwarded to the error-correction module. The figure 4 shows the ER-TCAM architecture for error correction which mainly comprises an SRAM storing binary-encoded contents of the TCAM table, an ECV computation unit, an address generation unit (AGU), and a read/write controller. The SRAM address is executed such that log2N-bits of the SRAM ID constitute its most significant bits and points to the start of the corresponding sub-block in SRAM, and the lower log2D bits from the counter select SRAM words in the sub-block. In this way, the AGU accesses all the binary encoded words of the corresponding partition of the TCAM table.

The TCAM words read are matched with the C-bit pattern to get a match bit each cycle, thus requiring D clock cycles to compute the match bits and associated parity bit, composing the ECV. The read/write controller generates write enable high signal for the corresponding SRAM to write the computed ECV over the corrupted SRAM word. During the error-correction process, the ER-TCAM allows search operations as SRAMs realizing the TCAM function are available for lookup operations. The ER-TCAM configures these SRAMs as simple dual-port RAM that performs the read and write in parallel at the same clock cycle. Once the ECV is computed, it is written using the write port of SRAM, thus, the error correction process completely overlaps the search operations in the ER-TCAM. Although a soft error can occur in the SRAM storing binary-encoded TCAM table; however, its error occurrence probability compared with that of SRAMs realizing ternary content addressable memory is very low, owing to its relatively small size.

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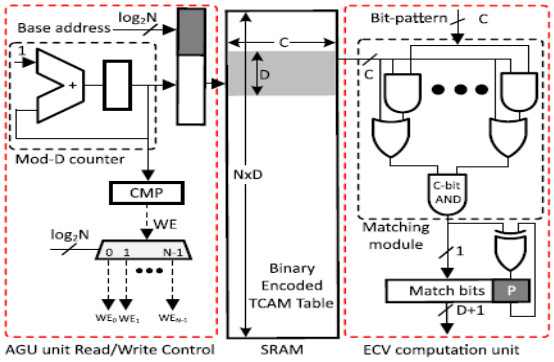

Fig. 4 Existing ER-TCAM error-correction module

II. TERNARY CONTENT ADDRESSABLE MEMORY

Ternary content addressable memories (TCAMs) are widely employed in network devices to implement packet classification. they're used, as an example, for packet forwarding, for security, and to implement software-defined networks (SDNs). An issue when using memories is that they can be tormented by soft errors that corrupt the stored bits. The memories are protected with a parity check to detect errors or with a blunder correction code to correct them, but this needs additional memory bits per word. During this brief, the protection of the memories to emulate TCAMs is taken into account. This scheme is to produce protection against soft errors and therefore the error correction technique which supplies low reaction time, low cost, high search performance for ensuring faultless SRAM –Based TCAM Design.

A. SRAM based TCAM on FPGAs

On chip SRAM memories in modern FPGAs are used for implementing TCAM solutions. as an example, a 1 × 1 TCAM are often implemented employing a 2 × 1 RAM specified the match knowledge is represented by storing a "1" at RAM[0] for the presence of a "0" TCAM state, a price of "1" by storing a "1" at SRAM[1], and "x" state by storing a "1" at both the SRAM[0] and SRAM[1] locations. A C-bit TCAM pattern are often implemented employing a 1-bit SRAM of 2C positions. The words of the SRAM stores match or mismatch information for each word of the TCAM table against all the possible C-bit patterns that is the address of an SRAM represents the C-bit TCAM pattern, during this way, a C-bit wide TCAM table of B words can be implemented employing a B bits wide SRAM of 2C positions. Researchers divide the wide TCAM bit patterns into smaller chunks as they're doing not scale well in terms of required memory in SRAM-based TCAMs. There are different solutions for implementing TCAM on FPGAs [7].

B. Error Detection and Correction in TCAM

Soft errors are a significant concern for contemporary electronic circuits and, in particular, for memories. A soft error can change the contents of the bits stored during a memory and cause a system failure. The soft error rate in terrestrial applications is low. as an example, it was estimated that the bit error rate was on the order of 10−9 errors per year for a 65-nm static random-access memory (SRAM) memory. However, even such an occasional error rate is a big concern for critical applications like communication networks on which the network elements like routers must provide a high level of reliability and availability. Therefore, soft errors are a crucial issue when designing routers or other network elements, and makers take them under consideration and incorporate error mitigation techniques. For instance, error detection and correction codes are commonly wanted to protect memories.

III. PROPOSED ERROR TOLERANT TCAM

Ternary Content Addressable Memory (TCAM) is a special type of memory used in high-speed searching applications. Classical TCAMs are implemented in application-specific integrated circuits (ASIC) and SRAM-based TCAMs are implemented in Field Programmable Gate Arrays (FPGA). CAM provides access to the stored data by its content instead of the address. Normally CAM is said to be binary CAM that stores 0's and 1's. An advanced version of CAM, known as Ternary CAM (TCAM) is a memory that can also store don't care bit along with 0's and 1's. When FPGA works for high-speed applications, there may be a chance of getting soft errors. The occurrence of such errors affects the functionality of the system. The protection of SRAM-based TCAMs against soft errors is challenging without compromising high search performance.

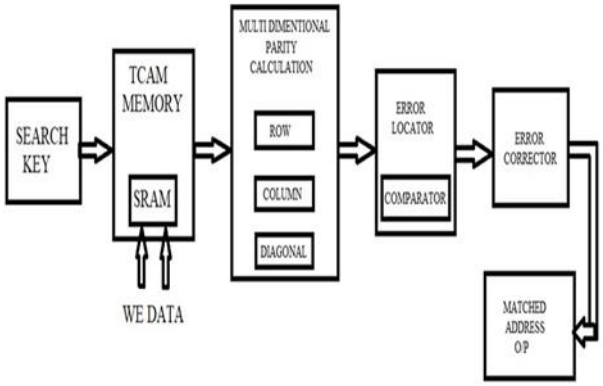

Fig.5 Block diagram of proposed error tolerant TCAM

The existing technique employs the detection and correction of single-bit upsets. The proposed technique presents a low-cost error detection and correction of multi-bit upsets (MBU). For the detection of multi-bit errors, three parities are used, that is along with the row parity, column parity, and diagonal parity are added. The error-correction process is carried out in the background to maintain a high search performance. Figure 5 represents the block diagram of the proposed system. When a search key is applied to the memory unit for the search operation, it searches the corresponding words in the SRAM. After that, the corresponding parities are calculated. If any mismatch occurs the error is detected. After the error detection, the words are sent to an error correction section. Then it is corrected and overwritten in the memory.

IV. MULTIBIT UPSETS PROTECTION

For error detection in each memory entry (i.e., word) employed parity bits are computed during each memory

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access in memory arrays of typical microprocessors like cache units. Hence, from the performance perspective, there is a slip-up detection coding for each memory entry. Otherwise, during each operation, all other entries that are involved within the computation of the corresponding common parity bit(s) must be accessed also. Although the errors in FPGAs are detected during the periodic scrubbing. Here the entire contents of a configuration frame can be accessed by the error checking unit. In the proposed error detection technique, different parities are calculated. With the help of these generated parity errors are detected. an error is detected if there's any mismatch between generated and calculated parity. After the error detection, words are sent to the error correction section. The corrected words are overwritten into the memory.

V. RESULTS AND DISCUSSION

A. Simulated result of existing TCAM

An error resilient TCAM is designed for single bit error detection and correction. Initially the error detection module is developed. After detecting the error, the error correction module works. During the error-correction process, the ER-TCAM allows search operations as SRAMs realizing the TCAM function are available for lookup operations. Once the ECV is computed, it is written using the write port of SRAM, thus, the error correction process completely overlaps the search operations in the ER-TCAM. In this existing technique it allows only single bit error detection and correction. That is this technique does not work if more than one error occurs.

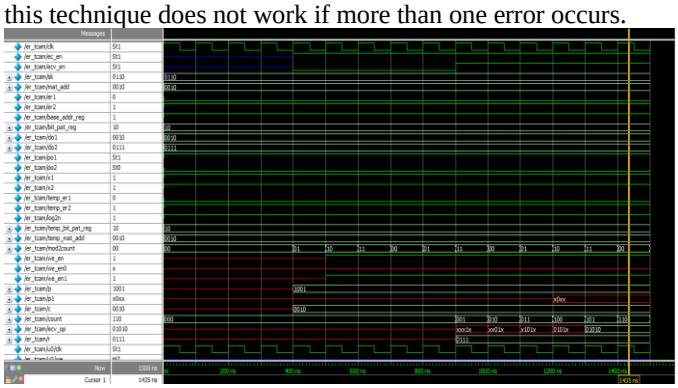

Fig.8 Simulated result of existing TCAM

B. Simulated result of proposed ER-TCAM

A multi-bit error resilient TCAM is designed for multi-bit error detection and correction. Initially, the error detection module is developed. Here it makes use of three types of parity calculation that is row parity, column parity, and diagonal parity are calculated. After detecting the error, the error correction module works. The error-correction process makes use of the error locator and gate operations. This proposed technique allows multi-bit error detection and correction.

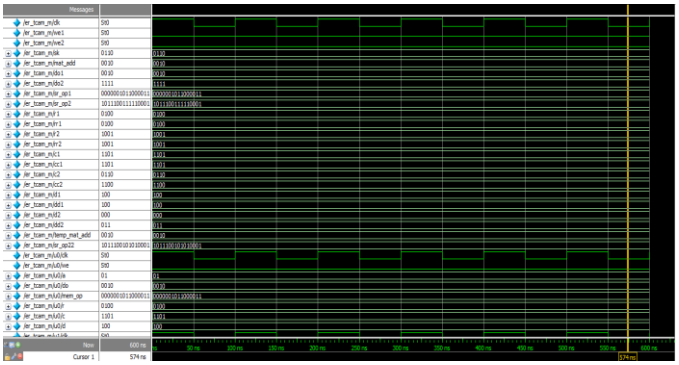

Fig.9 Simulated result of proposed ER-TCAM

VI. CONCLUSION

An error detection and correction technique for SRAM-based TCAMs makes the most of the redundant original TCAM content maintained on-chip for update purposes. The existing method uses single-bit parity to detect faults at a minimal cost of logic and critical path delay. The error resiliency technique, called ER-TCAM, employs the binary-encoded TCAM table in SRAM-based TCAMs to correct errors. SRAMs implementing the TCAM function are available for search operations during the error-correction process carried out in the background, thus, the error-correction technique does not affect the data path processing. Multibit error detection and correction of SRAM based TCAM was done in this proposed technique. For that purpose, it makes use of three parities. The error-correction process is carried out in the background to maintain a high search performance.

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