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# MTCMOS Based 14T SRAM Cell Optimized for High Performance Applications

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***Abstract*- Static Random Access Memories (SRAM) are designed to provide high speed access and low power consumption to the memory system. Due to aggressive scaling of devices, low power design is extremely important to meet the required constraints. MTCMOS is a technique to achieve low power consumption by employing sleep transistors to reduce the energy requirement of the cell during idle state. The conventional 12T MTCMOS based SRAM cell employs NMOS access transistors. However, this results in a delay and higher power consumption. Hence, a novel MTCMOS based 14T SRAM cell is designed to offer low power consumption with least delay. In the proposed structure, a voltage mode method and TGs are used to reduce the power dissipation. The simulations have been carried out at 45nm CMOS technology, power supply of 1v and a temperature of 25℃ is taken as a reference. Results show that the power, delay, Power delay product (PDP) and Static Noise Margin (SNM) of the proposed design are improved. Tanner EDA 14.11 is used for the analysis of the circuit and Bsim4v450 model library is used as a tool for simulation.**

***Keywords- MTCMOS, Dynamic Power, Swing Voltage, Transmission Gates.***

## I. INTRODUCTION

With the latest advancement in VLSI design methodology; there has been an immense scope of aggressive scaling of the designs. For, high speed memory systems, SRAM plays a vital role because of its low power consumption and very high operating speeds. Dynamic power dissipation and delay are the most crucial parameters while designing the cell (P. Upadhyay, 2015).

Certain power saving techniques had been investigated, among them is reducing the supply voltage. However, it does not prove to be good enough, since it causes the degradation in the circuit performance (Prashant Upadhyay R. K., 2013). The fact is that lowering the supply voltage, reduces the threshold voltage which ultimately increases the leakage current. Although there are other techniques to reduce the power consumption which includes Multiple Threshold CMOS, Sleep transistors, Voltage Mode method and implementation with new device structures (al F. H., 2000) (al R. W., 2003) (al M. S., 2007).

In Voltage Mode method, two voltage sources are used on either bit lines to compensate the voltage swing of the cell, hence dynamic power consumption reduces.

The given relation explains the above dependencies.

$$P_{dynamic} = \propto . C . V_{DD} . V_{swing} . f$$

Where, $\alpha$ is activity factor, $C$ is load capacitance, $V_{DD}$ is supply voltage, $V_{swing}$ is voltage swing and $f$ is frequency of operation.

MTCMOS technique uses multiple threshold transistors having low and high threshold voltages to reduce the power consumption of the cell (Suman Nehra, 2013).

The paper proposes a newly designed 14T SRAM cell which possesses Transmission Gates as the pass transistors. Two voltage sources are used to reduce the voltage swing hence making it less power hungry even at high frequencies. Moreover, Sleep Transistors are also employed to save the energy consumed during standby mode. TGs in the circuit provide charge recycling to reduce leakage power. Later, high performance parameters are calculated for proposed design and compared with the existing 12T SRAM cell.

The paper is organized as follows; section II explains the existing SRAM cells and their design development, section III describes the circuit diagram and the working principle of the proposed cell, section IV discusses the result and analysis part of the cell and its comparison with earlier cell design and finally section V concludes the paper.

## II. LITERATURE SURVEY

The schematic of conventional 6T SRAM cell employs pairs of cross coupled inverters. The pass transistors are activated by asserting the word line high while performing reading and writing operation in the cell (Prashant Upadhyay R. K., 2014). However, a cell is unstable during read and write operation which reduces the noise immunity of cell. Moreover, the dynamic power dissipation is not acceptable when used for high frequency applications (Kim TH, 2008). The 7T SRAM cell uses two virtual ground rails and a separate read bit lines for read operation, hence able to exhibit very good read Static Noise Margin (Azam T, 2010). The stability issue in 7T cell are minimized in 8T which uses separate read/write bit lines and write signal lines for their operations which improve the stability of the cell. However, bit line leakage is higher during read operation which causes severe voltage drop at the read bit line leading to large power dissipation (Chen G, 2010). The large bit line leakage is overcome in 9T cell design. Due to bit line leakage, bit line drops to a lower level. This limits it to the low density application. An additional NMOS is introduced in the design to decrease the bit line leakage by stack effect. Reduction in leakage makes this cell suitable for high density applications (Liu Z, 2008). A 10T SRAM cell incorporates an enabled

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Word line along with ground which is forced to 0 .Both the outputs can be decoupled during read access from the bit line. Thus, read stability is improved (Lo CH, 2011). As an enhancement, 11T possess a node where high logic value have to be written is disconnected from the ground therefore, results in faster write operation. The operation speed is also improved as the transistors are arranged in such a way to provide low effective resistance path (Singh AK, 2009). A 12T MTCMOS based SRAM cell improves certain parameters simultaneously like dynamic and static power dissipation by using high threshold sleep transistors, leakage current and stability (P. Upadhyay, 2015). The schematic diagram of 12T SRAM is given below in Figure 1:

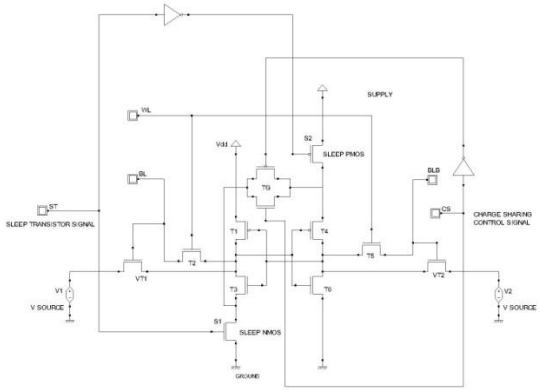


Figure 1 Base 12T SRAM Cell

For dynamic power reduction, voltage sources are used to reduce the voltage swing during switching activity. The high threshold sleep transistors are employed to lower the power consumption of the circuit while transmission gate provides the charge sharing to reduce the static power dissipation caused due to transition of the cell from sleep mode to active mode and vice versa. The charge sharing process can be enhanced by increasing the size of the transmission gate, though it has certain limitations because increasing the size beyond limit will reduce the energy saving ratio of the circuit (P. Upadhyay, 2015).

A voltage mode method limits the dynamic power consumption and makes it almost constant even at high frequencies. Since, they provide better switching capability; hence stability of the cell is also improved (Prashant Upadhyay R. K., 2013). The more number of transistors in the cell increases the layout area but this parameter can easily be overridden by less power consumption and improved stability.

## III. PROPOSED 14T SRAM CELL

A 12T SRAM design needs further optimization. So, a 14T SRAM cell is designed to improve the write delay and power consumption of the cell. Now, the circuit possess the transmission gates in place of NMOS pass transistors to optimize the high performance parameters of the cell. Figure 2 shows the schematic diagram of newly proposed cell.

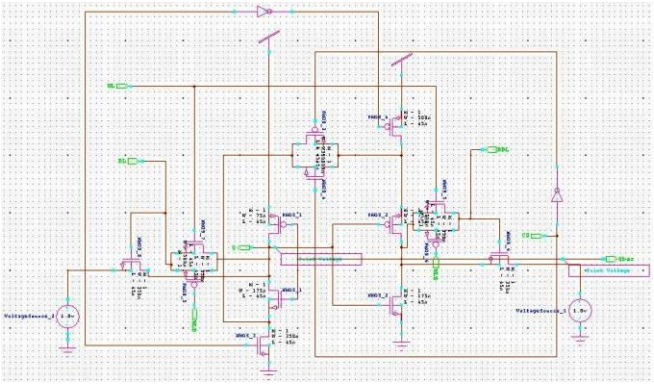

Figure 2 Schematic of 14T Proposed SRAM cell

Transmission gate is an analog switch which can pass the signal in either direction having wide range of voltage potential (Joshika Sharma, 2015). It removes the problem of not able to pass strong 0 and 1 by PMOS and NMOS respectively. Transmission gates solve this problem as both PMOS and NMOS conducts simultaneously. The parasitic resistance and capacitance of the circuit is often reduced by employing transmission gates. As above inability can reduce noise margin and increase static power dissipation of the circuit (P.Upadhyay, 2014).

### *A. Operation of Sleep Transistors*

As the sleep transistor signal (ST) is low, it turns on both the transistors. Hence, it connects the virtual ground to the actual ground. Similarly, the virtual supply is connected to actual supply via sleep transistor signal. During active period, both the transistors work in the linear region and the voltages at the nodes of both transistors are at 0 and $V_{DD}$ respectively. While writing 1 into the cell, and active to sleep transition (P.Upadhyay, 2014), the sleep transistors will be turned off and due to high threshold, they allow very low sub threshold leakage currents. Hence, power dissipation will be reduced. Both the virtual nodes are in floating mode during the transition. But, due to leakage current flowing through off transistor, the nodes are charged to weak $V_{DD}$ and discharged to weak ground. Similarly, charging and discharging of nodes occur while writing 0 . This charging and discharging phenomena leads to static power dissipation which is reduced by Transmission gate that employs charge recycling technique.

### *B. Swing Voltage*

While the transistor switches from high to low and vice versa at bit lines, there is a need of swing voltage. It is a major factor in dynamic power dissipation. This should be reduced to ensure low power dissipation. In our design, we use two voltage sources on bit and bit bar lines to reduce dynamic power dissipation even at higher frequencies. Better switching capability of the proposed SRAM cell will also enhances its stability.

While writing‘0’, BL (Bit Line) is low and BBL (Bit Bar Line) is high. Hence, NMOS VT1 will be off and NMOS VT2 on to decrease the voltage swing of the BBL output. Similarly, for writing‘1’, BL is high and BBL is low. Hence,

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VT1 will be on and VT2 will be off which decreases the swing voltage of the output of bit lines.

The increased area of the cell can easily be overridden by the improved power consumption, delay and stability of the proposed SRAM cell.

### C. *Charge Recycling Technique*

As the circuit switches between active and sleep mode, there occurs a static power dissipation which is not recommended for high speed applications. To reduce this power dissipation, a charge recycling technique is used which is employed by TG connected in a circuit. The TG connects the virtual ground and virtual supply nodes in the circuit. Charge recycling TG is activated just before turning on the sleep transistors (transition from sleep to active mode) and just after turning off the sleep transistors (transition from active to sleep mode) to share the charge between virtual ground and virtual supply nodes and maintain the common voltage i.e., $\propto . \boldsymbol{V_{DD}} (\propto < 1)$ , hence, mode transition energy is reduced (P.Upadhyay, 2014) (Agarwal N, 2014).

## IV. RESULTS AND DISCUSSIONS

This section shows the results including dynamic power dissipation, delay for write 0 and 1, Power Delay Product for write 0 and 1 and finally Static Noise Margin of the proposed SRAM cell and the results are compared with the base designs. Schematic and simulation have been done in 45nm CMOS technology by Tanner EDA 14.11 using Bsim4v450 model library. The various parameters used for simulation are listed in the Table 1. The transient response of proposed 14T SRAM cell is given in Figure 3.

Table 1 Parameters Used for Simulation

| | | |
|---|---|---|
| Supply Voltage | | 1.0 V |
| Transistor Width | PMOS (Pull Up) | 75 nm |
| | Access Transistors | 115 nm |
| | NMOS (Pull Down) | 175 nm |
| | NMOS (Voltage Mode) | 350 nm |
| | Sleep NMOS | 350 nm |
| | Sleep PMOS | 500 nm |
| | TG NMOS | 350 nm |
| | TG PMOS | 500 nm |
| Transistor Length | All transistors | 45 nm |
| Temperature | | 25°C |

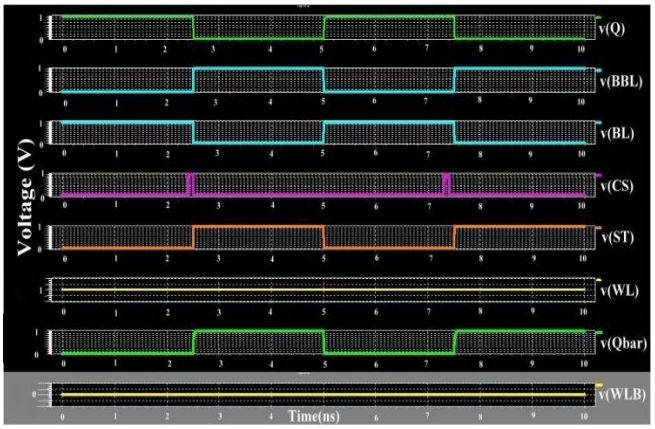


Figure 3 Transient Response of 14T SRAM Cell

### A. *Total Power Dissipation*

We have calculated the average power dissipation during write operation of the proposed SRAM cell and compared it with the base design. The comparison is shown in Table 2. The power consumption of the proposed cell shows an improvement of 52.25%.

Table 2 Power Dissipation of the designs

| Design | Power Consumed (uW) |
|---|---|
| 12T Base | 3.4427 |
| 14T Proposed | 1.6438 |

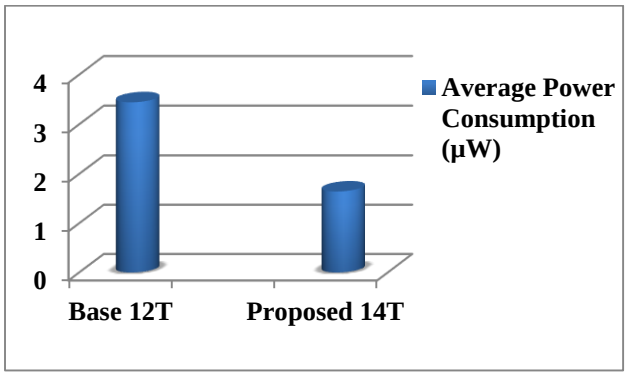


Figure 4 Comparison of Power Consumption

### B. *Access Times*

The access time of SRAM cell for write operation is the time required to complete one cycle of write operation (P. Upadhyay, 2015). The delay in the cell depends on the charging and discharging of load capacitance. The speed of proposed SRAM cell is found to be improved than its base design. The Table 3 shows the comparison of access times for write 0 and write 1 operation. The analysis confirms that delay for write 0 and write 1 is reduced by 74.68% and 69.28% respectively.

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Table 3 Comparison of Access Time

| Design | Write 0 (ps) | Write 1 (ps) |
|---|---|---|
| 12T Base | 12.597 | 3.7113 |
| 14T Proposed | 3.1896 | 1.1399 |

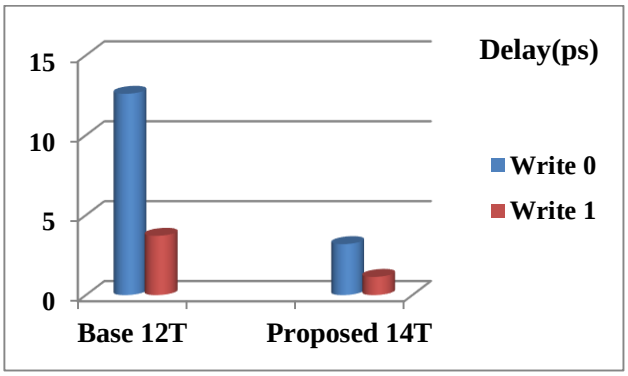


Figure 5 Comparison of Write Delay

### C. *Power Delay Product*

Power Delay Product is defined as the product of total power dissipation and the access time of the SRAM cell. Since, there exists a trade off between delay and power consumption, hence power delay product signifies the performance of the SRAM cell (P. Upadhyay, 2015). The comparison is shown in Table 4. In case of PDP, the improvement of 87.9% and 85.33% is observed during write 0 and write 1 operation.

Table 4 Comparison of PDP

| **Design** | **PDP 0 (aWs)** | **PDP 1 (aWs)** |
|---|---|---|
| **12T Base** | 43.366 | 12.777 |
| **14T Proposed** | 5.2431 | 1.8737 |

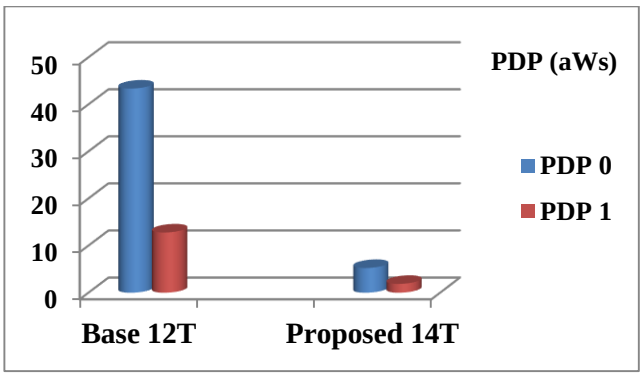


Figure 6 Comparison of PDP for Write Operation

### D. *Static Noise Margin*

Static Noise Margin defines the stability of the SRAM cell. Higher value of Noise Margin ensures the better noise immunity of SRAM cell. It is the minimum DC noise voltage, below which the states of cell will flip making it unstable. It is calculated by plotting the VTC curve of two inverters and fitting a square of maximum length. The length of square gives the value of SNM of the cell. Table 5 gives the comparison of SNM for both the designs of read, write and hold operations. The SNM for write operation improves by 27.5%, while hold operation offers no change. However, read SNM is reduced by 20%. Hence, cell possesses better stability during write operation.

Table 5 Comparison of SNM for both designs

| Design | SNM (mV) | | |
|---|---|---|---|
| | Write | Hold | Read |
| 12T Base | 400 | 300 | 100 |
| 14T Proposed | 510 | 300 | 80 |

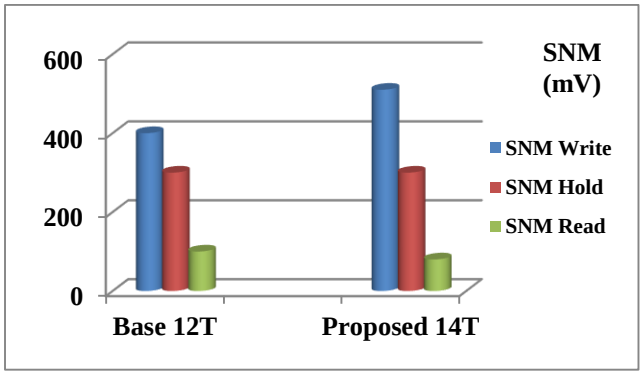


Figure 7 Comparison of SNM for both designs

## V. CONCLUSION

As the technology is enhancing and demand of high speed applications is increasing as a result the frequency of operation also have to be increased. Due to this, the dynamic power dissipation is becoming a critical issue in modern VLSI design. The novel MTCMOS design proposed dissipates less power even at high frequencies. It also offers the least delay with better stability as compared to other SRAM cells. The Transmission Gate used in the design reduces the static power consumption and leakage current. Simulation results shows that proposed design is far more superior to pre existing cell designs. The advantage of the design that we have not increased the number of transistors in the cell, hence the area remains intact but performance is improved considerably. The proposed 14T SRAM cell meets the current demand of high speed applications and low power design which can be used in various low power and high speed compact devices.

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