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Modified Seven-Level Cascaded H-Bridge Multilevel Inverter

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***Abstract*—— The multilevel inverter utilization has been increased since the last decade. These new types of inverters are suitable in various high voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. This paper presents a modified seven level cascaded H-bridge multilevel inverter, using multicarrier pulse width modulation technique.**

***Keywords*—Cascaded H-bridge multilevel inverter (CHB), multicarrier pulse-width modulation, total harmonic distortion (THD).**

I. INTRODUCTION

Demand for high-voltage, high power converters capable of producing high-quality waveforms while utilizing low voltage devices and reduced switching frequencies has led to the multilevel inverter development with regard to semiconductor power switch voltage limits. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

The most attractive features of multilevel inverters are as follows: -

1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4) They can operate with a lower switching frequency.

The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives, power conditioning devices, also conventional or renewable energy generation and distribution. The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitor multilevel inverter. Among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity, a feature that enables the inverter to continue operating at lower power levels after cell failure.

Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high-voltage applications. The cascaded multilevel inverter typically comprises several identical single-phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge, which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are varied to produce more output levels.

II. CONVENTIONAL CASCADED SEVEN LEVEL MULTILEVEL INVERTER

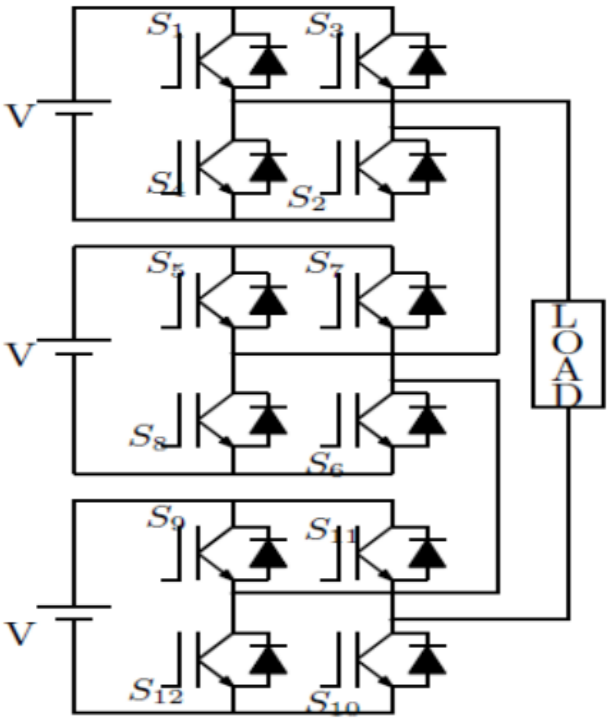

Fig 1. Conventional seven level multilevel inverter

Cascaded multilevel inverter is a series connection of single-phase inverters with separate dc sources. The seven-level multilevel inverter is obtained by cascading three full bridge inverter circuits. The three full bridge inverters are connected in series and a single-phase output is taken. Each full bridge is fed from separate DC source. The number of output levels m in each phase is related to number of full bridge inverter units n by, m/2n+1. Here number of levels is seven, hence number of inverter circuits connected in series is three. The

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single phase seven-level topology of cascaded H bridge multilevel inverter is shown in Fig. 1. Each H-bridge is fed with the same value of DC voltage hence it can be called as symmetrical cascaded multilevel inverter. Each full bridge inverter can generate three different voltage outputs: +Vdc, 0, and -Vdc. The output voltage is synthesized by sum of three inverter outputs are at three angles. These three angles are used for giving pulses to twelve switches.

TABLE I : SWITCHING STATES FOR A SEVEN LEVEL INVERTER

V_0	+V	+2V	+3V	0	-V	-2V	-3V
S_1	1	1	1	0	0	0	0
S_2	1	1	1	1	0	0	0
S_3	0	0	0	0	1	1	1
S_4	0	0	0	1	1	1	1
S_5	0	1	1	0	0	0	0
S_6	1	1	1	1	1	0	0
S_7	0	0	0	0	0	1	1
S_8	1	0	0	1	1	1	1
S_9	0	0	1	0	0	0	0
S_{10}	1	1	1	1	1	1	0
S_{11}	0	0	0	0	0	0	1
S_{12}	1	1	0	1	1	0	1

III. MODIFIED SEVEN LEVEL MULTILEVEL INVERTER

A modified seven level multilevel inverter was developed with reduced switches that can produce seven levels of DC voltage of 3Vs, 2Vs, Vs, 0, -Vs, -2Vs and 3Vs. This topology requires five fully controlled unidirectional-blocking-bidirectional conducting switches, two bidirectional-blocking-bidirectional-conducting switches and three DC sources for attaining a seven-level inverter. Conventional cascaded seven level inverter requires twelve switches and twelve gate drivers for attainment of distinct voltage levels. The developed reduced switch seven level inverter has a reduced device count of nine switches and seven gate drivers for generation of output voltage levels giving a 25 % reduction in the number of main power switches. The circuit diagram of new reduced switch seven level multilevel inverter compared to conventional seven level MLI is shown in Figure 2.

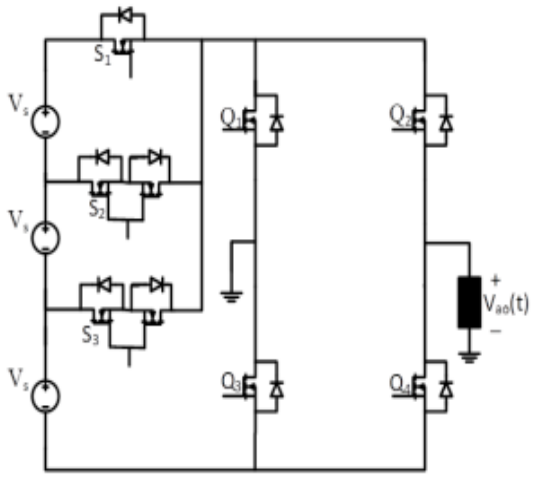

Fig 2.Modified seven level multilevel inverter

The switching pattern for reduced switch MLI (7-Level) is tabulated in Table 2. The logical equations governing the control circuit of the reduced switch seven level inverter are given below.

$$Q_1 = Q_4 = (P_1(C_1 + P_2)) + (\overline{P_1}\overline{(C_1 + (\overline{P_2}))})$$

$$Q_2 = Q_3 = \overline{(P_1(C_1 + P_2)) + (\overline{P_1}(C_1 + (\overline{P_2}))}$$

$$S_1 = C_3$$

$$S_2 = (\overline{C_2}\overline{(C_3)})$$

$$S_3 = C_1C_2$$

The control circuit of seven level inverter is shown in Figure 3. C1 and C2 and C3 represents the control pulses generated by comparing sine wave of amplitude 3 V and frequency 50 Hz with three triangular carriers (level shifted) of amplitude 1 V and frequency 1kHz. P1 is a square pulse having duty cycle of 0.5 and frequency 50 Hz. P2 is the delayed pulse of P1 shifted by 0.001 s from the origin.

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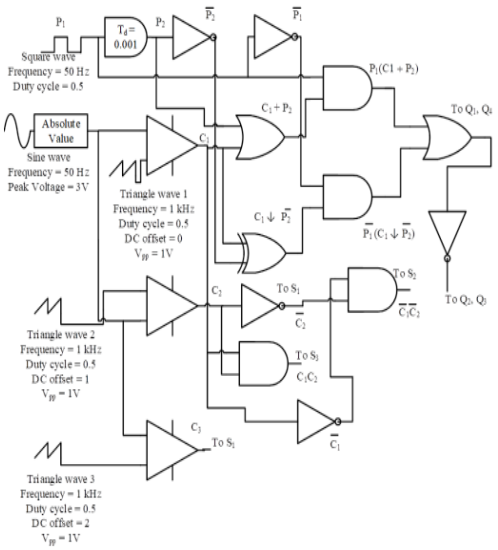

Fig 3. Control circuit for seven level inverter

TABLE 2 SWITCHING STATES FOR INVERTER

Modes	Switching pattern for inverter							
	V_o	Q_1	Q_2	Q_3	Q_4	S_1	S_2	S_3
Mode-1	$3V_s$	1	0	0	1	1	0	0
Mode-2	$2V_s$	1	0	0	1	0	1	0
Mode-3	V_s	1	0	0	1	0	0	1
Mode-4	0	0	0	1	1	0	0	0
Mode-5	$-V_s$	0	1	1	0	0	0	1
Mode-6	$-2V_s$	0	1	1	0	0	1	0
Mode-7	$-3V_s$	0	1	1	0	1	0	0

IV. SIMULATION RESULTS

Simulation results of reduced switch seven level inverter have been obtained using PSIM Professional Version 9.0.3.400.

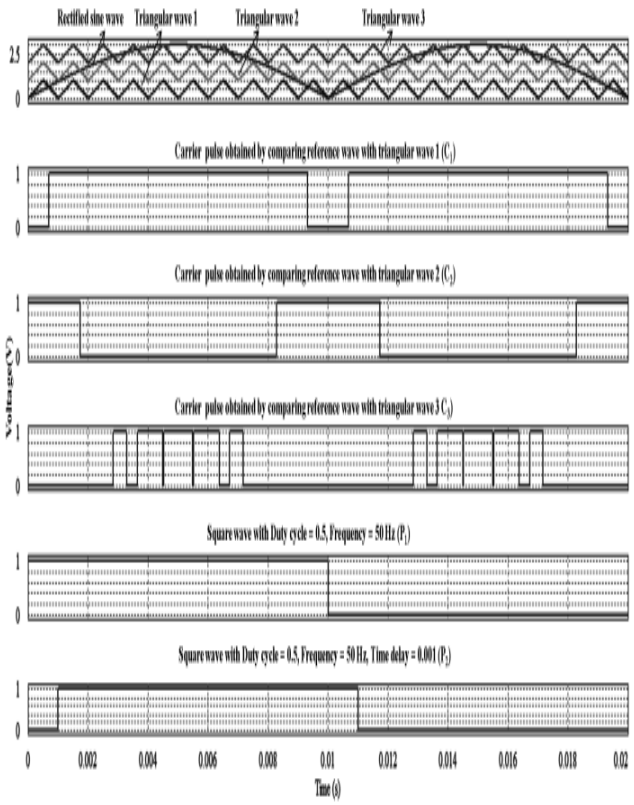

Fig 4. Generation of carrier signals

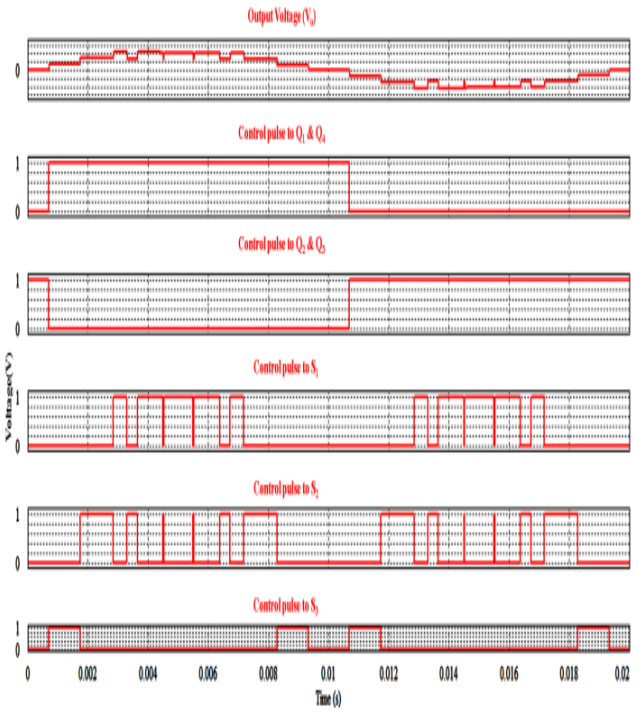

Fig 5. Generation of control signals

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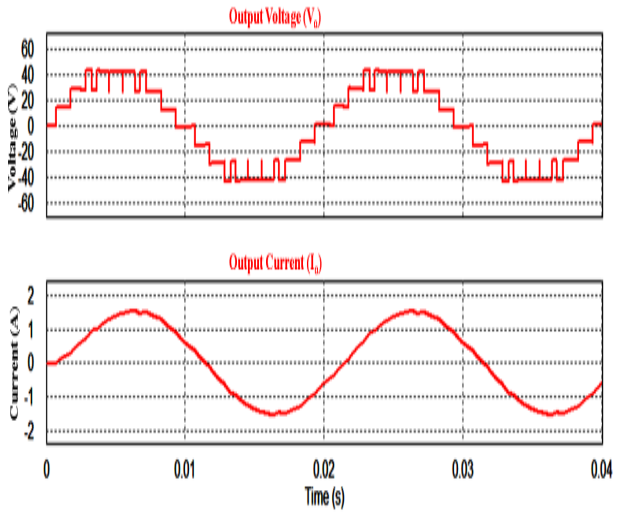

Fig 6. Output voltage and current

V CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. This paper presents a new seven-level Cascaded H-bridge multilevel inverter with reduced number of switches. The simulation was made using PSIM Professional Version 9.0.3.400. The simulation results shows that the developed seven-level Cascaded H-bridge Multilevel inverter has many merits such as reduce number of switches, lower EMI and less harmonic distortion. The reduced switch multilevel topology can be extended to three phase circuits. It is also more suitable for the purpose of integrating PV arrays and grid system.

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