MODIFIED 16-BIT LOW POWER AREA EFFICIENT CARRY SELECT ADDER

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Abstract—Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. By gate level modification of CSLA architecture we can reduce area and power. Based on this modification 16-b square-root CSLA (SQRT CSLA) architecture have been developed. The proposed design has reduced area and power as compared with the regular SQRT CSLA. This work evaluates the performance of the proposed designs in terms of area, power and through Xilinx ISE 13.2 (VHDL). And in here modification in XOR gate can further reduce the power and area of both regular and modified carry select adder. Microwind is used to calculate power of xor gate.

Keywords: Low Power, SQRT CSLA, Area Efficient, BEC.

I. INTRODUCTION

Design of area and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1 bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 1 and Table I respectively.

II. LITERATURE REVIEW

Existing system consist of high power & high area. Thus the proposed system reduces the area and power. But existing system consist of high speed than proposed system. Modification done in xor gate can reduce the area and also power.

III. EXISTING SYSTEM

The carry-select adder generally consists of two ripple Carry Adders (RCA) and a Multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two RCA). In order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one.

IV. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1 bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 1 and Table I respectively.

Fig. 1. 4-b BEC.[1]
Table 1. FUNCTION TABLE OF THE 4-b BEC[1]

<table>
<thead>
<tr>
<th>B[3:0]</th>
<th>X[3:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0001</td>
</tr>
<tr>
<td>0001</td>
<td>0110</td>
</tr>
<tr>
<td>0010</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td></td>
</tr>
<tr>
<td>0101</td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td>1111</td>
</tr>
<tr>
<td>0111</td>
<td>0000</td>
</tr>
</tbody>
</table>

\[
\begin{align*}
X_0 & = \sim B_0 \\
X_1 & = B_0 \sim B_1 \\
X_2 & = B_2 \sim (B_0 \& B_1) \\
X_3 & = B_3 \sim (B_0 \& B_1 \& B_2).
\end{align*}
\]

V. AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 4, in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows. 1) The group2 [see Fig. 4(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table 1, the arrival time of selection input \(C_1[\text{time}]=7\) of 6:3 mux is earlier than \(S_3[\text{time}]=8\) and later than \(S_2[\text{time}]=6\). Thus, \(\text{sum}_3[\text{time}]=11\) is summation of \(s_3\) and \(\text{mux}[\text{time}]=3\) and \(\text{sum}_2[\text{time}]=10\) is summation of \(c_1\) and \(\text{mux}\).

Fig. 2 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input \((B_3, B_2, B_1, \text{ and } B_0)\) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BECIs listed as (note the functional symbols \(\sim \text{NOT}, \& \text{AND}, \sim \text{XOR}\)).

Fig. 3. Regular 16-b SQRT CSLA.[1]
VI. AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA

![Diagrams showing the modified 16-bit SQRT CSLA with BEC](image)

The structure of the proposed 16-bit SQRT CSLA using BEC for RCA with cin=1 to optimize the area and power is shown in Fig. 5. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 6. The steps leading to the evaluation are given here.

1) The group2 [see Fig. 6(a)] has one 2-b RCA which has 1 FA and 1 HA for cin=0. Instead of another 2-b RCA with cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA.

Based on the consideration of delay values of Table I, the arrival time of selection input c1[t=6:3] mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) For the remaining group’s the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC’s.

![Diagrams showing the modified 16-bit SQRT CSLA with BEC](image)

Fig. 5. Modified 16-b SQRT CSLA. The parallel RCA with cin=1 is replaced with BEC

<table>
<thead>
<tr>
<th>GROUP</th>
<th>AREA</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUP2</td>
<td>57</td>
</tr>
<tr>
<td>GROUP3</td>
<td>87</td>
</tr>
<tr>
<td>GROUP4</td>
<td>117</td>
</tr>
<tr>
<td>GROUP5</td>
<td>147</td>
</tr>
</tbody>
</table>

**TABLE II. Area tabulation of regular 16-bit csla**

\[
\text{Gate count} = 57 \times (\text{FA} + \text{HA} + \text{Mux}) \\
\text{FA} = 39(3 \times 13) \\
\text{HA} = 6(1 \times 6) \\
\text{Mux} = 12(3 \times 4).
\]

\[
\text{Gate count} = 43 \times (\text{FA} + \text{HA} + \text{Mux} + \text{BEC}) \\
\text{FA} = 13(1 \times 13) \\
\text{HA} = 6(1 \times 6) \\
\text{AND} = 1 \\
\text{NOT} = 1 \\
\text{NOR} = 10(2 \times 5) \\
\text{Mux} = 12(3 \times 4).
\]
VII. MODIFICATION DONE IN XOR GATE

In this paper we are considering in detail about the xor gate. In here, existing xor gate having 2 AND gates, 2 NOT gates and 1 OR gate. So the expression used in here is

\((\text{NOT}(A) \text{ AND } B) \text{ OR } (A \text{ AND } \text{NOT}(B))\).

This expression is changed to

\((\text{NOT}(A \text{ AND } B)) \text{ AND } (A \text{ OR } B)\)

Thus when drawing the schematic we can understand that one inverter is reduced. When we use this expression in regular and modified 16-bit SQRT CSLA, the area and power will get reduced in both.

VII.a) EXISTING XOR GATE

Gate count:
AND gate=2
OR gate=1
Not gate=2
Total=5

VII.b) SCHEMATIC DIAGRAM

![Schematic diagram](image)

. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.
3) The area count of group 2 is determined above and the table is shown below.

TABLE.III. Area tabulation of modified 16-bit csla

<table>
<thead>
<tr>
<th>GROUP</th>
<th>AREA</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUP2</td>
<td>43</td>
</tr>
<tr>
<td>GROUP3</td>
<td>61</td>
</tr>
<tr>
<td>GROUP4</td>
<td>84</td>
</tr>
<tr>
<td>GROUP5</td>
<td>107</td>
</tr>
</tbody>
</table>

![Schematic diagram of existing xor gate](image)
VII.c) LAYOUT

VIII. MODIFIED XOR GATE

Gate count:
AND gate=2
OR gate=1
NOT gate=1
Total=4

VIII.a) SCHEMATIC DIAGRAM

IX. COMPARISON

Comparison of Regular and Modified 16-BIT SQRT CSLA using new xor gate is done in terms of area. And the power of both xor gate is compared.

<table>
<thead>
<tr>
<th>GROUP</th>
<th>REGULAR</th>
<th>MODIFIED</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUP1</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>GROUP2</td>
<td>50</td>
<td>38</td>
</tr>
<tr>
<td>GROUP3</td>
<td>76</td>
<td>58</td>
</tr>
<tr>
<td>GROUP4</td>
<td>102</td>
<td>78</td>
</tr>
<tr>
<td>GROUP5</td>
<td>128</td>
<td>98</td>
</tr>
</tbody>
</table>

TABLE III. Comparison of area

Fig.8. Layout of existing xor gate

Fig.10. Layout of modified xor gate

Fig.9. Schematic diagram of modified xor gate
AREA COUNT FOR GROUP 2
REGULAR
FA=33(3*11)
HA=5(1*5)
MUX=12(3*4)
TOTAL=50
MODIFIED
FA=11(1*11)
HA=5(1*5)
NOT=1
XOR=8(2*4)
AND=1
MUX=12(3*4)
TOTAL=38

TABLE IV. Comparison of power

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXISTING XOR GATE</th>
<th>MODIFIED XOR GATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER(μW)</td>
<td>10.068</td>
<td>7.113</td>
</tr>
</tbody>
</table>

X. SIMULATION

A.) WAVEFORM

Fig.11 REGULAR 16-B SQRT CSLA

B.) POWER REPORT

Fig.12 MODIFIED 16-B SQRT CSLA

Fig.13 Power of regular 16-bit csla
C.) DELAY REPORT

<table>
<thead>
<tr>
<th>Data Paths: b00 to c00</th>
<th>Clock No.</th>
<th>Gate</th>
<th>Net</th>
<th>Logical Path (Net Name)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUT(1:2)-l-0</td>
<td>2</td>
<td>0.479</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(3:3)-l-0</td>
<td>2</td>
<td>1.062</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(4:4)-l-0</td>
<td>1</td>
<td>0.704</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(5:5)-l-0</td>
<td>1</td>
<td>0.704</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(6:6)-l-0</td>
<td>1</td>
<td>0.704</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(7:7)-l-0</td>
<td>1</td>
<td>0.704</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>LUT(8:8)-l-0</td>
<td>1</td>
<td>0.704</td>
<td>F/A/0/1/2/1 (F)</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>16.401 ns</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Total REAL time to b00 completion: 4.00 ms
Total CPU time to b00 completion: 3.20 ms

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TABLE.V. Comparison of power and delay

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>REGULAR</th>
<th>MODIFIED</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER(W)</td>
<td>.027</td>
<td>.014</td>
</tr>
<tr>
<td>DELAY(NS)</td>
<td>16.401</td>
<td>20.703</td>
</tr>
</tbody>
</table>
D.) GRAPHS

XI. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay, but the area and power of the 16-b modified SQRT CSLA are significantly reduced respectively. The power and delay of the proposed design show a decrease for 16-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. Thus the modification in XOR gate can further reduces the power and area.

XII. REFERENCES


Fig.17. Graph showing power of existing xor gate

Fig.18. Graph showing power of modified xor gate