MODIFIED 16-BIT LOW POWER AREA EFFICIENT CARRY SELECT ADDER

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Abstract— Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions.By gate level modification of CSLA architecture we can reduce area and power.Based on this modification 16-b square-root CSLA (SQRT CSLA) architecture have been developed. The proposed design has reduced area and power as compared with the regular SQRT CSLA .This work evaluates the performance of the proposed designs in terms of area, power and through Xilinx ISE 13.2(VHDL). And in here modification in XOR gate can further reduce the power and area of both regular and modified carry select adder. Microwind is used to calculate power of xor gate.

Keywords :
Low Power,SQRT CSLA, Area Efficient, BEC.

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . However,the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers (mux).The basic idea of this work is to use Binary to Excess-1 Converter(BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.The modification in xor gate reduces area and can reduce power.

II. LITERATURE REVIEW

Existing system consist of high power & high area. Thus the proposed system reduces the area and power.But existing system consist of high speed than proposed system.Modification done in xor gate can reduce the area and also power.

III.EXISTING SYSTEM

The carry-select adder generally consists of two ripple Carry Adders (RCA) and a Multiplexer . Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two RCA).In order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one.

IV. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1 bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 1 and Table I respectively.

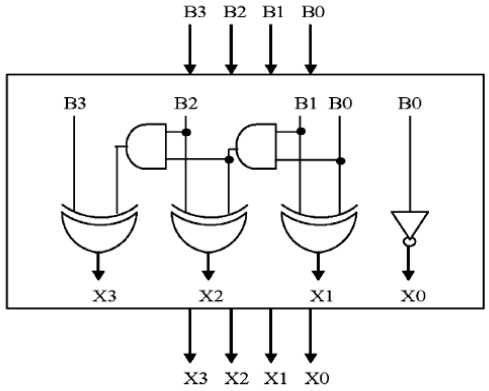

Fig. 1. 4-b BEC.[1]

Table 1. FUNCTION TABLE OF THE 4-b BEC[1]

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

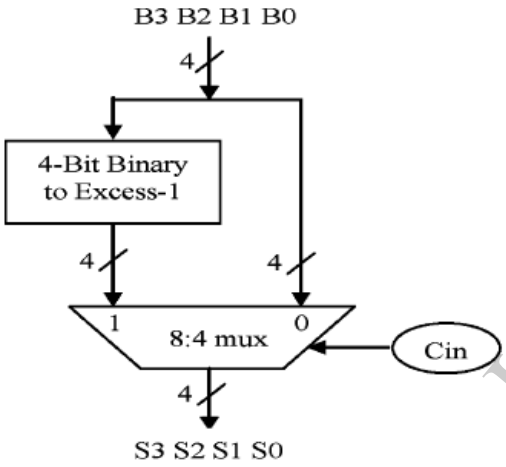

Fig. 2. 4-b BEC with 8:4 mux.[1]

Fig. 2 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BECis listed as (note the functional symbols ~NOT,&AND,^XOR).

$$X0 = \sim B0$$
$$X1 = B0 \hat{} B1$$
$$X2 = B2 \hat{} (B0 \,\&\, B1)$$
$$X3 = B3 \hat{} (B0 \,\&\, B1 \,\&\, B2).$$

V. AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 4, in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows. 1) The group2 [see Fig. 4(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input C1[time(t)=7] of 6:3 mux is earlier than S3[t=8] and later than S2[t=6] Thus, sum3[t=11] is summation of s3 and mux[t=3] and sum2[t=10] is summation of c1 and mux.

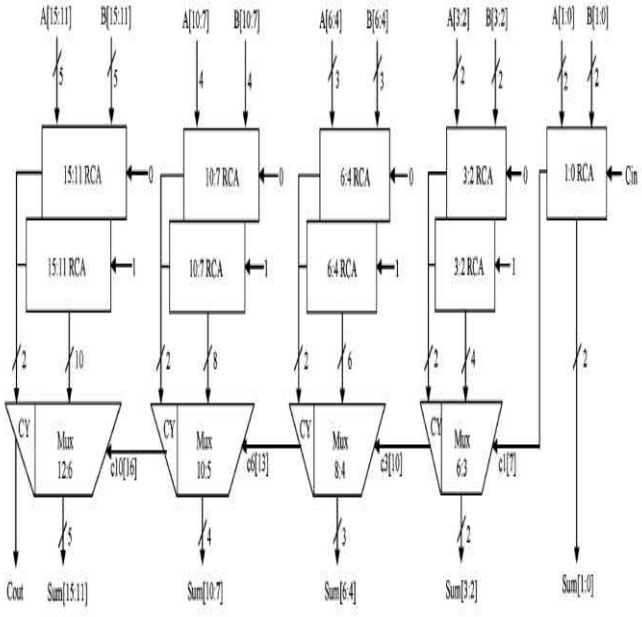

Fig. 3. Regular 16-b SQRT CSLA.[1]

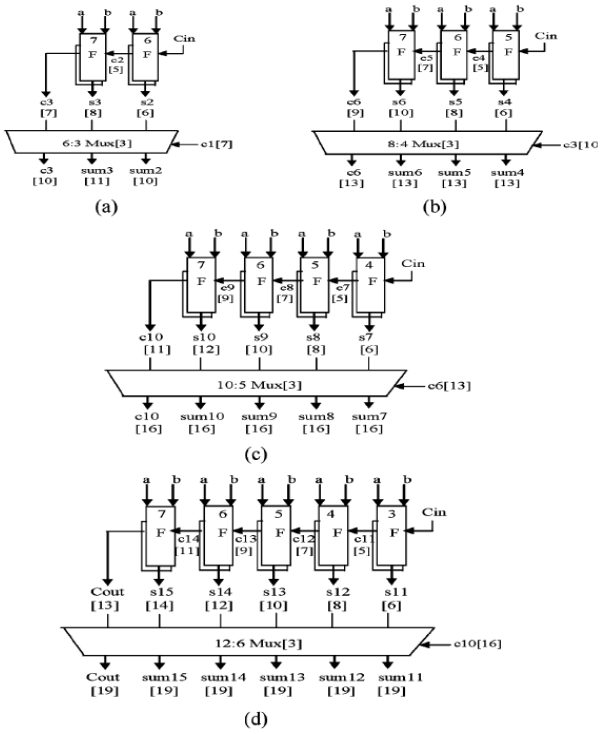

Fig. 4. Delay and area evaluation of regular SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder.[1]

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's.

3) The one set of 2-b RCA in group2 has 2 FA for cin=1 and the other set has 1 FA and 1 HA for cin=0.Based on the area of Table I, the total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57\ (\text{FA} + \text{HA} + \text{Mux})$$
$$\text{FA} = 39(3 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{Mux} = 12(3 * 4).$$

TABLE II.Area tabulation of regular 16-bit csla

GROUP	AREA
GROUP2	57
GROUP3	87
GROUP4	117
GROUP5	147

VI.AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA

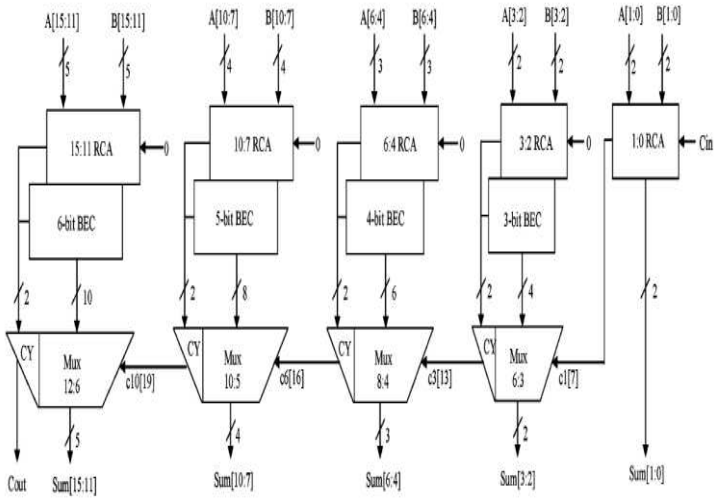

Fig. 5. Modified 16-b SQRT CSLA. The parallel RCA with cin=1 is replaced with BEC

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with cin=1 to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 6. The steps leading to the evaluation
are given here.

1) The group2 [see Fig. 6(a)] has one 2-b RCA which has 1 FA and 1 HA for cin=0 Instead of another 2-b RCA with cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA.

Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's .

$$\text{Gate count} = 43\ (\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$
$$\text{FA} = 13(1 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{AND} = 1$$
$$\text{NOT} = 1$$
$$\text{XOR} = 10(2 * 5)$$
$$\text{Mux} = 12(3 * 4).$$

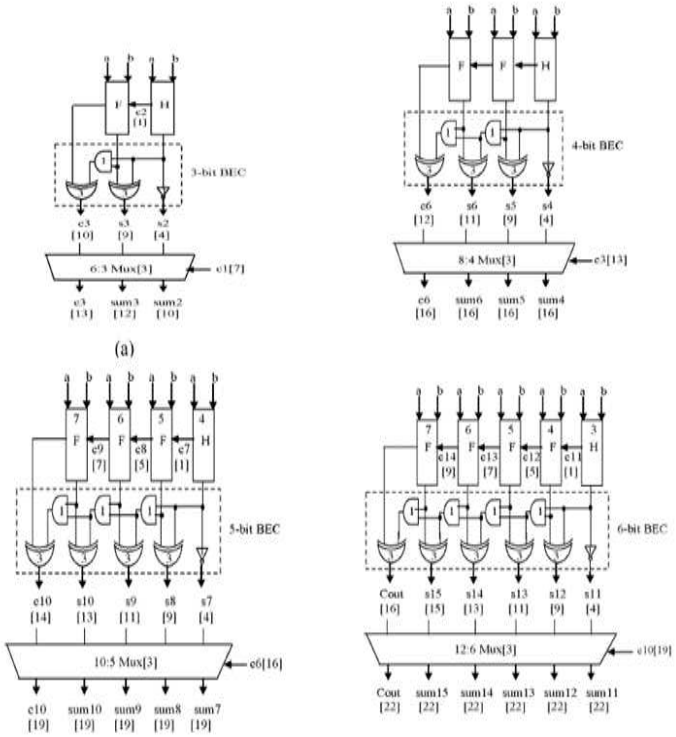

Fig. 6. Delay and area evaluation of modified SQRT CSLA: (a) group2,(b) group3, (c) group4, and (d)group5. H is a Half Adder.

. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group2 is determined above.and the table is shown below

TABLE.III.Area tabulation of modified 16-bit csla

GROUP	AREA
GROUP2	43
GROUP3	61
GROUP4	84
GROUP5	107

VII. MODIFICATION DONE IN XOR GATE

In this paper we are considering in detail about the xor gate.In here, existing xor gate having 2 AND gates,2 NOT gates and 1 OR gate.So the expression used in here is

(NOT(A) AND B) OR (A AND NOT(B)).

This expression is changed to

(NOT(A AND B)) AND (A OR B)

Thus when drawing the schematic we can understand that one inverter is reduced.When we use this expression in regular and modified 16-bit SQRT CSLA,the area and power will get reduced in both.

VII.a) EXISTING XOR GATE

Gate count:
AND gate=2
OR gate=1
Not gate=2
Total=5

VII.b) SCHEMATIC DIAGRAM

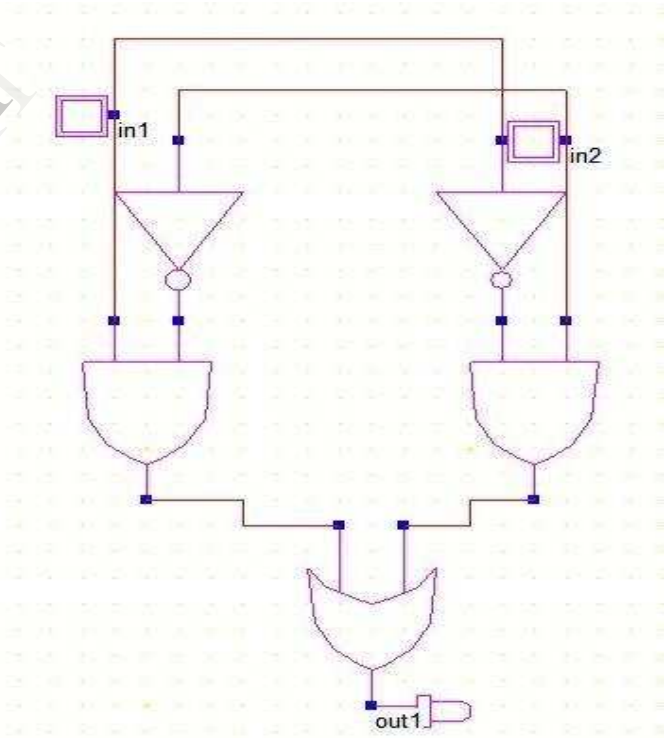

Fig.7.Schematic diagram of existing xor gate

VII.c) LAYOUT

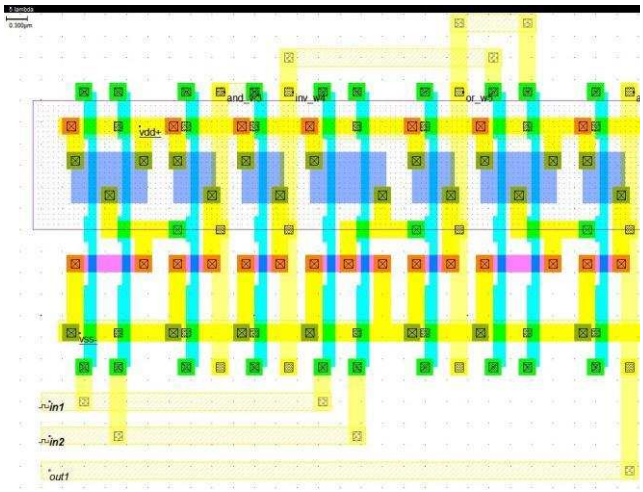

Fig.8.Layout of existing xor gate

VIII. MODIFIED XOR GATE

Gate count:
AND gate=2
OR gate=1
NOT gate=1
Total=4

VIII.a) SCHEMATIC DIAGRAM

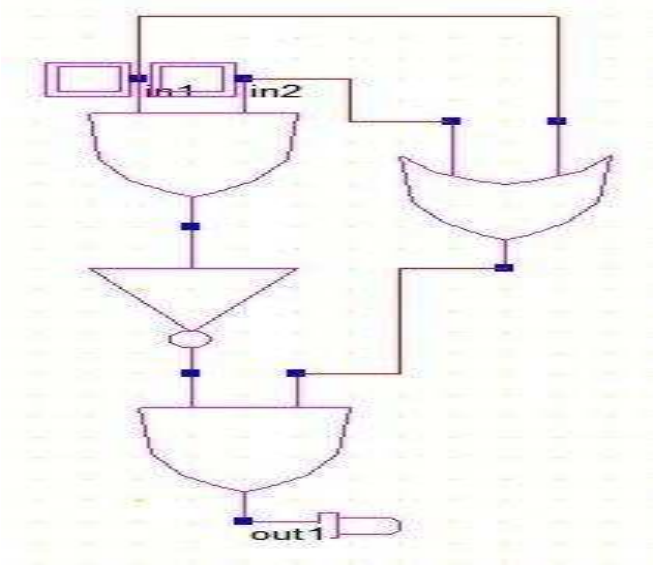

Fig.9.Schematic diagram of modified xor gate

VIII.b) LAYOUT

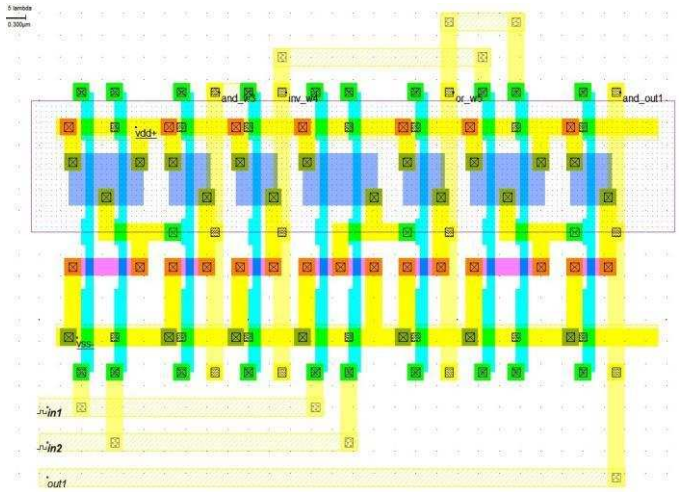

Fig.10.Layout of modified xor gate

IX. COMPARISON

Comparison of Regular and Modified 16-BIT SQRT CSLA using new xor gate is done in terms of area.And the power of both xor gate is compared.

TABLE III.Comparison of area

GROUP	REGULAR	MODIFIED
GROUP1	22	22
GROUP2	50	38
GROUP3	76	58
GROUP4	102	78
GROUP5	128	98

AREA COUNT FOR GROUP 2

REGULAR

FA=33(3*11)

HA=5(1*5)

MUX=12(3*4)

TOTAL=50

MODIFIED

FA=11(1*11)

HA=5(1*5)

NOT=1

XOR=8(2*4)

AND=1

MUX=12(3*4)

TOTAL=38

TABLE IV.Comparison of power

PARAMETER	EXISTING XOR GATE	MODIFIED XOR GATE
POWER(μW)	10.068	7.113

X. SIMULATION

A.) WAVEFORM

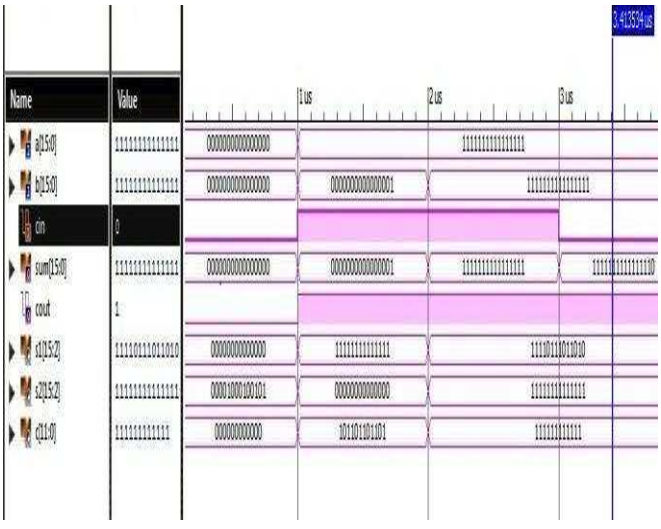

Fig.11 REGULAR 16-B SQRT CSLA

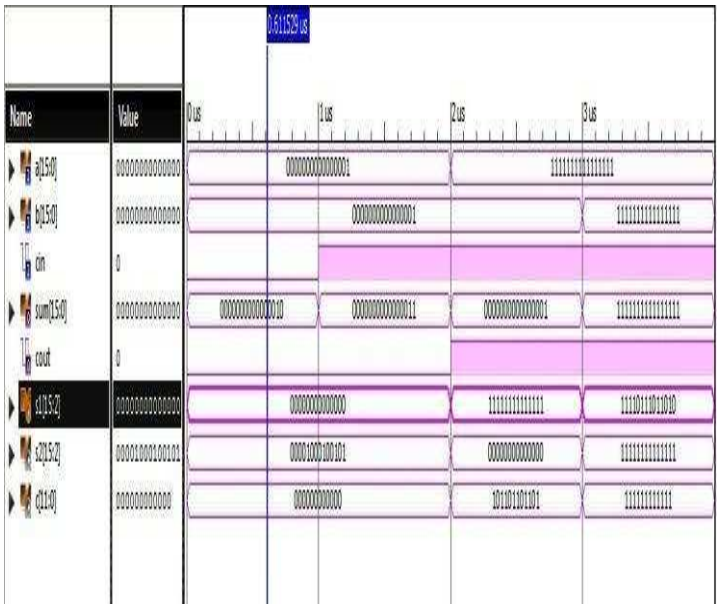

Fig.12. MODIFIED 16-B SQRT CSLA

B.) POWER REPORT

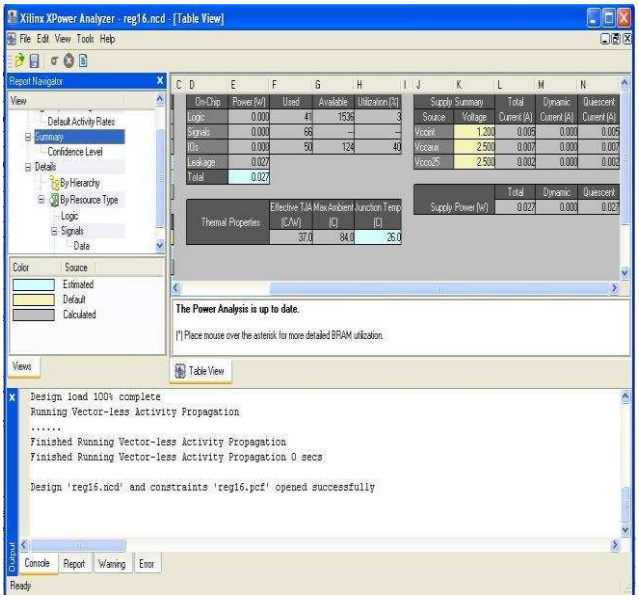

Fig.13..Power of regular 16-bit csla

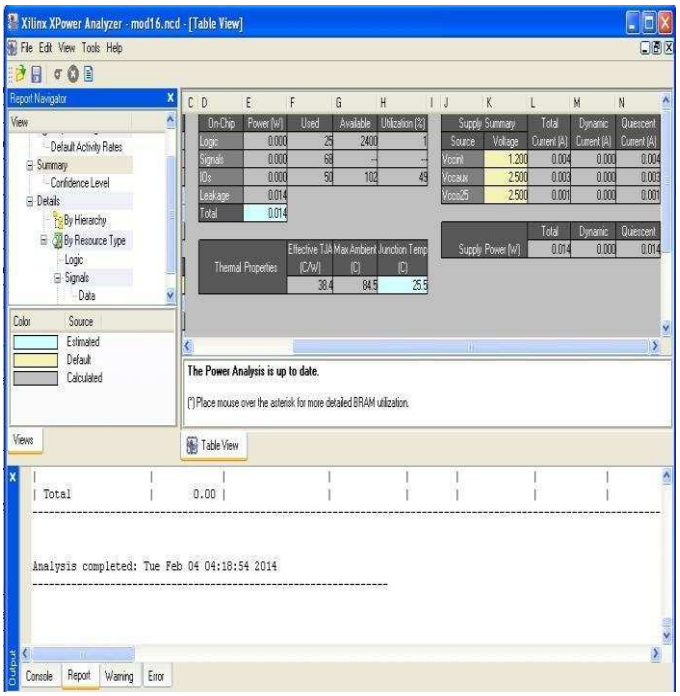

Fig.14.Power of modified 16-bit csla

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================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 585 / 17
--------------------------------------------------------------------------------
Delay:               20.703ns (Levels of Logic = 13)
  Source:            b<0> (PAD)
  Destination:       cout (PAD)

  Data Path: b<0> to cout
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.715   1.040  b_0_IBUF (b_0_IBUF)
     LUT3:I0->O            2   0.479   0.915  F1/A0/cout1 (F1/c)
     LUT3:I1->O            2   0.479   0.915  F1/A1/cout1 (c<0>)
     LUT3:I1->O            2   0.479   0.915  M2/y11 (N3)
     LUT3:I1->O            3   0.479   0.771  M3/y1 (c<3>)
     MUXF5:S->O            2   0.540   0.915  M4/y1_f5 (N2)
     LUT3:I1->O            4   0.479   0.949  M7/y1 (c<6>)
     LUT4:I1->O            2   0.479   0.804  M8/y128 (M8/y128)
     LUT4:I2->O            8   0.479   1.091  M12/y1 (c<9>)
     LUT4:I1->O            1   0.479   0.000  M13/y11 (M13/y1)
     MUXF5:I1->O           2   0.314   0.915  M13/y1_f5 (NO1)
     LUT3:I1->O            1   0.479   0.681  M18/y1 (cout_OBUF)
     OBUF:I->O                 4.909          cout_OBUF (cout)
    ----------------------------------------
    Total                     20.703ns (10.789ns logic, 9.914ns route)
                                       (52.1% logic, 47.9% route)

================================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.06 secs

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Fig.16.Delay of modified 16-bit csla

C.) DELAY REPORT

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================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 788 / 17
--------------------------------------------------------------------------------
Delay:               16.401ns (Levels of Logic = 9)
  Source:            a<8> (PAD)
  Destination:       cout (PAD)

  Data Path: a<8> to cout
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.715   1.040  a_8_IBUF (a_8_IBUF)
     LUT4:I0->O            2   0.479   0.804  F4/A1/cout1 (F4/c<1>)
     LUT3:I2->O            2   0.479   1.040  F4/A2/Mxor_sum_Result1 (s1<9>)
     LUT4:I0->O            3   0.479   1.066  B3/e_4_and000011 (B3/e_3_and000
     LUT4:I0->O            1   0.479   0.740  M12/y1_SW0 (N34)
     LUT4:I2->O            7   0.479   1.076  M12/y1 (c<9>)
     LUT4:I1->O            1   0.479   0.976  M18/y1_SW0 (N32)
     LUT4:I0->O            1   0.479   0.681  M18/y1 (cout_OBUF)
     OBUF:I->O                 4.909          cout_OBUF (cout)
    ----------------------------------------
    Total                     16.401ns (8.977ns logic, 7.424ns route)
                                       (54.7% logic, 45.3% route)

================================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.78 secs

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Total memory usage is 140444 kilobytes
```

Fig.15.Delay of regular 16-bit csla

TABLE.V.Comparison of power and delay

PARAMETERS	REGULAR	MODIFIED
POWER(W)	.027	.014
DELAY(NS)	16.401	20.703

D.) GRAPHS

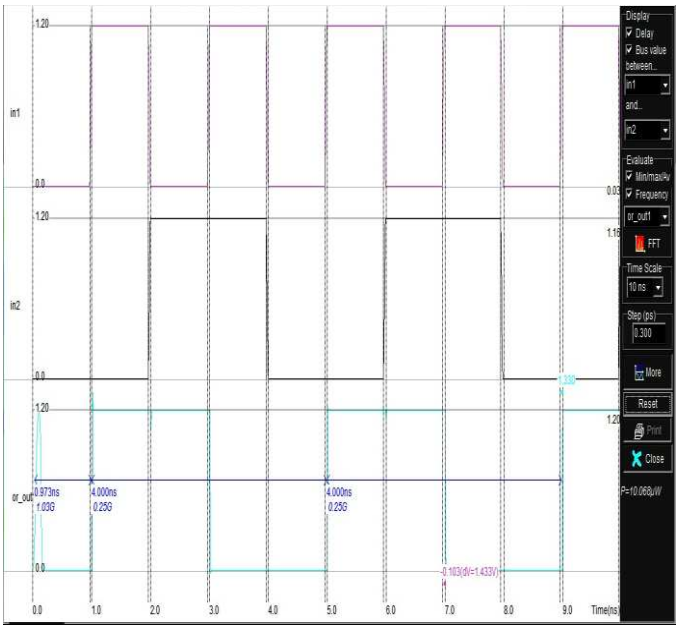

Fig.17.Graph showing power of existing xor gate

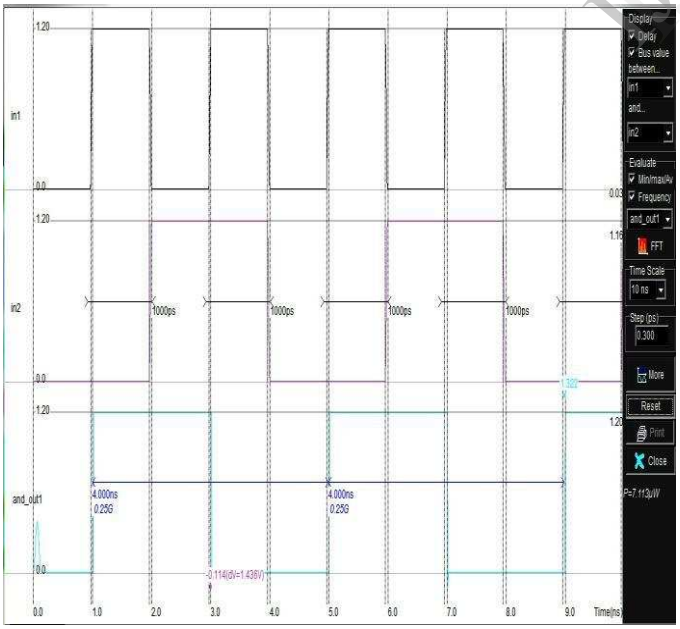

Fig.18.Graph showing power of modified xor gate

XI. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay, but the area and power of the 16-b modified SQRT CSLA are significantly reduced respectively. The power and delay of the proposed design show a decrease for 16-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. Thus the modification in XOR gate can further reduces the power and area.

XII. REFERENCES

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