

Modelling & Simulation of Five Level Diode Clamped Inverter for Reduction of Common Mode Voltage in Induction Motor Drive

Mr. Prafulla J. Kale

Dept. of Electrical Engineering,
Govt. College of Engineering,
Aurangabad (M.S), India

Dr. Vandana Deodhar-Kulkarni

Dept. of Electrical Engineering
Govt. College of Engineering,
Aurangabad (M.S), India

Miss. Shital Bhad

Dept Of Electrical Engineering,
Priyadarshni college of Engineering,
Nagpur (M.S.), India

Abstract: Recent developments in speed control methods of the induction motor have led to their large scale use in almost all electrical drives. For better performance the High power induction machines are designed at medium voltage (MV) rating. If Single power semiconductor switch is directly connected to medium voltage, it may damage. Also, conventional inverters generate high frequency common mode voltage. Multilevel inverter is an alternative solution for high power & medium voltage A.C. drive. It starts from three levels. The multilevel inverter topology synthesizes a sinusoidal voltage from several levels of voltages obtained from capacitor voltage sources. In this paper, an approach to reduce the common mode voltage (CMV) and Total Harmonic Distortion using five level diode clamped multilevel inverter (DCMLI) for three phase induction motor drive is proposed.

Keywords: CMV, DCMLI, SPWM, THD, MV

I. INTRODUCTION

Inverters are widely used in variable speed drives because of their ability to control the magnitude & frequency of the output voltage. Common mode voltage is main disadvantage of two level inverter. The Shaft voltage and the premature failure of the bearings is mainly effect of CMV [1]. The simultaneous switching of the series connected devices generates voltage with a high dv/dt at the output terminal of the inverter [2]. Hence, in the applications of AC motor drives, the analysis of the common mode voltage is important. A MLI can reduce as well as eliminate the CMV & reduces harmonic distortion at low switching frequency. Among the configurations of multilevel inverter, 5-level diode clamped multilevel inverters have some advance features hence simulation is performed using FLDCl & simulation results show that it reduces CMV as well as THD [3].

II. MULTILEVEL INVERTER

The basic structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically gain from capacitor voltage sources. "Multilevel" starts from three levels. The concept of multilevel inverter control is an alternative solution for induction motor which is operated to achieve performance equally that of dc motors. The main multilevel configuration is classified into three types: diode clamped inverters, flying capacitor inverters and cascaded inverters.

III. DIODE CLAMPED MULTILEVEL INVERTER

The number of main switches in each topology is equal. Comparison with other types, diode clamped inverters require less number of capacitors but require additional clamping diodes. Hence the diode clamped multilevel structure is better for high and medium voltage drives which are easily connected to the utility drive. The Diode Clamped Multilevel Inverter typically consists of $(m-1)$ capacitors on the DC bus in which m is the total number of positive, negative and zero levels in the output voltage. Figure 1 shows a three phase half-bridge five level diode clamped inverter. The order of numbering of the switches for phase x is S_{a1} , S_{a2} , S_{a3} , S_{a4} , $S_{a1''}$, $S_{a2''}$, $S_{a3''}$ and $S_{a4''}$ and likewise for other two phases. The DC bus consists of four capacitors C_1 , C_2 , C_3 and C_4 act as voltage divider. For a DC bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each (Switch) device is limited to $V_{dc}/4$ through clamping diode. The midpoint of the four capacitors "n" can be defined as the neutral point. Table 1 shows the output voltage levels and the corresponding switch states for one phase of the chosen five levels DCMLI. The switches are arranged into 4 pairs (S_{a1} , $S_{a1''}$), (S_{a2} , $S_{a2''}$), (S_{a3} , $S_{a3''}$), (S_{a4} , $S_{a4''}$). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the required level in the five levels DCMLI.

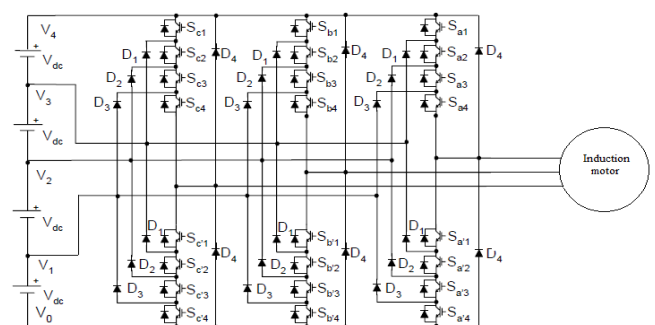


Fig.1 A three phase five level DCMLI

Table I. Switching State and Magnitude of output voltage

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}'	S_{a2}'	S_{a3}'	S_{a4}'	V_{an}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

IV. COMMON MODE VOLTAGE

In the applications of AC motor drives, the analysis of the common mode voltage is important. It is occurs between the neutral point of the star connected motor (node n) to the earth ground (node e), it leads to common mode current. The Shaft voltage and the premature failure of the bearings is mainly effect of CMV. The simultaneous switching of the series connected devices produces voltage with a high dv/dt at the output terminal of the inverter. The sudden rise in inverter voltage hazardous to the motor drive application. It is very important to reduce the CMV and limit this voltage within certain bounds. A MLI can reduce as well as eliminate the CMV. Some approaches to reduce CMV include four leg inverters, passive filters and dual bridge inverters but Five level diode clamped inverter is the best option to reduce CMV. Causes of CMV are leakage current, bearing current & Bearing Failure.

V. MODELING & SIMULATION OF DIODE CLAMPED MULTILEVEL INVERTER

An Inverter fed three phase squirrel cage Induction Motor is used for simulation. Reduction of common mode voltage and Total Harmonic Distortion in Line Voltage is obtained by using Multilevel Inverter as explained in this paper. Analysis of CMV of the Three phase Induction Motor by using different Level Inverter i.e. Two Level Inverter, Three Level Inverter and Five Level Inverter. Here, Two Level Inverter and Three Level Inverter is control by using PWM technique. In Five Level Diode Clamped Inverter, SPWM technique is used to reduce CMV as well as THD.

Module 1: Two Level Inverter Fed Induction Motor

Induction Motor is fed by Conventional Two Level Inverter. Simulation in MATLAB environment has been made for full load torque condition. In these Two Level Inverter, two levels i.e. +300 and -300 of output voltage is obtained. CMV from simulation result of Conventional method is found to be 300V to -300V. From FFF analysis THD is obtained 80.63% in Line Voltage of Two Level Inverter. Here, CMV is high and THD is also more.

Output Voltage of Two Level Inverter

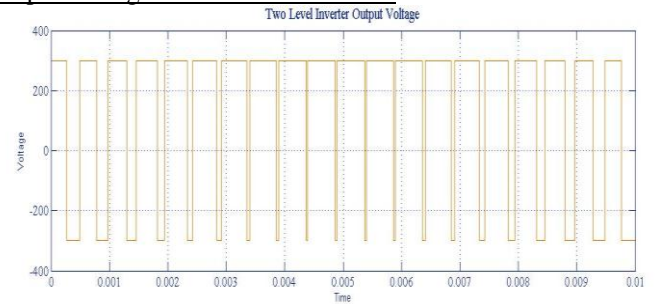


Fig.2 Output Voltage waveform of Two level Inverter

CMV of Two Level Inverter

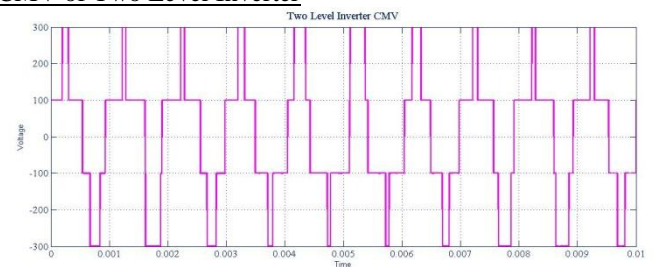


Fig.3 Common Mode Voltage waveform of Two level Inverter

THD of Two Level Inverter

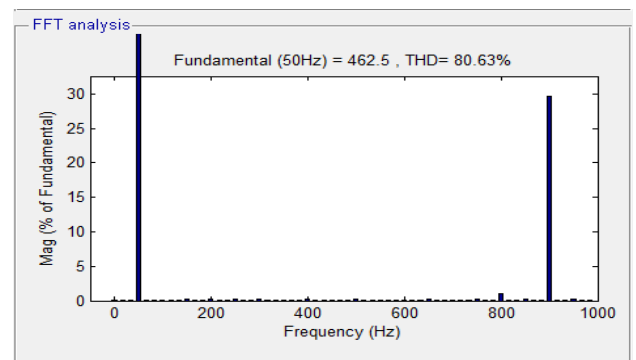


Fig.4 Total Harmonic Distortion of Two level Inverter fed Induction Motor

Module 2: Three Level Inverter Fed Induction Motor

Induction Motor is fed by Three Level Inverter. Simulation in MATLAB environment has been made for three fourth load torque condition. In this Module of Three Level Inverter should get three levels of output voltage and $\pm V_{dc}/3$ CMV.

Output Voltage of Three Level Inverter

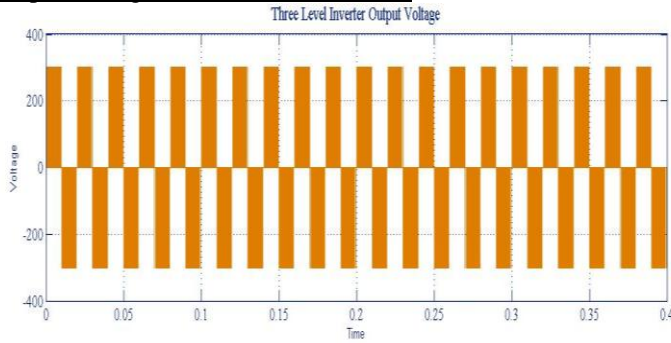


Fig.5 Output Voltage waveform of Three Level Inverter

CMV of Three Level Inverter

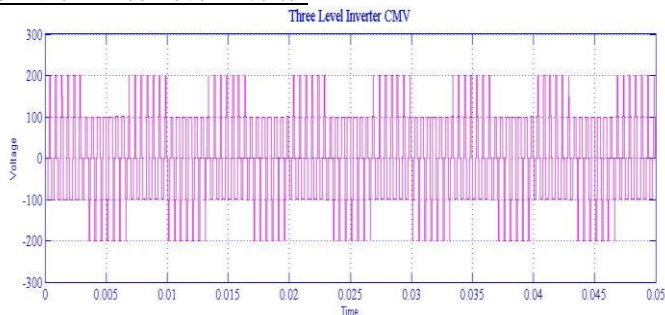


Fig.6 Common Mode Voltage waveform of Three Level Inverter

THD of Three Level Inverter

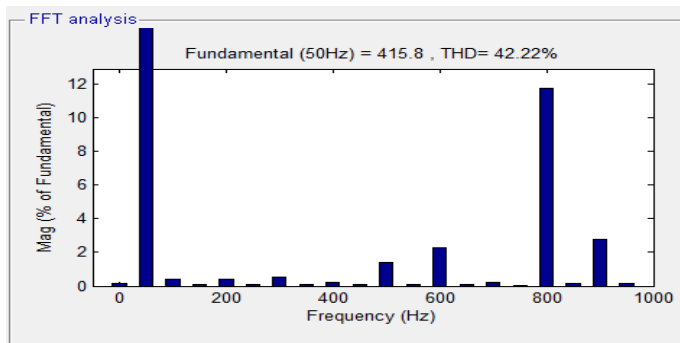


Fig.7 Total Harmonic Distortion of Three Level Inverter

From Three Level Inverter output waveform three levels i.e. -300V, 0V and +300V of output voltage is obtained. Three Level Inverter is operate in 27 switching states. The CMV varies from -200V to +200V can be observed from waveform of CMV of Three Level Inverter. From FFF analysis THD is obtained 42.22% in Line Voltage of Two Level Inverter. Here, comparison with Two Level Inverter CMV & THD is decreases.

Module 3: Five Level Diode Clamped Multilevel Inverter Fed Induction Motor

Induction Motor is fed by Five Level Diode Clamped Inverter. Simulation in MATLAB environment has been made for full load torque condition. In this Module of Five Level Diode Clamped Inverter should get five levels of output voltage and $\pm V_{dc}/12$ CMV.

Output voltage of five level Diode Clamped inverter

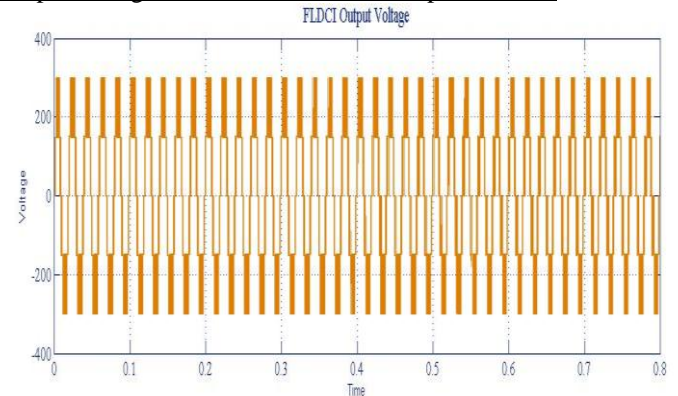


Fig.8 Output Voltage waveform of FLDC Inverter

CMV of FLDC Inverter

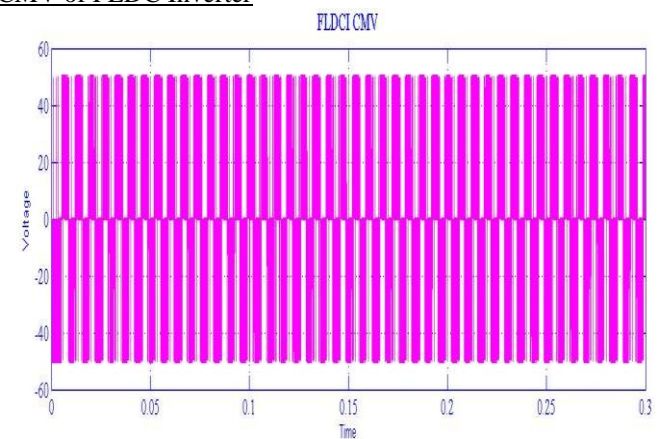


Fig.9 Common Mode Voltage waveform of FLDCI

THD of Output of FLDC Inverter

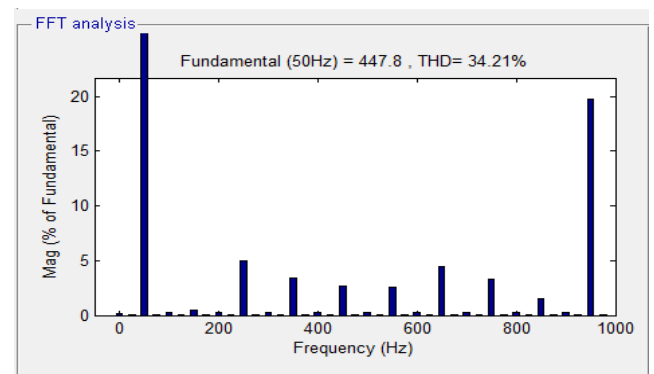


Fig.10 Total Harmonic Distortion of FLDCI

From Five Level Diode Clamped Inverter output waveform, five levels i.e. -300V, -150, 0V, +150 and +300V of output voltage is obtained. Five Level Inverter is operate in 125 switching states. The CMV varies from -50V to +50V can be observed from waveform of CMV of Five Level Diode Clamped Inverter. From FFF analysis THD is obtained 34.21% in Line Voltage of Five Level Diode Clamped Inverter.

TABLE II
COMPARISON OF TOTAL HARMONIC DISTORTION
IN LINE VOLTAGE AND COMMON MODE
VOLTAGE

	THD in Line Voltage	CMV
Two Level Inverter	80.51%	$\pm V_{dc}/2$
Three Level Inverter	42.14%	$\pm V_{dc}/3$
FLDC Inverter	34.21%	$\pm V_{dc}/12$

Here, CMV is decreases as compare to CMV of Two Level and Three Level Inverter. THD is also decreases as compare to Two Level and Three Level Inverter.

VI.CONCLUSION:

In this Paper the simulation results of three phases Two Level Inverter, Three Level Inverter & five level diode clamped inverter fed Induction Motor load are obtained through MATLAB/SIMULINK. The CMV has been found to be major cause of premature failure of motor bearings and windings. Multilevel inverter reduces the CMV, dv/dt & leakage current which are responsible for premature failure of bearing and winding. As the level of Inverter goes on increasing it has been observed that the CMV and Total Harmonic Distortion decreases. This topology can be applied to medium voltage & low voltage drives to increase the life of bearing of motor and improves the reliability of motor.

REFERENCES

- [1] C. Bharatiraja, S. Raghu, Prakash Rao, K.R.S. Paliniyamy, "Comparative Analysis of the Different PWM Techniques to Reduce Common Mode Voltage in Three- Level Neutral- Point- Clamped Inverters for Variable Speed Induction Drives", *International Journal of Power Electronics and Drive System*, Vol. 3, No. 1, Marc 2013, pp. 105-116.
- [2] M. M. Renge, and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans Power Electron.*, Vol. 23, No. 4, pp. 1598-1607, Jul. 2008.
- [3] Mohan M. Renge and Hiralal M. Suryawanshi "Multilevel Inverter to Reduce Common Mo- Voltage in AC Motor Drives Using SPWM Technique", *Journal of Power Electronics*, Vol. 11, No. 1, January 2011, 2006, pp.21-27.
- [4] C. R. Balamurugan, S. P. Natarajan, R. Bensraj "Investigations on Three Phase Five Level Diode Clamped Multilevel Inverter ". *International Journal of Modern Engineering Research*, Vol.2, Issue.3, May-June 2012 pp-1273-1279.
- [5] Chenggang Mei, Juan Carlos Balda, and William P. Waite, "Cancellation of common-mode voltages for induction motor drives using active method," *IEEE Trans. Energy Conversion*, Vol.21, No. 2, pp. 380-386, Jun. 2006.
- [6] Hirofui Akagi, and Shunsuke Tamura, "A Passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Trans. Power Elctron.*, Vol. 21, No. 5, pp. 982-989, Sep. 2006.
- [7] K. Gupta and A. M. Khambadkone, "A general space vector PWM algorithm for multilevel inverters, including operation in over modulation range," *IEEE Tra Power Elec tron.*, Vol. 22, No. 2, pp. 517-526, Mar. 2007.
- [8] Haoran Zhang, Annette Von Jouanne, and Shaoan Dai, "A reduced switched dual bridge inverter topology for the mitigation of bearing current, EMI, and dc voltage variation", *IEEE Trans. Ind. Appl.*, vol. 37, No. 5, pp 1365-1372, Sep./Oct. 2001.
- [9] Gopal Mondal, K. Gopakumar, P. N. Tekwani, and Emil Levi, "A reduced- switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *IEEE Trans. on Indl. Electron.*, Vol. 54, No. 4, pp. 2344-2351, Aug 2007.
- [10] P. Chiang, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "A reduced common mode hysteresis current regulation strategy for multilevel inverter," *IEEE Trans Power Electron.*, vol. 19, no. 1, pp. 1992-2000, Jan. 2004.