Modelling of Four Switch Buck Boost Dynamic Capacitor

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Abstract—**This paper presents a novel VAR technology Four-Switch Buck-Boost Dynamic Capacitor which promises to combine the performance of the AC/AC buck and boost cells into a single power electronic device This is done in an effort to reduce the required component count and thus reduce the overall device footprint and implementation cost of the Dynamic Capacitor technology. Derivations and analysis will detail the workings of the Four-Switch Buck-Boost Dynamic Capacitor, while simulations will demonstrate the functionality and performance of the proposed topology.**

Keywords— VAR Technology, SVC, Statcom, Dynamic Capacitor, Shunt Reactive Compensation

I.   INTRODUCTION

Four-Switch Buck-Boost Dynamic Capacitor is a relatively new VAR topology like SVC or STATCOM technologies that offers various advantages over its predecessors [1]. The motivation behind exploring this topology is that it promises to combine the performance of both the buck and boost D-Cap devices into a single power electronic converter. By doing so, full capacitive VAR control can be achieved using fewer components, thus making the D-Cap an even more affordable technology [2][3].

At the core of the 4-Switch Buck-Boost Dynamic Capacitor is the 4-Switch Buck-Boost Converter [4]. While this converter topology is not new, its implementation as an AC/AC converter as well as a shunt reactive compensation device are both novel concepts [5].
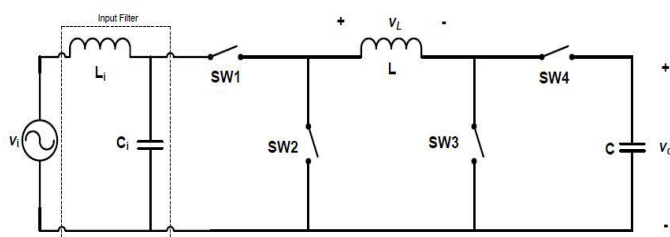

Fig 1. 4SWBB D-Cap(with Input Filter Shown)

Looking at Figure 1 above one can see that by closing switch SW4, leaving switch SW3 open and modulating switches SW1 and SW2 by D and (1-D) respectively, the 4SWBB D-Cap would essentially behave just like the Buck Cell D-Cap. Conversely by closing switch 1, leaving switch 2 open and modulating switches 3 and 4 by D and (1-D) respectively, the

4SWBB D-Cap would essentially behave just like the Boost Cell D-Cap [6].

To prove the 4SWBB D-Cap's shunt reactive compensation capabilities, it is desired to model it after an existing output characteristic. The design characteristics for the 4SWBB D-Cap as pertaining to this paper will thus be to provide +240 MVAR at a rated line-to-line voltage of 115 kV. Furthermore, the 4SWBB D-Cap will be designed such that it will be capable of providing full VAR output during a voltage depression (up to 20%) at the connected bus [7].

II.   CONTROLLER

In order for the 4-Switch Buck-Boost Dynamic Capacitor to function as desired, a controller is needed. To provide shunt VAR compensation the controller will monitor the voltage at the bus where the compensation is desired. This measurement will be compared with a reference voltage set to the nominal bus voltage. The comparison between the two voltages determines the action taken by the controller as discussed below:

A. $V_{bus} < V_{ref}$

The VAR output in this mode is at its maximum. Once Dbuck=1 the D-Cap will switch to boost mode and start increasing Dboost to provide additional VARs until the system is compensated or the maximum VAR output of the converter has been reached (Dboost-max)

B. $V_{bus} > V_{ref}$

In this case there is an excess amount of capacitive VARs in the system thus causing the bus voltage to rise above its nominal value. To correct this, the D-Cap must reduce the amount of capacitive VARs that it is injecting. While the D-Cap is in boost mode the controller will decrease the duty cycle until the bus voltage is back to normal or D_{boost}=0. Once D_{boost}=0 the D-Cap will switch to buck mode and start decreasing the duty cycle until the bus voltage is back to normal or D_{buck}=0 at which point the D-Cap is not inputting any VARs.

C. $V_{bus} = V_{ref}$

During this case no additional compensation is needed thus the current switching signals are left as is.

III.   SYSTEM DESIGN AND COMPONENT SELECTION

A. Transfer Function Derivations

As with any other power electronic devices, the 4SWBB has a set of equations which characterize its basic operation and function. We assume that the Converter will operate in Continuous Conduction mode. Furthermore the switching frequency of this converter will be chosen to be much higher than the system frequency of 60 Hz, thus during any given switching period the input voltage and current will approximately remain constant.

1.   Buck Mode

In buck mode switch SW3 remains open, switch SW4 remains closed, and switch SW1 and SW2 are modulated according to D and (1-D) respectively.

It is worthy to note that since we are dealing with an AC/AC converter the input voltage has the form $v_i(t) = V_i sin(wt)$, however as previously mentioned, $f_{sw} \gg f_{sys}$ therefore during any given switching period (T_{sw}) the value for t and thus $v_i(t)$ is relatively constant. During the time interval $kT_{sw} \rightarrow (k+D)T_{sw}$ switch SW1 is closed, switch SW2 is open and the D-Cap performs according to the following equations:

$$v_L(t) = v_i(t) - v_0(t) \tag{1}$$

$$v_L(t) = L \frac{di_L(t)}{dt} \tag{2}$$

$$i_i(t) = i_L(t) = i_0(t) \tag{3}$$

$$\Delta i_L = \frac{v_i(t) - v_o(t)}{L} DT \tag{4}$$

During the time interval $(k+D)T_{sw} \rightarrow (k+1)T_{sw}$ the D-Cap behaves according to the following equations:

$$v_L(t) = -v_0(t) \tag{5}$$

$$i_i(t) = 0 \tag{6}$$

$$i_0(t) = i_L(t) \tag{7}$$

$$\Delta i_L = \frac{-v_o(t)}{L}(1-D)T \tag{8}$$

From equations (3), (6) and (7) we can describe the currents for the Buck mode with the general equations below:

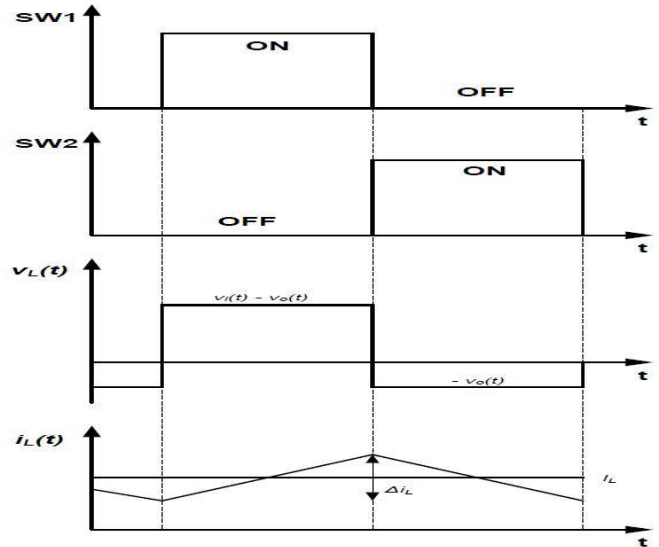$$i_i(t) = D * i_L(t) \tag{9}$$

$$i_0(t) = i_L(t) \tag{10}$$

Fig 2.Inductor voltage and current waveforms in Buck mode

To derive a steady state transfer function for the buck mode we take a look at the average inductor voltage over an entire switching period. Using equations (1) and (5) this can be seen to be:

$$v_L(t) = [v_i(t) - v_0(t)]D + [-v_0(t)](1-D)$$

Reducing the right hand side and plugging in equation (2) on the left, this expression becomes:

$$L \frac{di_L(t)}{dt} = D v_i(t) - v_0(t)$$

Plugging in (9) for $i_L(t)$ and through some rearranging of terms we get the equation below:

$$D v_i(t) = \frac{L}{D} \frac{di_i(t)}{dt} + v_0(t) \tag{11}$$

Using equation (11) the steady state equivalent circuit for the buck mode 4SWBB D-Cap can be modeled as shown in Figure 3.
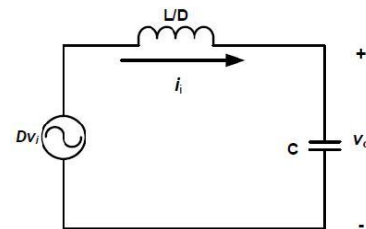

Fig 3.Steady State Equivalent circuit in Buck Mode

By applying ohms law, the input current is given by:

$$i_i(t) = \frac{D v_i(t)}{Z eq} \tag{12}$$

Where

$$Z eq = \frac{Z_L}{D} + Z_c = \frac{j\omega L}{D} + \frac{1}{j\omega C}$$

By knowing the impedance of the capacitor and the current flowing through it, the expression for the output voltage in terms of the input voltage is derived

$$v_0(t) = i_i(t) * Z_c = \frac{D v_i(t)}{(1 - \frac{\omega^2 LC}{D})} \qquad (13)$$

2. Boost Mode

While in buck mode switch SW1 remains closed, switch SW2 remains open, and switch SW3 and SW4 are modulated according to D and (1-D) respectively

During the time interval $kTsw \rightarrow (k+D)Tsw$ switch SW3 is closed, switch SW4 is open and the D-Cap performs according to the following equations:

$$v_L(t) = v_i(t) \qquad (14)$$

$$v_L(t) = L\frac{di_L(t)}{dt} \qquad (15)$$

$$i_i(t) = i_L(t) \qquad (16)$$

$$i_0(t) = 0 \qquad (17)$$

$$\Delta i_L = \frac{v_i(t)}{L} DT \qquad (18)$$

During the time interval $(k+D)Tsw \rightarrow (k+1)Tsw$ switch SW3 is open, switch SW4 is closed and the D-Cap is defined by the following equations:

$$v_L(t) = v_i(t) - v_0(t) \qquad (19)$$

$$i_i(t) = i_L(t) = i_0(t) \qquad (20)$$

$$\Delta i_L = \frac{v_i(t) - v_0(t)}{L}(1 - D)T \qquad (21)$$

From equations (16), (17) and (20) we can describe the currents for the Buck mode with the general equations below:

$$i_i(t) = i_L(t) \qquad (22)$$

$$i_0(t) = (1 - D) * i_L(t) \qquad (23)$$

As in the case of the buck mode, steady state transfer function given by:

$$v_L(t) = [v_i(t)]D + [v_i(t) - v_0(t)](1 - D)$$

Reducing the right hand side and plugging in equation (15) on the left, this expression becomes:

$$L\frac{di_L(t)}{dt} = v_i(t) - (1 - D)v_0(t)$$

Plugging in (22) for $i_L(t)$ and through some rearranging of terms we get the equation below:

$$\frac{v_i(t)}{1 - D} = \frac{L}{1 - D}\frac{di_i(t)}{dt} + v_0(t) \qquad (24)$$

Using equation (24) the steady state equivalent circuit for the boost mode 4SWBB D-Cap can be modeled as shown in Figure 4.
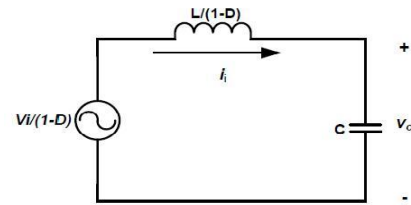

Fig 2.Steady State Equivalent Circuit in Boost Mode

By applying ohms law the input current is given by:

$$i_i(t) = \frac{v_i(t)}{(1 - D)Z_{eq}} \qquad (25)$$

Where

$$Z_{eq} = \frac{Z_L}{1 - D} + Z_C = \frac{J\omega L}{1 - D} + \frac{1}{j\omega C}$$

By knowing the impedance of the capacitor and the current flowing through it, the expression for the output voltage is derived:

$$v_0(t) = i_i(t) * Z_c = \frac{v_i(t)}{(1 - D)(1 - \frac{\omega^2 LC}{1 - D})} \qquad (26)$$

Looking at the transfer functions for both the buck and boost mode one can see that they have very similar terms in the denominator.

$$\left(1 - \frac{X_L}{X_C D}\right)[Buck]$$

$$\left(1 - \frac{X_L}{X_c(1 - D)}\right)[Boost]$$

By choosing component values such that $X_C \gg X_L$ the right hand term for both the equations above will be very small. Therefore, these constants will be approximately equal to 1 and the transfer functions become:

$$v_0(t) = D v_i(t) \qquad (27)$$

$$v_0(t) = \frac{v_i(t)}{(1 - D)} \qquad (28)$$

The transfer functions shown equations (27) and (28), are then identical to the transfer functions of the individual DC/DC buck and DC/DC boost converters respectively. Using equation (27) the equation describing the capacitor current for buck mode would then be:

$$i_c(t) = i_L(t) = \frac{v_0(t)}{X_c}\omega CD v_i(t) \qquad (29)$$

Using equation (9) the resulting input current would be:

$$i_i(t) = Di_c(t) = \omega CD^2 v_i(t) \qquad (30)$$

In buck mode, this effective capacitance is calculated as shown below:

$$X_{Ceff-buck} = \frac{v_0(t)}{i_i(t)} = \frac{D v_i(t)}{\omega C D^2 v_i(t)} = \frac{1}{\omega CD}$$

$$C_{eff-buck} = \frac{1}{\omega X_{Ceff-buck}} = CD \tag{31}$$

Using equation (28) the equation describing the capacitor current for boost mode would then be:

$$i_c(t) = = \frac{v_0(t)}{X_C} = \frac{\omega C v_i(t)}{(1-D)} \tag{32}$$

Using equation (23) the resulting input current would be:

$$i_i(t) = \frac{i_c(t)}{(1-D)} = \frac{\omega C v_i(t)}{(1-D)^2} \tag{33}$$

The effective shunt capacitance that the 4SWBB D-Cap supplies to the system while in boost mode is calculated as shown below:

$$X_{Ceff-boost} = \frac{v_0(t)}{i_i(t)} = \frac{v_i(t)(1-D)^2}{(1-D)\omega C v_i(t)} = \frac{(1-D)}{\omega C}$$
$$C_{eff-boost} = \frac{1}{\omega X_{ceff-boost}} = \frac{C}{(1-D)} \tag{34}$$

B. Dboost-max Selection:

From the derivations in the section above it is seen that while the converter is in boost mode the voltage output increases towards infinity as the duty cycle approaches a value of 1. However, when the converter reaches a duty cycle of 1, SW3 is always closed while SW4 remains open thus effectively shorting the voltage input to ground. This of course is highly undesirable and therefore it is convenient to limit the Duty Cycle of the Boost mode to a specified design value. As mentioned for this paper it is desired for the 4SWBB D-Cap to have the capability of outputting full VARs up to a voltage depression of 20%. Therefore the value of Dboost-max is selected such that during a system voltage drop of 20% the converter can increase the voltage across the capacitor to a value equal to the nominal system input voltage. To do this Dboost-max is chosen to be 0.2 or 20%. To illustrate this point the nominal system voltage for this paper is 115kVLL or 66.4kVrms single phase. A 20% voltage reduction would mean an input voltage of 53.12 kVrms. Using equation (28) with Dboost = Dboost-max the voltage across the capacitor would be

$$v_0(t) = \frac{v_i(t)}{(1-D)} = \frac{53.12}{1-0.2} = 66.4 KVrms$$

C. Capacitor Sizing:

When selecting component values for the 4SWBB D-Cap, the size of the power factor correction capacitor is normally the first to be determined. The amount of reactive power that a capacitor generates is given by:

$$C = \frac{Q}{\omega_{sys} V_{rms}^2} \tag{35}$$

As previously mentioned for the purpose of this paper, it is desired to model a single phase 4SWBB D-Cap which will provide +240 MVAR at rated line-to-line voltage of 115kV

and system frequency of 60Hz. Using equation (32) the capacitance required would be:

$$C = \frac{240}{2 * \pi * 60HZ (115kV_{L-L}\backslash\sqrt{3})^2} = 144\mu F$$

D. Switching Frequency Selection:

In order for the 4SWBB D-Cap to function properly as a capacitive shunt reactive compensator it must be seen as a capacitor by the system. For this reason we want the impedance of the system to be almost purely capacitive. Therefore, the size of the inductor is what must be designed to make this condition true. As will be explained below, the switching frequency is inversely proportional to the size of the inductor needed to maintain CCM, therefore higher switching frequencies are desired. To fulfill these conditions, the switching frequency has been selected to be 20 kHz.

E. Inductor Sizing

1. Buck Mode

The following steps must be taken to calculate the critical inductance during buck mode. Taking Equation (8) and rearranging it such that L is on the right hand side:

$$L = \frac{-v_0(t)}{\Delta i_L}(1-D)T \tag{36}$$

A general definition for the inductor current ripple is that it is twice the average inductor current multiplied by the inductor current ripple coefficient (*ki*).

$$\Delta i_L = 2 * k_i * i_L(t) \tag{37}$$

By inserting Equation (37) into Equation (36):

$$L = \frac{-v_0(t)}{2 * k_i * i_L(t)}(1-D)T \tag{38}$$

The efficiency of the converter during any given switching frequency is given by:

$$\eta = \frac{v_0(t)i_0(t)}{v_i(t)i_i(t)} \tag{39}$$

Assuming $X_C \gg X_L$ the ideal buck transfer function (equation 27) can be used. Combining equations (9), (27), (39) and solving for the inductor current gives the equation below:

$$i_L(t) = \frac{i_0(t)}{\eta} \tag{40}$$

By replacing the inductor current in equation (38) with equation (40):

$$L_c = \frac{1}{2}\left[\frac{v_0(t)(1-D)\eta}{i_0(t)k_i f_{sw}}\right] \tag{41}$$

Since the output voltage is taken across the capacitor and the output current is the current through the capacitor, ohms law states:

$$\frac{1}{\omega_{sys}C} = \frac{v_o(t)}{i_o(t)} \tag{42}$$

Plugging equation (42) into equation (41) the critical inductance for the 4SWBB D-Cap in buck mode is calculated as

$$L_c = \frac{1}{2}\left[\frac{(1-D)\eta}{\omega_{sys}C\,k_i\,f_{sw}}\right] \tag{43}$$

From equation (43) it can be seen that a small duty cycle causes the (1-D) term to approach 1 at which point the inductance would be at its highest value. As the inductor current ripple coefficient has been chosen to be 20% the critical inductance for the 4SWBB D-Cap in buck mode is calculated as:

$$L_c = \frac{1}{2}\left[\frac{1}{2\Pi*60*144\mu F*0.20*20KHz}\right] = 2.3mH$$

2. Boost Mode

The following steps must be taken to calculate the critical inductance during boost mode. Taking Equation (18) and rearranging it such that L is on the right hand side:

$$L = \frac{v_i(t)}{\Delta i_L}DT \tag{44}$$

By inserting Equation (37) into Equation (44):

$$L = \frac{v_i(t)}{2*k_i*i_L(t)}DT \tag{45}$$

Taking similar steps as previously seen in the buck mode case, by combining equations (40) and (42) with equation (45) above, the critical inductance for the 4SWBB D-Cap in buck mode is calculated as:

$$L_c = \frac{1}{2}\left[\frac{D(1-D)^2\eta}{\omega_{sys}C\,k_i\,f_{sw}}\right] \tag{46}$$

Using the same assumptions as in the buck mode case and noting that the worst case scenario for the critical inductance occurs at D=1/3, the critical inductance for the 4SWBB D-Cap in boost mode is calculated as:

$$L_c = \frac{1}{2}\left[\frac{\left(\frac{1}{3}\right)\left(1-\frac{1}{3}\right)^2}{2\pi*60*144\mu F*0.20*20KHz}\right] = 340\mu H$$

The 4 Switch Buck-Boost Dynamic Capacitor uses a single inductor for both modes of operation, therefore the larger of the two inductance values must be chosen to assure CCM at all points of operation. The larger inductance value of 2.3mF results from the buck mode equations. For extra precaution a slightly larger inductance value of 2.5mF is chosen.

F. Input Filter Calculations

Due to the high frequency switching of the 4-Switch Buck-Boost Dynamic Capacitor, it is often the case that high frequency harmonics be present at the input side of the converter. It is undesirable for the input of the 4SWBB D-Cap have these input harmonics as they can affect the power quality of the system that the converter is connected to. To eliminate the high frequency harmonics a second-order LC filter is added at the input side of the 4SWBB D-Cap.

In order for the input filter to not to affect the expected performance of the 4SWBB DCap the filter capacitor must be much smaller than the capacitor of the converter. The size of the filter inductor is not as crucial since it is in series with the converter inductor and can only raise the inductance value further above the critical inductance required to keep CCM. Choosing a capacitor size 100 times smaller than the converter capacitor, the inductor value is calculated below:

$$f_c = \frac{1}{2\pi\sqrt{L_i*C_i}}$$
$$f_c = 2kHz$$
$$C_i \ll C \rightarrow C_i = 1.44\mu F$$
$$L_i = \frac{1}{(2\pi f_c)^2 C_i} = \frac{1}{(2\pi*2kHz)^2(1.44\mu F)} = 4.4mH$$

IV. SIMULATION AND RESULT

To test the true operation of the Four-Switch Dynamic Capacitor a test transmission system is constructed in Simulink. Three possible modes of compensation will be simulated to demonstrate the operation of the 4SWBB D-Cap.
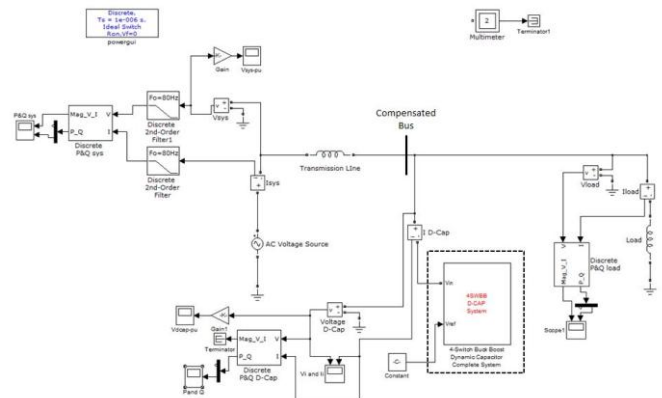

Fig 3.4SWBB D-CAP Simulation Test Setup

A. Compensation in Buck Mode

The first mode of operation of the 4SWBB D-Cap occurs when the device is able to compensate the system while staying in Buck Mode. To ensure that the D-Cap will remain in buck mode, the load is set to draw less reactive power than the rating of the 4SWBB D-Cap. Since the rating of the 4SWBB D-Cap is 240 MVAR the load will be set to draw175 MVAR. In Figure 6, one can see that after an initial transient the load draws a constant value of 175 MVARs.
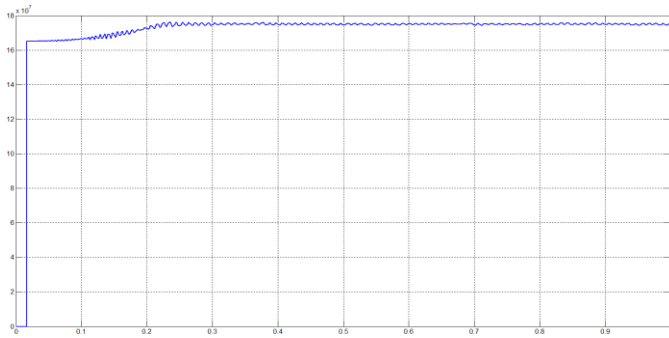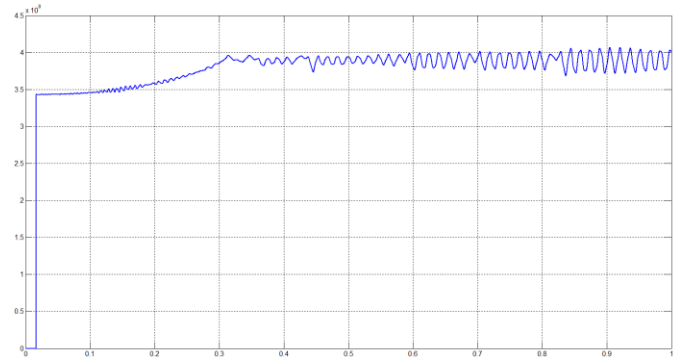
Fig 4.Reactive Power Consumption of the Load

Fig 7.Reactive Power Consumption of the Load

Figure 7 shows how the initial voltage depression at the bus causes a positive error signal to be sent to the D-Cap controller.

In Figure 10 once again one can see that the positive error signal, caused by the reactive demands of the load, force the controller to increase the duty cycles of the 4SWBB D-Cap.
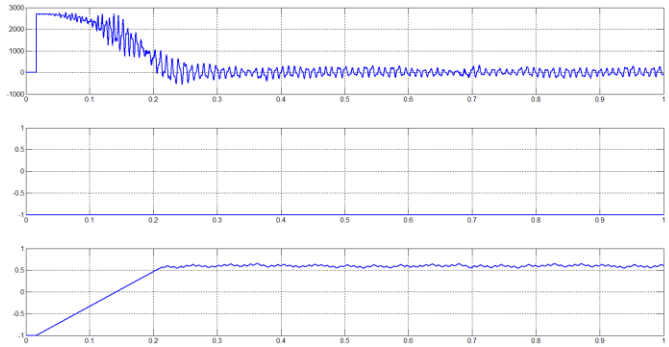

Fig 5.Error input(top),D_{boost}(middle),D_{buck}(bottom)

Figure 8 depicts the reactive power consumption for the Four- Switch Buck-Boost Dynamic Capacitor
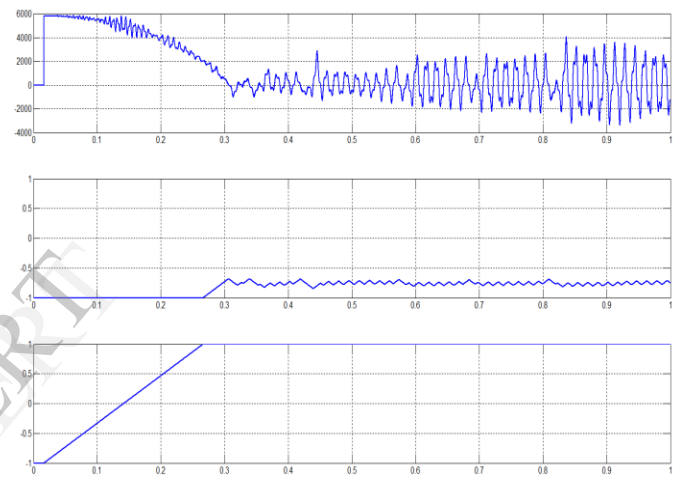
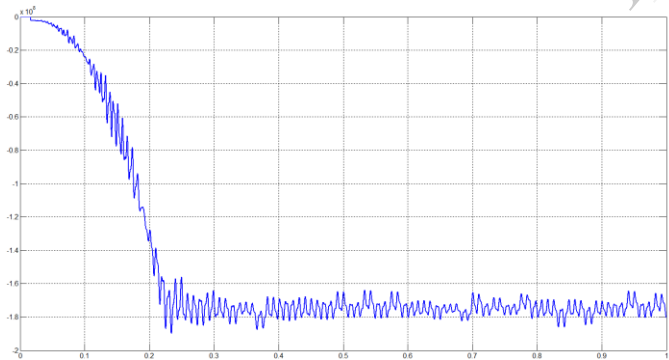Fig 8.Error input(top),D_{boost}(middle),D_{buck}(bottom)

Figure 11 shows how the reactive power output of the 4SWBB D-Cap increases as the duty cycle is increased.
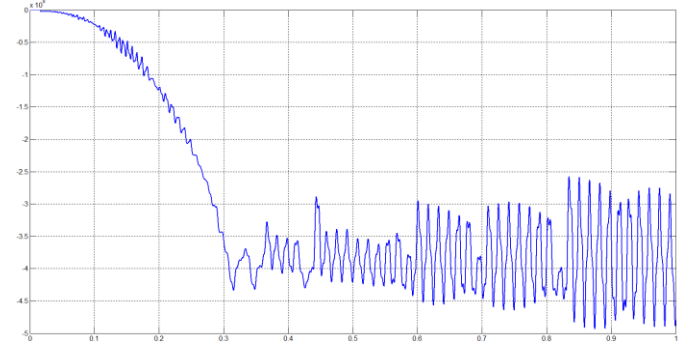

Fig 6.Reactive Power Consumption of 4SWBB D-Cap

B. Compensation in Boost Mode

The second mode of operation of occurs when the device is able to compensate the system but must enter boost mode to do so. Figure 9 shows how after an initial transient the load reactive power remains constant.

Fig 9.Reactive Power Consumption of 4SWBB D-Cap

C. Compensation not possible

The third and final mode of operation occurs when reactive power demands of the load exceed the compensating capabilities of the 4SWBB D-Cap.
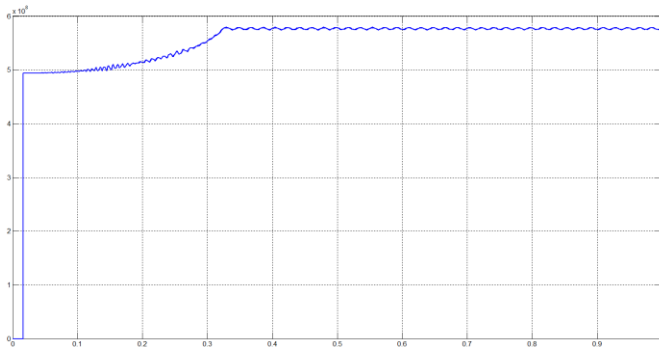
Fig 10.Reactive Power Consumption of the Load

Figure 13 depicts how a positive error signal causes the 4SWBB D-Cap controller to increase the duty cycle starting with buck mode.
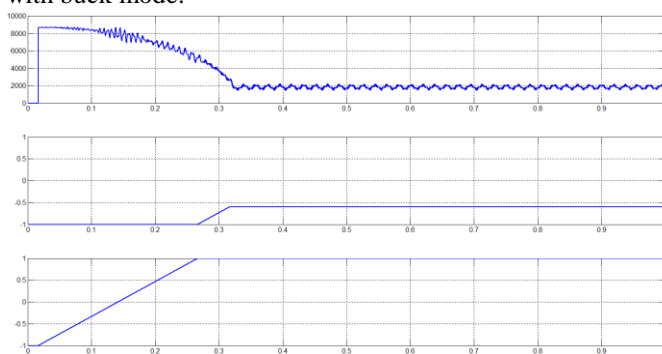

Fig 11.Error input(top),D_{boost}(middle),D_{buck}(bottom)

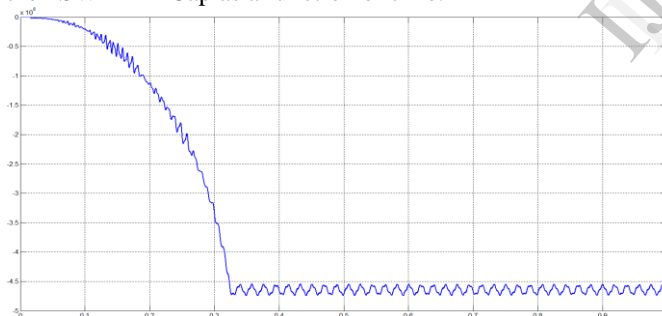Figure 14 demonstrates the Reactive Power Consumption of the 4SWBB D-Cap as a function of time.

Fig 12.Reactive Power Consumption of 4SWBB D-Cap

V. CONCLUSION

In conclusion, this paper demonstrates that the Four-Switch Buck-Boost Dynamic Capacitor works as expected and is indeed a feasible method of providing shunt reactive compensation. From the simulations it was seen that the 4SWBB D-Cap successfully compensates the system by providing the reactive power demand of the load at the bus thus reducing the amount of reactive power supply of the source to approximately zero. This in turn reduces transmission line losses, improves voltage regulation at the compensating bus, and thus will increase overall system stability. This new topology has proven to be an improvement over the existing method of implementing dynamic capacitors by successfully combining the functionality of the buck and boost D-Cap topologies into a single power electronic device. This in turn allows for a smaller design footprint and lower design costs.

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