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Modeling of Electronic Device using CI Technique for Simulation

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***Abstract*: This paper presents modeling of devices, system, sub-system for any kind of field and providing the finding of developed optimization technique for simulation of bench mark circuits. The modeling can be adapted for any of device and system in general way but for this research work electronic devices and circuits under consideration. As day by day circuit complexity increases, proportionally simulation time will also increase. The proposed method is based on computational intelligence with backbone by artificial intelligence. The simulation is based upon mathematical model, and processing element consume the time for each fetch, decode and execute so if object under simulation process is complex it will took more time to process. In this regard the AI and CI modeling helps to process without going into direct mathematical modeling of the object. Obvious pre processing of data, data analysis and training required in the process. For the design and analysis software tools like C, python and MATLAB are used. The comparison of simulation time result table is shown for various circuits. It is found that CI and AI will help in simulation in future years.**

Keywords—Simulation, Modeling, Computational Intelligence, Artificial intelligence, Optimization, Electronic devices.

INTRODUCTION

The circuit simulator is computer program which virtually realize the circuit behavior based on circuit elements mathematical model and there interconnection.
Most popular circuit simulator in earlier days was CANCER and SPICE program written in FORTON. These programs were able to simulate the all required linear and nonlinear circuit elements, poses the three analysis types DC, AC and Transient analysis.
DC analysis gives the dc operating point and it based on equilibrium condition. A matrix will form by applying the KVL and KCL according to elements and there connections, and solve it for the unknown voltage and current.
AC analysis is also called small signal ac analysis, slightly more complicates than dc analysis. AC analysis determines the small-signal solution of the circuit in sinusoidal steady-state. The equations for a linear ac analysis are assembled by the same method that is used for dc analysis except the course, that the circuit equations are complex for ac analysis. Usually, the value that is assigned to a particular source is different for dc analysis than for ac analysis.
The implementation of ac analysis capabilities in a simulation program is similar to the implementation of the dc analysis, the circuit equations in an analysis are of course complex. However, the same formulation and linear solution algorithm that are used for dc analysis may be used for ac analysis. Moreover no new methods are required to implement the small signal analysis.
Transient analysis determines the time-domain response of the circuit over a specific time interval (0,t).The initially time point arbitrarily is defined as time zero. The initial solution either specified by the user or more conveniently is determined by a dc operating point analysis.
Computer simulation of an electronics circuit involves the numerical analysis mathematical model of the circuit. The solution of these equations, for specified special case, simulates the specified electrical characteristics of the circuit.
The number of model parameters for semiconductor devices is gradually increases as technology advances and result in more computation overheads.
The modeling of such complex devices or system can optimize the computation overheads by computational intelligence with backbone of artificial intelligence.

I. PROPOSED WORK

In circuit, all linear and non linear components are connected in well fashion for particular application. In circuit simulation, the process starts with formalization of circuit matrix based on component interconnection and the type of analysis for which it is going to process. After the normalization of matrix, simulator places the component model parameters into the matrix and according to the working region of device it reformulates the matrix and its equations. This process is continuing until the simulation completed. The simulator solve the matrix based on model parameters and device model equations, this is the normal process in simulator. And day by day the model parameters of the device getting increase in number in its model equations for more close approximation. Here the propose research work gives the method in which it first formulate the table between input and output of the device under consideration. This table is use in artificial intelligence to train, test and validate the output. The process of training the network or system is an iterative process and need proper setting of network parameters.

The advantage of doing the modeling for the devices in circuit simulation process is that the result of formulated equations which was initially outcome of direct equation solving process which may took large time due to involvement of the number of model parameters and its model equations variations in particular region of operation

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of that device under its electrical parameters across it. Artificial intelligence completely replaces the direct equation calculation for particular region of operation of the device, so it become fast in natural way than the earlier one.

Again the process of database for table formalization can be optimize using the down sample the values before the training process which farther helps in making fast and light AI model for the device. The AI process is continues and not region based of device which also helps in reduction of cost. The AI process reduces the variables used in the computation process which indirectly save the memory resources as well. The AI also helps in constrain range problem due to predication mechanism.

II. CIRCUIT SIMULATION

Circuit simulation programs have almost completely replaced the traditional breadboard or fabrication and testing of integrated circuits as means of verifying design acceptability. In fact, a breadboard may give results which have small resemblance to the manufactured circuit performances due to the completely different nature of parasitic components. Fabrication and testing of an integrated circuit for verifying a design is very expensive and time consuming. Moreover, extensive probing is not possible and modification of circuit components to determine a better design is practically unfeasible. On the other hand, circuit simulators such as SPICE [18] and ASTAP [19] give very accurate prediction of circuit performances and provide information impossible to obtain from laboratory measurements. As a measure of the use of circuit simulators we offer the following data:

1-At a major IC house SPICE is run about 10000 times per month.

2-At the University of California, Berkeley, SPICE is accessed about 60000 times per year.

3-At IBM East Fishkill facility during December 1977 more than 150 ASTAP jobs per working day were submitted and about 40 hours per working day of CPU of IBM 370/168 were spent for ASTAP runs.

Even though circuits with hundreds of active devices are commonly simulated, circuit simulators are too expensive at present to perform the analysis of a complete VLSI circuit containing more than ten thousand devices (at Bell Laboratories a circuit with 3000 active devices has been analyzed on a CRAY computer in 1/3 of an hour). However circuit simulators still find their application in VLSI circuit design when analog voltage levels are important to verify a design of a part of the entire circuit or when tightly coupled feedback loops need to be taken into account.

Basically the simulation is the process of evaluating the model equations which is based on theoretical concept, which later on lead to sequential program which runs on sequential machine, which took some machine cycles to complete its task, and the time need to complete its task is depend on how much complex task is given? While performing such simulations it consumes computer resources, so more complex equations means more computer resources. Hence it is now the need to reduce the use of resources and increase the speed of operation in simulations[3].

III. SPICE CIRCUIT SIMULATION

In 1972 SPICE circuit simulator was develop by Laurence W. Nagel in Electronics Research Laboratory at University of California, Berkeley. From the development the simulator was so widely used in various universities and in electronics companies. SPICE is a computer program which is used asan electronic circuit simulator. The simulator calculates the quiescent operating point, the time domain response of the circuit, and frequency domain analysis for small circuits. The SPICE program was used by IBM, Honeywell, UNIVAC, RCA and PDP computer systems. The input syntax is a free format style in which it is require to enter data in fixed column format. It need to supply some reasonable circuit parameters and simulation control to get the simulation results.

It also performs a considerable amount of error-checking to ensure that the circuit has been entered correctly. A beginning user needs to specify a minimal number of circuit parameters and simulation controls to obtain reasonable simulation results.

IV. MOSFET MODELING

Circuit simulation using MOSFET device model is done in MATLAB and in SPICE in various circuits. MOSFET is the basic of various devices as well as circuits in IC design so in this work focus is given for the modeling of MOSFET. To model the device it is necessary to understand the characteristics of it.

MOSFET Characteristics

Metal-oxide semiconductor field effect transistors (MOSFETs) normally have high input resistance because of the oxide insulation between the gate and the channel. There are two types of MOSFETs: the enhancement type and the depletion type. In the enhancement type, the channel between the source and drain has to be induced by applying a voltage at the gate. In the depletion-type MOSFET, the structure of the device is such that there exists a channel between the source and drain. Because the enhancement-type MOSFET is widely used, the consideration of MOSFET in this section will be done using the enhancement-type MOSFET.

The voltage needed to create the channel between the source and drain is called the threshold voltage V_T. For an n-channel enhancement MOSFET, V_T is positive and for a p-channel device, it is negative.

Depending on the voltage applied to MOSFETs, it can operate in three modes: cut-off, triode, and saturation regions. The following is a short description of the three regions of operation.

Cut-off Region:

For an n-channel MOSFET, if the gate-source voltage VGS satisfies the condition

$$VGS < VT \quad (10)$$

then the device is cut off. This implies that the drain current is zero for all values of the drain-to-source voltage.

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Triode Region:
When V_{GS}, V_T and V_{DS} is small, the MOSFET will be in the triode region. In this region, the device behaves as nonlinear voltage-controlled resistance. The drain current I_D is related to drain-source voltage V_{DS} by

$$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2](1 + \lambda V_{DS}) \quad (11)$$

provided that

$$V_{DS} \leq V_{GS} — V_T \quad (12)$$

Where

$$K_n = \frac{\mu_n \varepsilon \varepsilon_{OX}}{2t_{OX}} \frac{W}{L} = \frac{\mu_n C_{OX}}{2} \left(\frac{W}{L}\right) \quad (13)$$

and

μn is the surface mobility of electrons
ε is the permittivity of free space (8.85 x 10^{-12} F/cm)
εox is the dielectric constant of SiO2
tox is the oxide thickness
L is the length of the channel
W is the width of the channel
X is the channel width modulation factor Saturation Region:
If V_{GS}> V_T, a MOSFET operate in the saturation region provided

$$V_{DS} \geq V_{GS}\ V_T \quad (14)$$

In the saturation region, the current-voltage characteristics are given as

$$I_D = K_n(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (15)$$

The transconductance is given as:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (16)$$

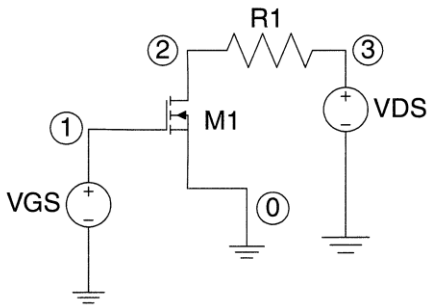


Figure 2- Circuit for obtaining characteristics of MOSFET

and the incremented drain-to-source resistance r_{DS} is given as

$$r_{DS} = \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad (17)$$

The following example obtains the I_D vs. V_{GS} characteristics of a MOSFET shown in figure 4.

MOSFET modeling
MOSFET modeling is done in MATLAB and training is given using ANFIS. To create training data MOSFET model is run in MATLAB and creates data. This data is then used for training of ANFIS.

figure 3 shows the VI characteristics of MOSFET modeling, having different regions of operation depending upon the input VGS
Results shows V-I characteristics of MOSFET with AI in figure 4.

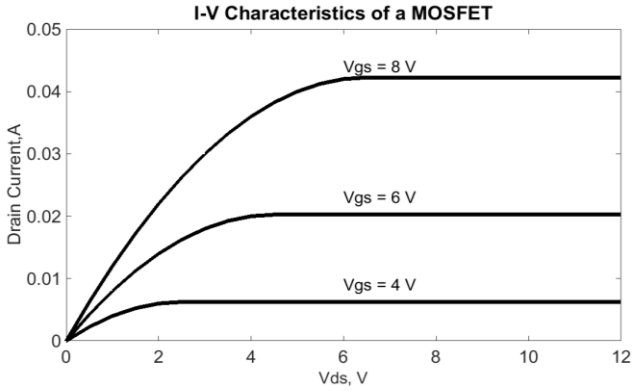


Figure 3- V-I characteristics of MOSFET

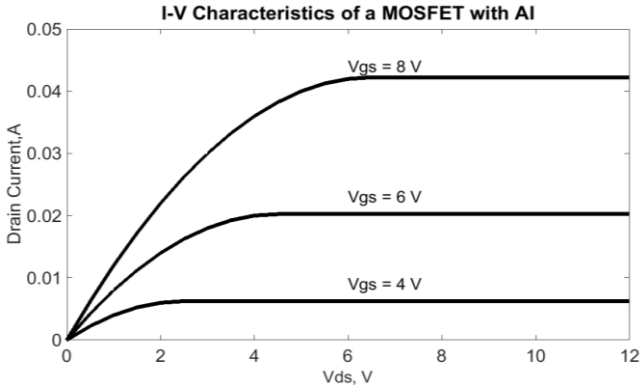
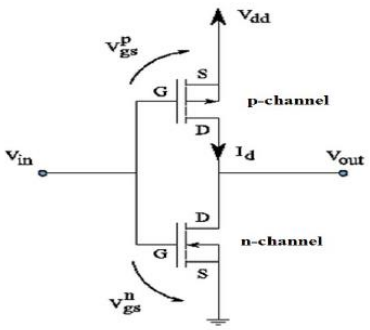


Figure 4- V-I characteristics of MOSFET with ANFIS

To show the benefit of proposed model, we simulate some frequently use circuits in simulator. Comparison of output is done in SPICE for both model.

V. RESULTS AND DISCUSSION

CMOS inverter:-
CMOS inverter is design using two transistor NMOS and PMOS connected in a complimentary push/ pull configuration. Input is given by connecting gates of both MOSFET and output is taken by connecting drains of both as shown in figure 5.



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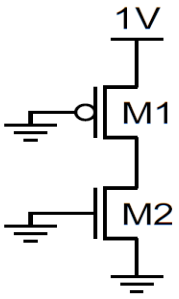

Figure 5 – CMOS inverter

Simulation of CMOS is done using nmos and pmos implemented model in SPICE. Comparison of actual SPICE CMOS model and ANFIS CMOS model shows in the result in figure 6.

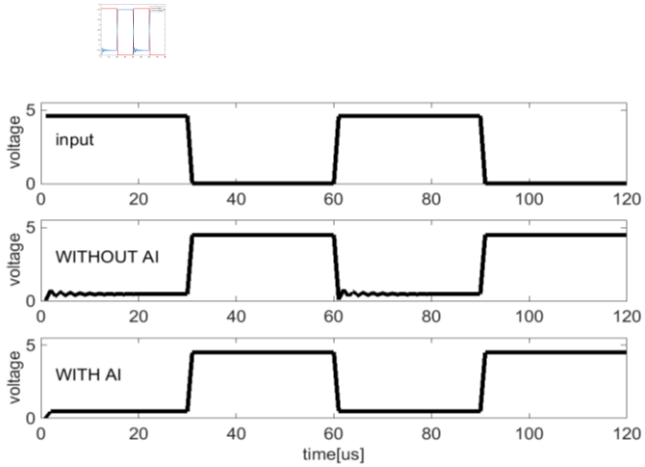

Figure 6 - Output comparison of CMOS Inverter model

Nand Gate:-

Once the basic pseudo nMOS inverter is designed, other logic gates can be derived from it. The procedure is the same as that for CMOS, except that it is applied only to nMOS transistors. NAND gates can be implemented using CMOS logic shown if figure 7. It has two inputs and one output. Its code and waveforms given below in figure 8.

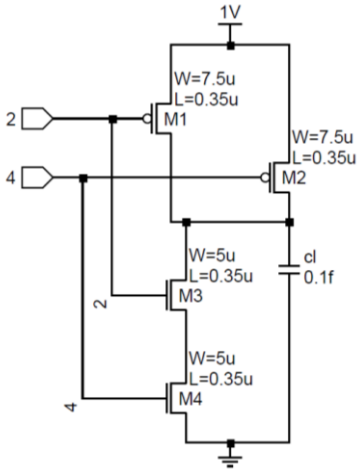

Figure 7: NandGate using CMOS model

```
.model n1 nmos
.model p1 pmos
vdd    3        0        1v
*vss    0        0        0v

M1 3 2 1 3 p1  w=7.5u l=0.35u pd =13.5u ad=22.5p ps=13.5u as=22.5p
M2 3 4 1 3 p1  w=7.5u l=0.35u pd =13.5u ad=22.5p ps=13.5u as=22.5p
M3 1 2 5 0 n1  w=5u   l=0.35u  pd=9u   ad=9p    ps=9u    as=9p
M4 5 4 0 0 n1  w=5u   l=0.35u  pd=9u   ad=9p    ps=9u    as=9p

VA 2 0 pulse(1 0 0 0 0 20ns 40ns)
VB 4 0 pulse(1 0 0 0 0 40ns 80ns)
*cl 1          0              0.1f
*.option acct
*.tran 10ps 80ns
*.print tranv(2)  v(4) v(1)
.control
tran 1ps 80ns
pre_setstrict_errorhandling
unset ngdebug
run
display

*set xbrushwidth=1.9

plot v(2)+10 v(4)+8 v(1)+6

wrdatanandgate1_nodeval.txt  v(2)  v(4) v(1)

acct rusags all > nandgate1_rusags.txt
mrdump nandgate1_rhs_matrix.txt
mdump  nandgate1_lhs_matrix.txt
write andgate1_rdata.raw all
.endc
.end
```

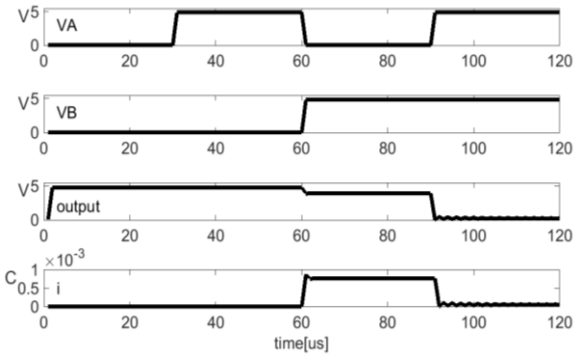

Figure 8: Nand Gate output without CI

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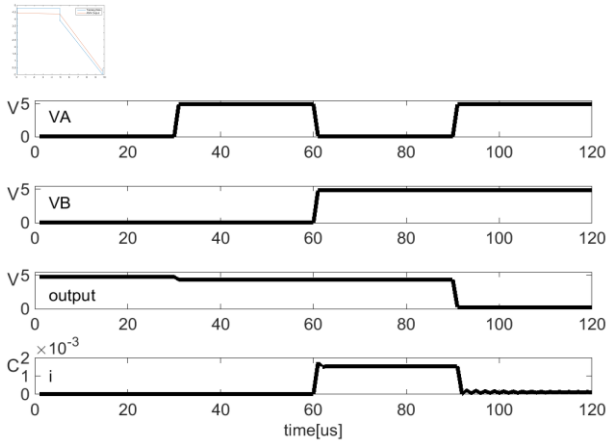

Figure 9: Nand Gate output with ANN

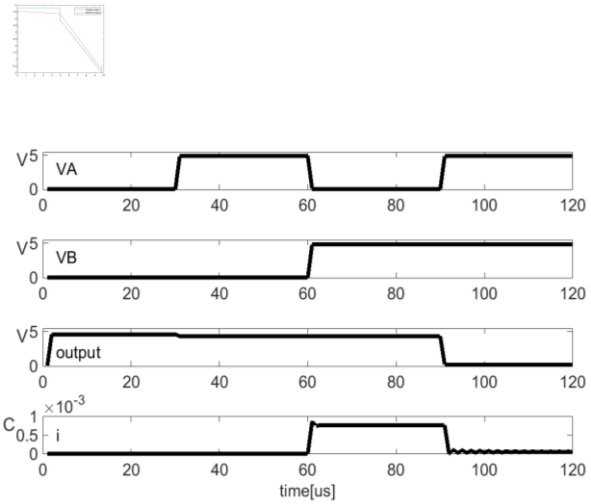

Figure 10: Nand Gate output with ANFIS

Nandgate & NOR gate rusage: result of simulation

Ruses parameters	NAND GATE	NOR GATE
Total elapsed time:	5.039 sec	0.634 sec
Total DRAM available	2012.36MB.	2012.36MB
DRAM currently available	1316.0MB.	1332.19MB
Total ngspice program size	14.53MB.	7.39MB
Number of lines in the deck	18	18
Netlist loading time	0	0
Netlist parsing time	-2.24E-19	7.75E-01
Nominal temperature	27	27
Operating temperature	27	27
Total iterations	220149	16147
Transient iterations	220137	16140
Circuit Equations	9	9
Circuit original non-zeroes	27	29
Circuit fill-in non-zeroes	0	0
Circuit total non-zeroes	27	29
Transient timepoints	80035	80035
Accepted timepoints	80035	80035
Rejected timepoints	0	0
Total analysis time	1.918	0.203
Matrix load time	0.705	0.048
Matrix synchronize time	0	0
Matrix reorder time	-2.60E-17	1.76E-01
Matrix factor time	0.047	-8.53E-01
Matrix solve time	0.048	-8.53E-01
Transient analysis time	1.872	0.171
Transient load time	0.705	0.046
Transient sync time	0	0
Transient factor time	0.047	-8.53E-01
Transient solve time	0.048	-8.53E-01
Transient trunc time	0.156	0.013
Transient iters per point	0	0sS

Other circuits also were implemented using the same model and their performances were comparing and it is given in table. It shows the number of transistors in the circuit, total elapse time required for circuit simulation.

Table 1- Elapse Time Comparison of output of various electronic circuits

Name of circuit	**No. of transistor**	**Total elapse Time without CI**	**Total elapse Time with CI**	**MSE**
Ai_inv	02	3.370	2.290	0.0062
Nand Gate	04	5.039	3.475	0.0043
Norgate	04	0.624	0.425	0.0048
OR gate	06	5.008	3.255	0.0092
AND-OR inverter	06	0.234	0.172	0.0122

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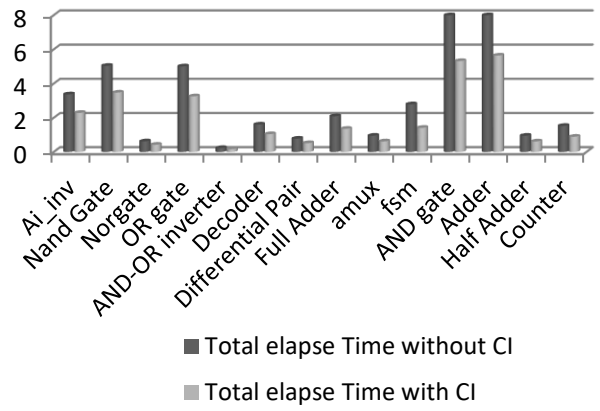
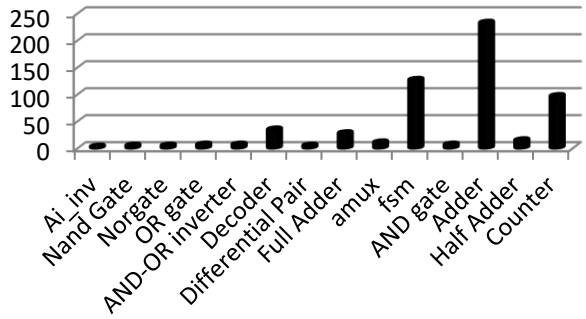
Decoder	34	1.607	1.044	0.0052
Differential Pair	04	0.780	0.517	0.0034
Full Adder	27	2.090	1.358	0.0078
amux	10	0.954	0.620	0.0062
fsm	126	2.792	1.414	0.0088
AND gate	06	8.187	5.321	0.0076
Adder	232	9.141	5.641	0.0098
Half Adder	14	0.952	0.618	0.0056
Counter	96	1.529	0.893	0.0067

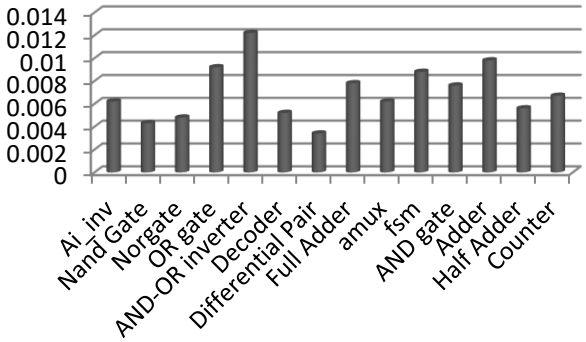
The table 1 gives the comparison of time required for simulation in NGSPICE using previous model and new design CI model. Above results show that time required for simulation of circuits using CI model is less as compared to previous models. It also shows error between both outputs which is very less.



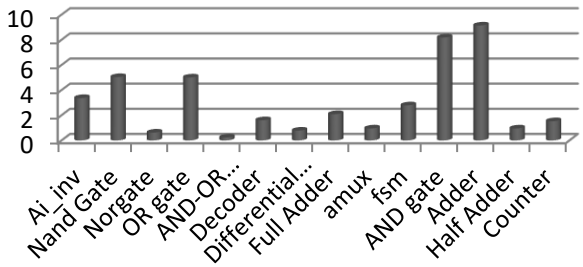
No. of transistor



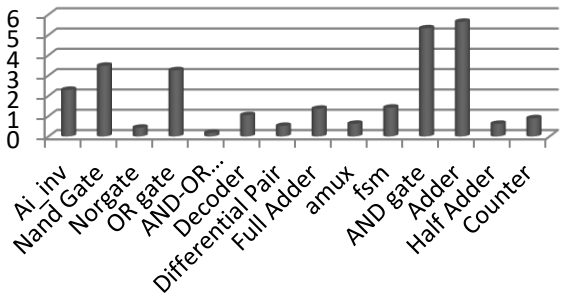
MSE



Total elapse Time without CI



Total elapse Time with CI



VI. CONCLUSION

The focus of work in this paper is on modeling and optimization of simulation by using various parameters of computational intelligence(ANFIS). From study of various works mention in this paper, it is observed that devices can be modeled in various method which gives better simulation in terms of time complexity. This work will give new dimension to the optimization and simulation techniques in any field like electrical, mechanical, civil areas. In this paper emphasis is given on modeling of MOSFET device using ANFIS and SPICE is done, and it is compared in SPICE with neural network. With this study it can be conclude that ANFIS gives excellent simulation results which can be implement in AISPICE simulation. Thus it can be used in various simulators.

In today's world of optimization, it is necessary to work on reducing the overload of circuit simulation. This works shows that the MOSFET model design using computational intelligence (ANFIS) gives same result as with SPICE model but reduces the circuit simulation time. The model which is developed in this work is simple to design, more accurate and also faster. The designed CI model is used in NGSPICE and it is compared with previous simulation model, this comparisons shows that the results of both are nearly same with least error and same accuracy. This result shows that with CI model the simulation time of all circuits were reduced by 40-45% than the regular model. So we can conclude that the CI techniques can be used in simulation for improving the time complexity and optimization of simulators.

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