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Modeling and Implementation of Modular Multi-Level Converter based HVDC System for **Grid Connection**

Punam B. Sao

PG Scholar, Department of Electrical Engineering Shri Sai Collage of Engineering and Technology Bhadrawati, Maharashtra, India.

Abstract— This paper explores the application of modular multi-level converters (MMC) as a means for harnessing the power from off-shore wind power plants. The MMC consists of a large number of simple voltage sourced converter (VSC) sub modules that can be easily assembled into a converter for highvoltage and high power. The work shows that the MMC converter has a fast response and low harmonic content in comparison with a two-level VSC option. This paper gives the modeling approach used, including a solution to the modeling challenge imposed by the very large number of switching devices in the MMC.

The two-level converter valve together with series-connected press-pack insulated-gate bipolar transistors (IGBTs) is a reliable and proven technology for transmission-scale converters. This has been put to use in a further development of high-voltage dc (HVDC) transmission employing voltage-source converters (VSCs). A cascaded two-level (CTL) converter consisting of several smaller two-level building blocks, also called cells, enables the creation of a nearly sinusoidal output voltage from the converter. The development of the CTL is the subject for this paper. Using technology modules developed and refined during the last 15 years, it has been possible to create a converter that addresses and solves many of the limitations of VSC-HVDC transmission while retaining all operational functionality.

Keywords— Modular Multilevel Converter (MMC), HVDC transmission, Voltage Source Converter (VSC), Converter Control, Mathematical modelling.

INTRODUCTION

The MMC is selected as the topology for this work in HVdc applications. The MMC topology is shown in figure 2.4, with the green dashed line showing one of the arms of the MMC and the blue dashed line showing one of the legs of the MMC. When compared to the HVdc-VSC topologies, the MMC has the following advantages [10]:

- Less expensive and faster fabrication process due to modular design.
- It is easy to scale up to high voltages without adding extra complexity.
- The rise time of dc-side fault currents is limited by the arm inductors.

There have been three proposed topologies for the SM of a MMC. These topologies are: half-bridge sub-module (HBSM), full-bridge sub-module (FBSM) and clamp-double sub-module (CDSM) [16]. The major limitation of the HBSM is that it is unable to block dc-side faults, but this can be overcome by the use of a dc-breaker like the one proposed in 0. The mayor advantages of the HBSM are the lower component count, when

U. G. Bonde

Professor, Department of Electrical Engineering Shri Sai Collage of Engineering and Technology Bhadrawati, Maharashtra, India.

compared to the other SM topologies, and higher efficiency. For the reasons mentioned before, the HBSM is selected as the SM topology for the MMC. The HBSM has four possible current paths, as shown in figure 2.

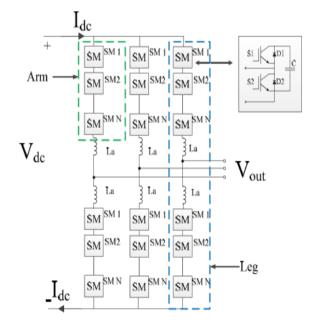


Fig. 1. Modular multilevel converter.

The blue lines indicate current flowing into the SM and the red lines indicate current flowing out of the SM. Currents flowing into the SM charge the capacitor and currents flowing out discharge the capacitor.

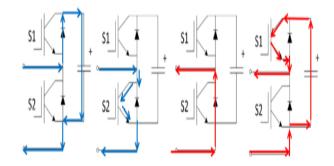


Fig. 2. Modular multilevel converter.

Operation principles

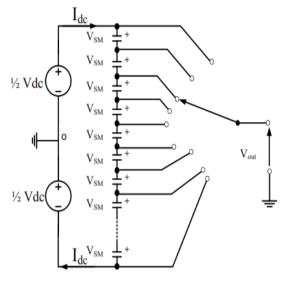


Fig. 3. MMC Representation.

The MMC operates by inserting or bypassing the SM capacitor to form, in staircase shape, the output voltage waveform [17]. The capacitor is inserted when S1 is on, and bypassed when S2 is turned on. When both switches in the SM (i.e., S1 and S2) are off, the current flows through the freewheeling diodes. The operation of the MMC is illustrated in figure 3, using dc sources instead of capacitors and a selector. The selector inserts or bypasses dc sources according to the control algorithm of the MMC. The inserted dc sources produce a voltage output with a staircase form, as shown in figure 4. The six levels voltage waveform in figure 4 is produced with five SMs per arm of the MMC.

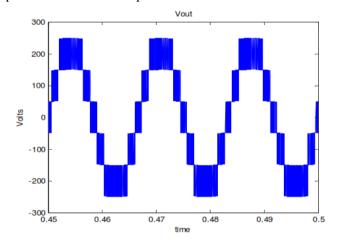


Fig. 4. Output Voltage of the MMC.

B. Passive components of the MMC

This section explains the process of selecting the values for the passive components, namely, the SM capacitor and the arm inductor, whose main functions are energy storage and limiting the circulating current, respectively. The selection of the SM capacitance and inductance values for the MMC has been discussed in [18]-[20], and this section is an explanation of what is presented in the literature.

Assuming that the MMC has an infinite amount of SM and neglecting inductor La, the arms of the MMC can be replaced by ideal ac voltage sources as shown in Fig. 5, and the dc link

can be considered as an ideal dc source. By applying Kirchhoff's current law to figure 5, the arm current for one phase can be defined as [20]:

$$i_{a1} = \frac{1}{3}I_{dc} + \frac{1}{2}i_a(t) = \frac{1}{3}I_{dc} + \frac{1}{2}\hat{i_a}\sin(\omega_0 t + \varphi)$$
 (1)

Where ω_0 is the fundamental frequency of the system in radians per second, φ is the phase shift between the voltage and the current, and (i a) is the peak phase current.

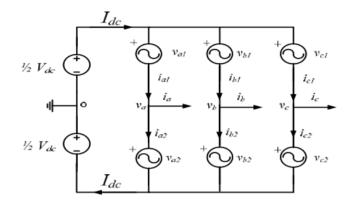


Fig. 5. Ideal model of MMC.

By applying Kirchhoff's voltage law to figure.5, the arm voltage source can be defined as:

$$v_{a1}(t) = \frac{1}{2}V_{dc} - v_a(t) = \frac{1}{2}V_{dc} - \widehat{v_a}\sin(\omega_0 t)$$
 (2)

For simplicity, (2.3) and (2.4) the relation between ac and dc variables as are defined as [16]:

$$m = \frac{3}{2} \frac{\widehat{\iota_a}}{I_{dc}} \tag{3}$$

$$k = 2 \frac{\widehat{v_a}}{v_{dc}} \tag{4}$$

Introducing (3) and (4) into (1) and (2), respectively, gives:

$$i_{a1}(t) = \frac{1}{3}I_{dc}[1 + m\sin(\omega_0 t + \varphi)]$$
 (5)

$$v_{a1}(t) = \frac{1}{2} V_{dc} [1 - k \sin(\omega_0 t)]$$
 (6)

In order to calculate the power in the arm of the MMC, (5) and (6) are multiplied, yielding:

$$p_{a1}(t) = \frac{P_{dc}}{6} [1 + m \sin(\omega_0 t + \varphi)] [1 - k \sin(\omega_0 t)]$$
 (7)

Where, Pdc is defined by (8)

$$P_{dc} = V_{dc} I_{dc} \tag{8}$$

Integrating (7) over half a period yields the total energy change ΔW in the arm of the MMC as follows:

$$\Delta w = \frac{{}^{2} P_{dc}}{3 k \omega_0 \cos \varphi} \left[1 - \left(\frac{k \cos \varphi}{2} \right)^2 \right]^{3/2}$$
 (9)

In order to obtain the energy change of the MMC SM, (9) is divided by the number of SMs per arm (N), yielding:

$$\Delta W_{SM} = \frac{2 P_{dc}}{3 k \omega_0 N \cos \varphi} \left[1 - \left(\frac{k \cos \varphi}{2} \right)^2 \right]^{3/2}$$
 (10)

The energy stored in a capacitor is defined as:

$$w = \frac{1}{2}cv^2 \tag{11}$$

By combining (10) and (11), the SM capacitance can be calculated as:

$$C_{SM} = \frac{\Delta W_{SM}}{2 \in V_{SM}^2} \tag{12}$$

Where, ∈ is the capacitor voltage ripple factor in percentage and VSM is the SM voltage. The capacitors of the SM are charging and discharging during the normal operation of the MMC. This will create a voltage difference across the arm inductances that can be defined by [18]:

$$v_{dif} = V_{dc} - (v_{a1} + v_{a2}) = 2 R_a i_{Z_a} + 2 L_a \frac{d}{dt} i_{Z_a}$$
 (13)

$$i_{Z_a} = \frac{i_{a1} + i_{a2}}{2} \tag{14}$$

Where, iz_a represents the circulating current between phases and Ra the arm resistance of the MMC. Neglecting the arm resistance, the voltage difference (13) can be approximated by:

$$v_{dif} = 2L_a \frac{d}{dt} i_{Z_a} \tag{15}$$

Then (15) can be used to determine the value of the arm inductance. If the inductance arm inductance is too low, the circulating current can become difficult to control; if selected too great v_dif becomes too large and makes the voltages of the leg difficult to balance [15]. Using (14) and simulations, to fine tune the results, it was found that a value of 2% was a good compromise between the two tradeoffs.

II. CONTROLLERS FOR A TWO-TERMINAL MMC-BASED HVDC TRANSMISSION SYSTEM

The control of two terminal MMC-based HVdc system encompasses several controllers regulating the SM capacitor

voltage, minimizing the circulating currents and transferring the desired active and reactive powers. This session analyzes the active and reactive power outer controllers, the dc-voltage outer controller, the current controller, and the SM capacitor voltage controllers and circulating current controller. The gains for the controllers are selected using simplified models, and Bode plots and step responses are used to evaluate the current and dc voltage controllers.

Session I provided the background to understand the MMC topology and the PS-SPWM algorithm controlling the switching devices. This session focuses on the controllers depicted in figure 6 for a two-terminal MMC-based HVdc transmission system. It is customary to control a two-terminal HVdc link by having the sending-end Terminal 1 controlling the dc-link voltage and reactive power, and the receiving-end Terminal 2 controlling the active and reactive powers injected into the receiving grid [31]. The associated controllers are indicated in figure 6 as "dc Voltage controller", "Power controller" and "Current controller" for Terminal 1 and "Power controller" and "Current controller" for Terminal 2. In addition, two other control functions are important; namely, maintaining the SM capacitor voltages at their reference values, and controlling the circulating current to avoid system instabilities [32]. These two functions are accomplished by the "SM Capacitor voltage controller" block on each terminal. The "dc Voltage controller" and "Power controller" form the socalled outer controllers. The "Current controller" is the inner controller.

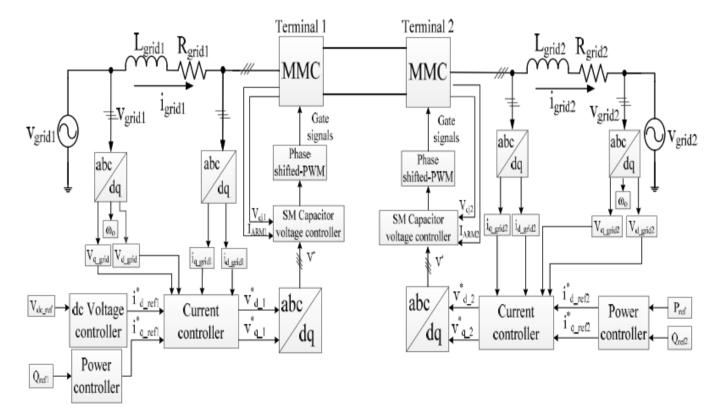


Fig. 6. Typical control scheme of a two terminal HVdc-link.

The "abc/dq" block makes use of the Park's Transformation [33] to transform from the abc stationary reference frame to a synchronously-rotating frame and its detailed Matlab/Simulink representation is given in Appendix A.1. The controllers are analyzed and their respective gains selected using the system [34].

III. SIMULATION RESULT

This simulink model shows a Sim Power Systems (SPS) model of a High Voltage Direct Current (HVDC) interconnection using Voltage-Sourced Converters (VSC) based on the Modular Multi-level Converter (MMC) technology. The SPS simulation is optimized by the use of an aggregate MMC model as shown in figure 7.

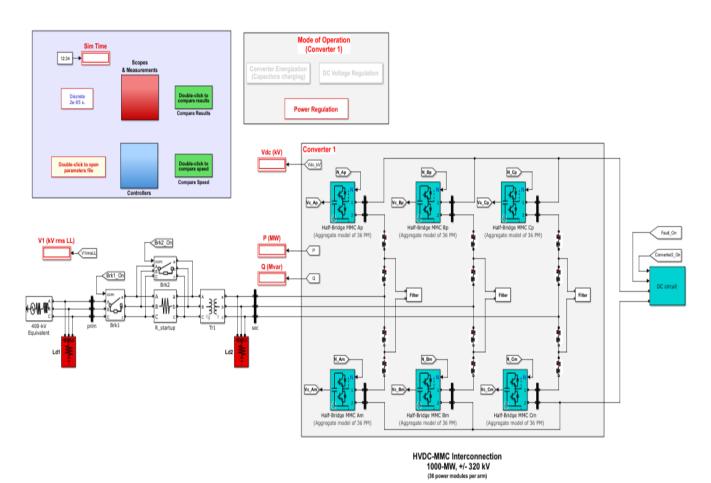


Fig. 7. Typical simulink model of MMC based Hvdc system.

Simulating SPS model for 10 seconds allows observation of the operation of the interconnection during start-up (capacitor charging), voltage regulation, and power regulation. All parameters required to run the model can be found in the following file: HVDC_MMC_param.m.

This file is automatically executed in the MATLAB workspace when the example is open. Run the model and observe the following events:

- At 0.1s, Breaker 1 is closed and Converter 1 is energized through a resistor to reduce the charging current. Capacitors are being charged and at 1s, the start-up resistor is short circuited by closing Breaker 2.
- At 1.5s, Converter 1 is deblocked and the Voltage Regulator is enabled.

- At 2s, the Voltage Regulator set point is ramped to the nominal DC operating voltage of the interconnection: 640 kV (+/-320 kV).
- At 4s, PQ regulators are enabled and Converters 2 switches are closed.
- At 4.2s, the Active Power Regulator setpoint is ramped to 1pu (1000 MW).
- \bullet At 7.5s, the Reactive Power Regulator setpoint is ramped to 0.25pu (250 Mvar).

If one set the value of parameter 'Tfault' to 7 (actual default value=9999) in the workspace and re-start the simulation, a DC fault will be applied at the middle of the cable at 7s. The half-bridge MMC will be blocked and the interconnection will be shut down after two cycles (Brk1 will be opened).

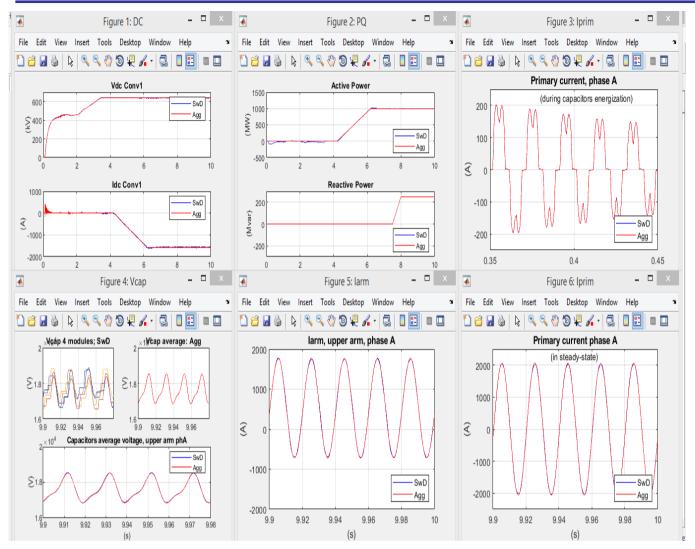


Fig. 8. Simulation result of MMC HVdc system.

IV. CONCLUSION

The main objective of this paper was to analyze the current technologies used for transmitting power, focusing on HVdc systems. The enabling objectives were to build a simulation model of an HVdc system between to power grids, to implement a sensorless controller for grid synchronization of an MMC-based HVdc terminal, and to analyze the impact of a high-voltage, fast-switching IGBT's on an MMC-based terminal. This paper has accomplished the following:

- A theoretical background was given of HVdc technologies, focusing on MMCs. From this background it was concluded that the MMC has several advantages over other HVdc-VSC topologies so it is a viable alternative for HVdc-VSC links, especially when trying to connect to weak ac grids.
- A first order transfer function to model the MMC plant was presented. Once a PI controller is added to control the plant, it becomes a second order transfer function that facilitates the design the current controller of the MMC. The process was shown and validated with simulations. The calculation of the various gains for the inner current of the

MMC followed a similar process to the one followed for a two-level inverter. This facilitates the process of building a simulation model for individuals already familiar with a three-phase two-level inverter control. A prefilter was added to reference command of the controller to ensure the selected bandwidth was achieved. Without a prefilter, the system bandwidth is more than twice the selected design target.

- The outer controllers of an HVdc link, power control and dc-voltage control, were explained and a method was presented to calculate the various gains for the controllers. The tuning of the outer controllers must be done with care to ensure that the correct bandwidth of the controller is selected in order to avoid instability issues of the system. A bandwidth of 40 Hz for the outer controller proved to be suitable for the Matlab/Simulink simulations.
- A working model of an MMC-based two-terminal HVdc link was presented and the design steps of the model were given. The model was built using the theoretical background given in the thesis and it can be expanded and improved for different simulation purposes.

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