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Modeling and Comparing of Dual Rail Delay Insensitive Circuit Architecture

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***Abstract*: Power dissipation is one of the important factors while considering the performance. The other factors are delay, slew rate, rise time and fall time. In this paper, we intend a dual rail asynchronous design approach which yields to low power consumption. With shrinking technology demoting power consumption and over all power management on chip are the chief challenges in semiconductor devices due to the elevated complexity. Low power devices are designed due to increase in demand of portable devices. For many designs, optimization of power is important as timing due to the necessitate to extended battery life. CMOS is used in VLSI design which boosts sub threshold leakage current and gains static power dissipation. This paper also enumerates low power using Multi Threshold Null Convention Logic (MTNCL), Sleep Convention Logic (SCL) and Multi Threshold Dual spacer Dual rail Delay Insensitive Logic (MTD³L). Due to high threshold voltage transistors in these designs reduces the power consumption. All these designs techniques are explained and the performance is compared using multiplexer. The evaluated results are tabulated & waveforms are collected.**

Keywords - Complementary Metal Oxide Semiconductor (CMOS), MTNCL, MTD³L, Power Dissipation, Gate Delay.

I. INTRODUCTION

Portable and handheld devices insist high-speed computation and intricate functionality with low power consumption. For these applications, low power dissipation is an incredibly significant design constraint to be considered[1]. The power is starting to frontier the speed of Integrated Circuits(IC's). As technology reduces, power dissipation and delay becomes a vital parameter. Like mobile phone, laptops, all electronics gadgets are designed to have minimum power consumption and delay [2]. Power consumption plays a significant task in the present day VLSI technology [1, 2]. Power and performance are always trade off to congregate the system necessities. Power shows a direct impact on the system cost. If a semi conductor device is consuming more power, then a superior cooling mechanism would be essential to maintain the circuit in normal conditions. If not, its performance is corrupted and on incessant use it may be eternally damaged [2].

In accessible CMOS technologies sub threshold leakage current is superior to other leakage components [3]. As technology scales down to nanometer, sub threshold leakage power increases exponentially with the diminution of supply voltage. To decipher this snag, diverse techniques have been urbanized at different levels of abstraction [4]. In sub threshold circuits, the supply voltage is abridged well below the threshold voltage of a transistor. Sub threshold CMOS logic operates with the power supply V_{dd} less than the transistors' threshold voltage Vt[5]. This is done to ensure that all the transistors are indeed operating in the sub threshold region. In CMOS technology, Power dissipation can be alienated into two sorts: Static and Dynamic.

1.1 Static power dissipation: Static power dissipation is occurred due to the leakage currents [4]. Sub threshold leakage, Reverse bias leakage are diverse leakage components that form static power. Static power can be expressed as,

$$p_{static} = V_{DD}\, I_{leakage} \qquad (1)$$

Where P_{static} is static power, V_{DD} is supply voltage & $I_{Leakage}$ is leakage current.

1.2 Dynamic power dissipation: The dynamic power consumption is mainly due to the switching of transistors. Dynamic power dissipation is from current flow during logic transitions [3]. Dynamic power can be expressed as,

$$P_{avg} = \propto C_L\, V_{DD}^2\, f \qquad (2)$$

Where α is the switching activity, C_L is load capacitance, V_{dd} is supply voltage, and f is the frequency.

Most of the integrated circuits schemed and fabricated today are synchronous in nature. In synchronous circuits, all components partake a common time, defined by a clock signal distributed throughout the circuit [4, 5]. In high-speed circuits, as the clock frequency addendums, power consumption also increases gradually. An efficacious method for degrade power consumption is reducing the dependency on the clock in the circuit. To procure this, the digital system should be disunited into smaller autonomous blocks [6]. These blocks should not share a common time defined by a clock signal. This leads to the asynchronous design style. Asynchronous circuits are fundamentally different from the synchronous counterpart and use handshaking among components to perform the necessary synchronization, communication and sequencing of

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operations [5]. The use of confined handshakes for flow control instead of a global clock is the common principle underlying all asynchronous approaches. In disparity to synchronous circuits where the clock signal is applied in a untainted "feed forward" demeanor, these handshakes ascertain a closed-loop scheme between every source pair, which tends to formulate the operation more robust[6]. The lack of a global clock eliminates the clock distribution crisis. The dynamic power dissipation of asynchronous circuits is negligible, since devoid of stimulation by events at the input they do not execute any operation. Asynchronous circuits are categorized into two models: Bounded-delay and Delay insensitivity [1, 2]. In bounded delay, delays are bounded in both gates and wires. To avoid the perilous stipulation the delays are added [3]. This leads to wide timing analysis for the correct circuit operation. In Delay Insensitive model, delays are unbounded in logic gates, interconnects, and in wires. Compared to bounded delay and clocked approach, Delay insensitivity yields the timing analysis and provides average correct circuit operation. Delay Insensitive (DI) circuits assembled as: Quasi Delay Insensitive (QDI) circuits, Speed Independent (SI) circuits & Self Timed (ST) circuits.

The existing techniques CMOS, MTNCL, MTD^{3}L, SCL are effective techniques to reduce power consumption. In this paper we are comparing all these methods in terms of power, delay, slew rate, rise time & fall time. All these techniques are demonstrated by the assistance of multiplexer.

The paper organized as follows: Section II provides overview of dual rail delay insensitive approaches. Section III provides comparison between CMOS, MTNCL, MTD^{3}L, SCL implementations. Finally Section IV concludes the paper.

II. DUAL RAIL APPROACHES

Power consumption is a significant property of a design that affects feasibility cost and reliability. It persuades a larger number of critical design decisions, such as power supply capacity, battery life time, packaging requirements [7]. To reduce those drawbacks, some techniques have been suggested like CMOS, MTNCL, MTD^{3}L, and SCL.

2.1 Complementary Metal Oxide Semiconductor (CMOS):

Today's leakage power reduction is a tectonic chore to amend the performance of CMOS circuit with the power loss scenario. CMOS logic is the union of PMOS pull up network and NMOS pull down network [8]. The static logic is the widely accustomed logic style in CMOS technique. The structure of the CMOS technology is shown in figure 1(a). The sovereign vantages of static CMOS logic are low power consumption, robustness and passable performance with no static power dissipation [8, 9]. In this technology MOS transistors are accustomed in complementary pairs. In which the inputs of the two transistors (PMOS & NMOS) are tie jointly. The PMOS transistors will set the output to 1 whenever the implemented Boolean logic function defines it & NMOS transistors has the duty of setting output to 0 whenever the implemented function defines it[9]. Both the networks cannot be active at the coequal time and cannot be off at the identical time. The main benefit of CMOS logic circuits is that they have high noise margin, hence they are more scalable.

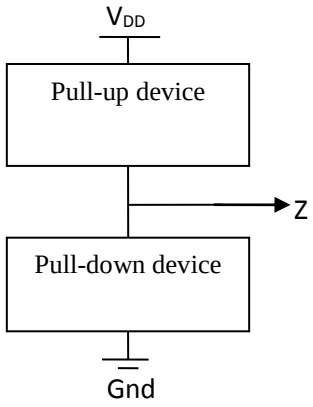

Figure 1(a): Schematic of CMOS logic

The fig1 (b) shows the implementation of NAND gate using CMOS logic. In which, transistors Q1 and Q3 are resemble the series joined complementary pair from the inverter circuit. Both the transistors are controlled by same input pin A. Similarly, Q2 and Q4 are controlled by input pin B. When the input is high, PMOS transistors are turning off & NMOS transistors are on.

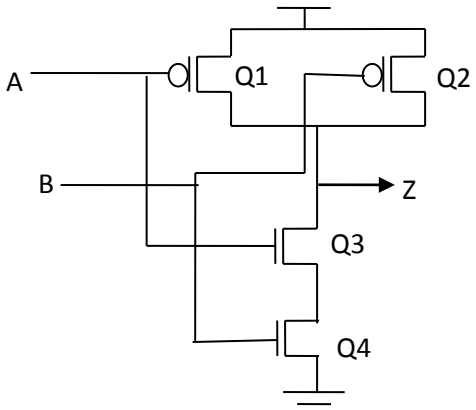

Figure 1(b): Implementation of NAND gate

The main drawback of CMOS technique is that uses more number of transistors which increases the area and delay of the circuits.

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2.2 Multi Threshold Null Convention Logic (MTNCL): MTNCL combines the Multi-Threshold CMOS (MTCMOS) power-gating structure with the NCL architecture, in providing momentous improvements in leakage power reduction, delay, and area [10]. In this method, the reset circuit is not essential for further since all the gate output will now be enforced to NULL by the MTCMOS sleep mechanism, instead of all inputs becoming logic 0 as shown in fig 2(a) [11]. Due to the confiscation of hysteresis, MTNCL threshold gates essentially use fewer transistors than that of original NCL. This is consummate by the amputation of the reset and hold1 blocks in the original NCL threshold gate design, as only requiring two extra transistors for sleep functionality, as shown in fig (2b).

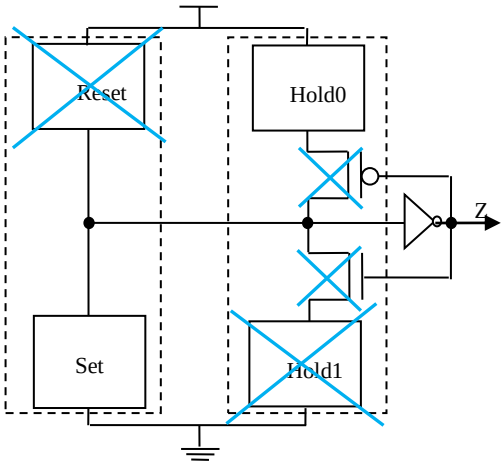

Figure 2(a): Integrating MTCMOS into NCL threshold gates.

The $hold_1$ circuitry and subsequent NMOS transistors are detached, and the reset circuitry consists of a PMOS transistor is detached to sustain the complementary nature of CMOS logic (such that the gate will never float.

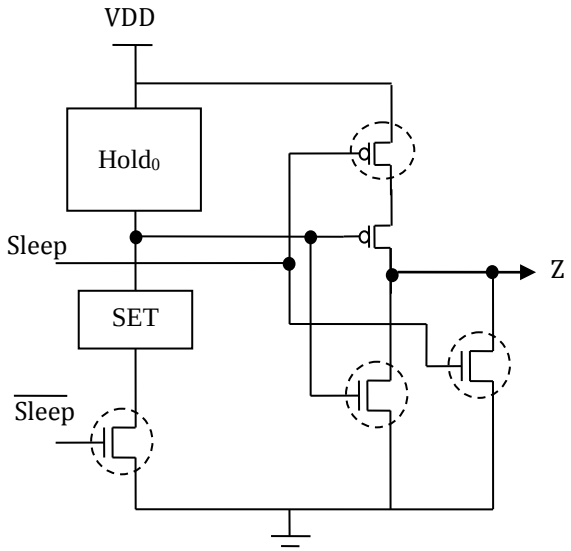

Figure 2(b): Structure of MTNCL

This structure eliminates the output, which mounts glitch by moving the power gating high threshold voltage transistor to pull down network (PDN) and removing the two bypass transistors. When the gate is in sleep mode, except the output inverter, all the PMOS transistors are turned ON and the inputs become logic 0 and remnants ON when the gate exits from sleep mode i.e., the gate's set condition becomes true[12]. In both cases, the gate output is already logic0; so the speed of these p-MOS transistors does not affect performance of the circuits, therefore high V_t transistors are used to shrink the leakage power dissipation.

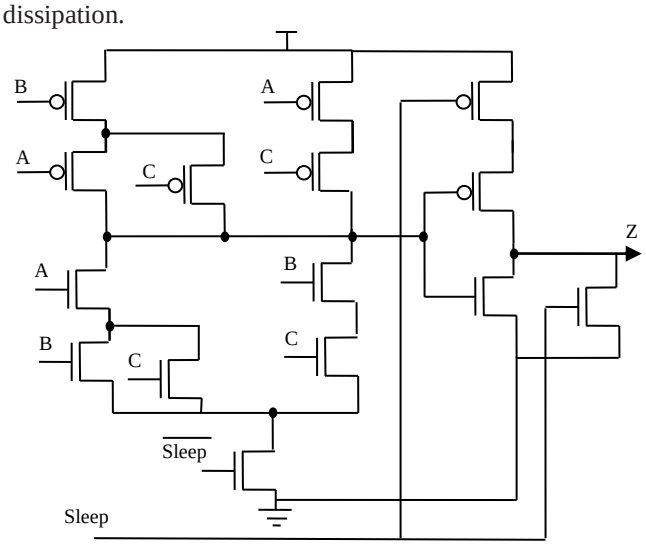

Figure 2(c): Implementation of TH23 gate using MTNCL

The MTNCL implementation of TH23 gate is shown in fig2(c), whose inputs n = 3, threshold m = 2. Initially we presume all the inputs of the threshold logic gate are NULL. If a compelling DATA is propagated through input A, the output remains NULL while no threshold, m=3 is meet. When the next valid DATA is given to either input B or C, the TH23 gate passes the DATA value at the output of the gate since it meets the threshold, m=3. Consequently the absolute DATA wave-front is passed through the yield of the gate insisting input DATA entirety in relation to NULL. If one of the inputs is NULL, the circuit attains DATA at the output attributable to its threshold value. To achieve an absolute NULL wave-front all the inputs of the gate required being NULL and for this reason the gate switches the output to NULL, finally the switching of DATA asserts input NULL completion with respect to DATA.

2.3 Multi Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L): D^{3}L utilizes a dual spacer dual rail delay insensitive protocol. These gates do not use hysteresis, so an external source is essential for circuit operation [13]. So it consumes more area overhead. Therefore MTNCL is integrated in every D^{3}L threshold gate so called Multi Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L) to reduce delay and area overhead. D^{3}L does not require any modification because it previously matches the structure of the modified NCL gates utilized in the MTNCL technique—a hold0 block and a set block [13]. The required modification is the addition of sleep transistors. Sleep – to – 0 (s0), sleep – to – 1 (s1) and their complements are the sleep signals which controls sleep transistors.

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Table 1: MTD^{3}L Sleep Signals

Sleep Signals		Output
s0	s1	
0	0	Normal
0	1	All-One Spacer
1	0	All-Zero Spacer
1	1	Invalid

These two sleep signals should not be asserted at the identical time. If either of these inputs (sleep signals) is asserted, then the circuit will be sleep to the appropriate value. Instead, if one of the inputs is asserted, the circuit will be slept to the correct value.

When S0 is asserted, the gate will sleep in All-Zeros state, i.e. the NMOS transistor, which is parallel to the output inverter, will turn ON, that means the NMOS transistor will organize the main device and gating the circuit to ground, is OFF, and PMOS transistor which is gating the output circuit to supply voltage is too turned OFF [14].

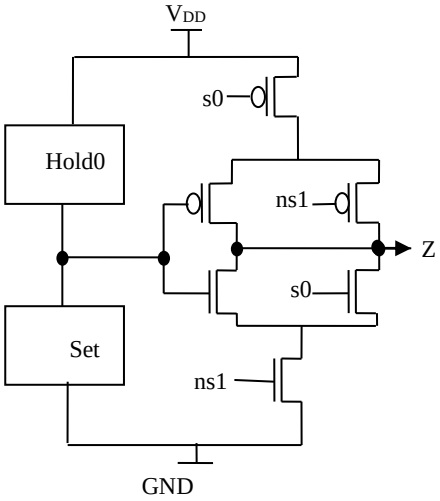

Figure 3(a): Structure of MTD^{3}L Gate

Now, the S1 is de-asserted, the NMOS transistor, which is controlled by complemented s1 (ns1) signal is turned ON, and there is a pathway from the output to ground, that means forcing the output to low. If s1 is asserted, the circuit will sleep in All-One state. i.e.; there is no lane between V_{DD} and circuit, while the pathway to ground remains ON and allows logic low as input to the inverter. The inverter path to ground is OFF and a direct path to V_{DD} is created and forcing the result as logic high.

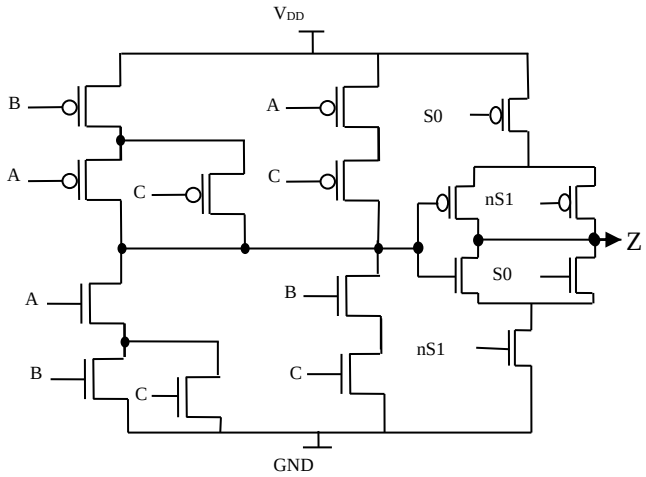

Figure 3(b): Implementation of TH23 gate using MTD^{3}L

Implementation of TH23 gate using MTD^{3}L is shown in fig 3(b). The TH23 gate consists of inputs n =3 & threshold m=2. This design eliminates the power- and ground-gating transistors from the main circuit, leaving only the four transistors on the output inverter. These transistors are controlled by s0 and the complement of s1, allowing for the removal of s0's complement and s1 itself. Thus, only two signals should be buffered instead of four. The snag to this technique is that the main circuit is directly bare to power and ground, eliminating the capability to gate the circuit with high-TV transistors.

2.4 Sleep Convention Logic (SCL):

The CMOS, MTNCL & MTD^{3}L consumes more power and delay. Therefore to reduce those drawbacks, we are combining MTCMOS circuits with NCL. Hence, it is named as Sleep Convention Logic (SCL). In SCL functional blocks are made of threshold gates and implements Boolean functions. For data communication/ transmission SCL uses delay-insensitive encoded data. The trendiest delay-insensitive encoding is dual rail. .A SCL gate is denoted as THmnWw1 . . . , win where n is the number of inputs, m is the threshold value of the gate, and w1, w2, win are the weights of inputs when the weights are > 1. A dual-rail encoded signal D contains two wires, D0 and D1. when D1 = 1 and D0 = 0 then D is logic 1 (DATA1), D is logic 0 (DATA0) if D0 = 1 and D1 = 0, and is NULL when both D0 and D1 are 0. SCL gate is schemed by using SET and HOLD0 blocks. Compared to original NCL, RESET & HOLD1blocks are removed.

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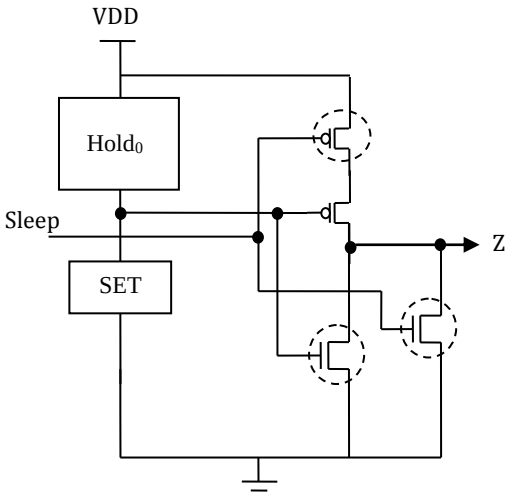

Figure 4(a): SCL functional block

In the SCL circuits, however, since all the gates within the functional blocks are enforced to reset by asserting the sleep signal, input-completeness with respect to NULL is intrinsically ensured and NULL wave front propagation is no longer required. High TV transistors are used to limit the leakage power.

The designing of TH23 gate using SCL technique is shown in fig 4(b). This technique utilizes less number of transistors compared to other leakage reduction approaches. Hence, area overhead is minimized. TH23 gate contains inputs n = 3, threshold m = 2. In initial state we assume all the inputs of the threshold gate are NULL i.e.; circuit is reset to NULL.

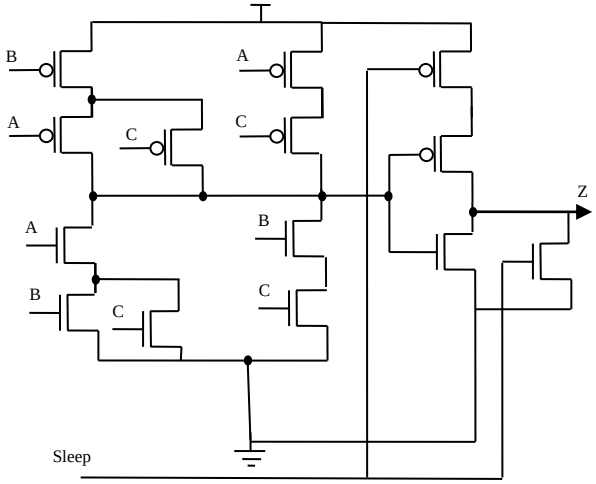

Figure 4(b): Designing of TH23 using SCL

If a DATA is propagated throughout input A, the output remains NULL while no threshold, m=3 is meet. When the subsequently valid DATA is set to either input B or C, the TH23 gate passes the DATA at the output of the gate so it meets the threshold, m=3. Consequently the supreme DATA wave-front is passed through the yield of the gate insisting input DATA entirety in relation to NULL. If one of the inputs is NULL, the circuit provides DATA at the output attributable to its threshold value.

III. RESULTS & DISCUSSIONS

In this paper, CMOS, MTNCL, MTD^{3}L, SCL gates are designed and simulated. All those techniques are compared in terms of power, gate delay, slew rate, rise time & fall time. These methods are verified by the backing of multiplexer. Multiplexer means numerous into one. Multiplexer is a gadget that selects one out of numerous inputs on the called control lines. Multiplexer is used to route any one of the many input signals to a single output. Fig. 5 shows the 2:1 multiplexer. It has two input signals I0 & I1, 1 control signal S and one output signal Z. The output expression of the 2:1 multiplexer is

$$Z = S'I0 + SI1$$

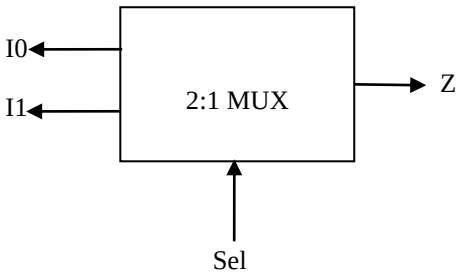

Figure 5: Diagram of 2:1 Multiplexer

In this paper, we have to schemed the 2:1 multiplexer using SCL technique in Mentor graphics tool. Fig 6 shows the SCL implementation of 2:1 multiplexer. THAND0, TH24COMP0, TH22 gates are utilized in the designing of multiplexer in SCL logic.

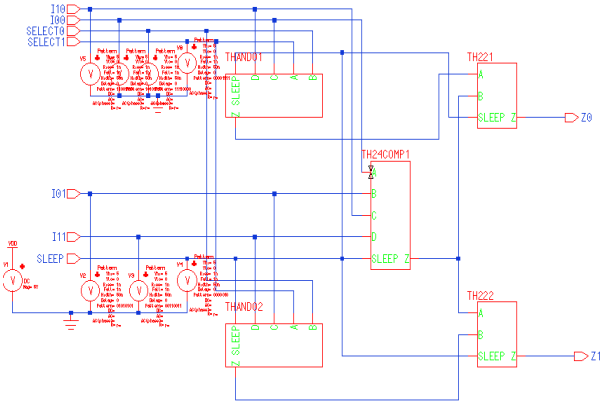

Figure 6: Implementation of Multiplexer using SCL

This schematic is designed in Mentor Graphics 130nm technology using SCL logic which reduces the area overhead compared to CMOS, MTNCL, MTD^{3}L. These Multiplexers are utilized in building digital semiconductors like CPUs and graphic controller, as programmable logic devices, in telecommunications, in computer networks.

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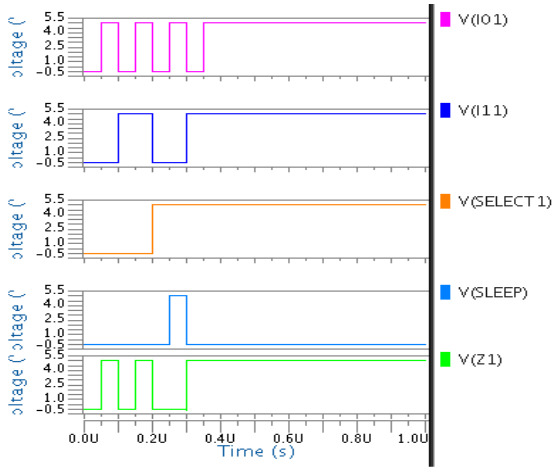

Figure 7: Waveforms of Multiplexer using SCL

Fig 7 shows the simulation waveforms of 2 to 1 multiplexer. In which S is the selection line, Io and I1 are inputs and Z is the output. When S is low, output will pursue I0 i.e. Z=I0. When S is High, output will pursue the I1 i.e. Z=I1. In this way the logic has been verified Multiplexer using SCL.

In this paper, all threshold gates has been analyzed in terms of power, propagation delay, slew rate, rise time and fall time and the values are measured. The area overhead of the SCL technique is lower than that of other approaches.

3.1 Power Dissipation: Power dissipation is an essential property of circuit design which affects reliability. It sways a greater number of design decisions like power supply capacity, battery life time requirements[14]. Table II shows the power dissipation simulation results of CMOS, MTNCL, MTD^{3}L and SCL gates. Where the average power is calculated as

$$P_{avg} = P_{dynamic} + P_{static} + P_{short\text{-}circuit} + P_{leakage} \quad (3)$$

Where P_{avg} is the total average power, $P_{dynamic}$ is the total dynamic power, P_{static} is the total static power while $P_{shortcircuit}$ is the short circuit power & $P_{leakage}$ is the leakage power dissipated by the circuit.

Table II. Power dissipation Comparison (n Watts)

Threshold Gates	CMOS	MTNCL	MTD^{3}L	SCL
TH12	158.15	7.34	156.34	6.78
TH22	7.38	4.18	5.59	4.03
TH13	24.42	8.27	23.58	8.06
TH23	12.79	4.81	9.00	4.55
TH33	6.48	4.02	4.69	3.76
TH23W2	89.66	6.39	81.87	6.12
TH33W2	21.99	4.44	19.95	4.18
TH14	19.47	12.64	13.64	12.41
TH24	24.86	15.26	17.58	14.35
TH34	72.48	8.67	71.94	8.24
TH44	15.54	8.94	14.49	6.54
TH24W2	18.87	12.34	15.76	10.07
TH34W2	10.42	4.28	9.64	3.94
TH44W2	28.64	12.05	26.24	11.02
TH34W3	7.84	6.18	7.57	5.94
TH44W3	12.68	16.48	11.28	16.07
TH24W22	29.30	24.25	28.64	24.06
TH34W22	7.64	8.64	6.47	8.54
TH44W22	13.65	22.46	12.34	22.04
TH54W22	54.27	12.34	47.78	11.17
TH34W32	11.97	8.64	9.30	7.36
TH54W32	8.14	4.52	8.02	4.06
TH44W322	15.94	12.36	13.64	11.93
TH54W322	24.76	8.54	15.94	8.06
THXOR0	15.17	4.55	12.38	4.28
THAND0	9.78	4.81	9.20	4.54
TH24COMP0	72.40	4.05	69.06	4.28
Half Adder	148.80	32.82	135.94	29.84
Full Adder	98.02	39.86	85.72	36.68
Multiplexer	86.73	46.87	75.78	42.81

From this table we observed that SCL principle gives finer performance in terms of power when compared to CMOS, MTNCL, MTD^{3}L. So for low power and ultra low power requirements SCL is an effectual choice for logic circuit designs.

Fig 8 depicting the power consumption Vs Threshold gates Of various asynchronous approaches. SCL technique shows least power dissipation compared to other approaches. Hence SCL is the efficient choice for low power and ultra low power requirements of circuit designs.

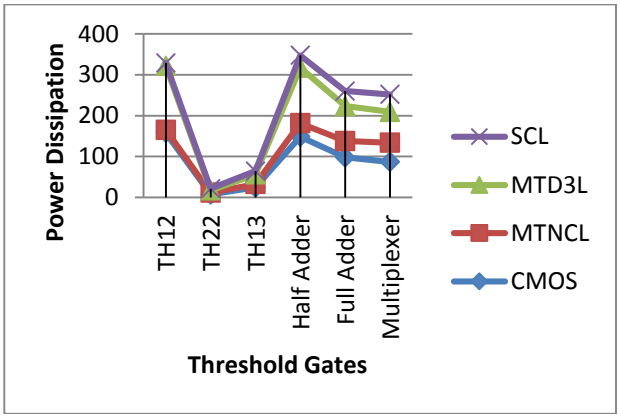

Figure 8: Power Dissipation Comparison between various asynchronous approaches

3.2 Propagation Delay: The propagation delay of a circuit is a key factor on how speedy the circuit is able to work. If one obstruct of the circuit has a high delay, rest of the circuit will have to stay for this one block to supply a valid output. Propagation Delay is the time among when an input to the circuit changes awaiting that change propagates through the circuit and changes the output[14]. If the devices are small then the delay is very short. If the numbers of components are increased in the circuit, then the delay is increases too. Due to this the speed will be reduced. The propagation delay of every transition is a measure from 50% of the input voltage swing to that of the output voltage swing.

$$T_{pd} = (T_{phl} + T_{lph}) / 2 \quad (4)$$

Where Tpd is the propagation/gate delay, Tphl is rising propagation delay and Tlph is falling propagation delay.

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The diminution in the delay gives exact performance of circuit.

Table III. Delay(n sec) comparison between various dual rail asynchronous approaches

Threshold Gates	CMOS	MTNCL	MTD^{3}L	SCL
TH12	35.10	47.64	24.42	42.68
TH22	17.65	36.19	15.99	34.57
TH13	24.14	49.06	15.11	48.74
TH23	50.08	69.04	50.04	64.33
TH33	68.14	87.28	69.00	73.16
TH23W2	150.08	178.87	99.77	106.12
TH33W2	99.97	110.13	99.98	104.67
TH14	57.14	76.93	15.84	52.67
TH24	24.58	43.7	18.76	34.39
TH34	28.68	52.06	25.74	48.24
TH44	80.13	98.64	80.04	86.54
TH24W2	80.64	112.58	70.94	110.07
TH34W2	69.97	85.67	50.49	3.94
TH44W2	40.61	48.06	35.47	45.02
TH34W3	79.75	82.37	50.03	75.94
TH44W3	46.62	66.76	40.72	53.07
TH24W22	79.54	84.34	66.49	80.06
TH34W22	68.49	88.34	63.76	85.54
TH44W22	70.64	98.64	15.60	94.04
TH54W22	40.73	64.37	38.76	63.17
TH34W32	48.37	94.37	32.79	92.36
TH54W32	56.48	74.37	46.49	71.06
TH44W322	49.38	68.76	40.46	67.93
TH54W322	68.76	88.37	42.69	82.06
THXOR0	110.05	129.84	90.04	114.28
THAND0	85.09	99.65	70.06	95.54
TH24com0	112.32	149.86	94.20	97.28
Half Adder	50.08	75.39	38.06	73.84
Full Adder	99.64	112.79	99.63	110.68
Multiplexer	50.01	99.63	49.98	92.81

The propagation delays of the proposed SCL gates are measured and compared with other logic gates and valuated in table III. Compared to other logic designs SCL provides better delay and achieves higher speed of operation but the downside is the MTD^{3}L design provides low delay.

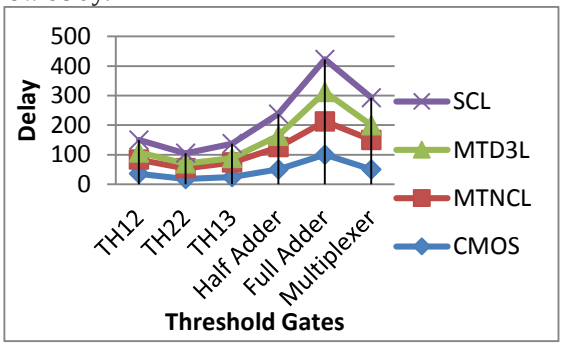

Figure 9: Comparison of Delay between various approaches

3.3: Slew Rate (SR) : Slew rate is defined as the rate of change of voltages per unit time. It is prearranged by

$$SR \geq 2\pi fVpk \qquad (5)$$

Where f is the frequency & Vpk is the peak amplitude of the signal. The high slew rate attains a faster response, i.e., changes the state of the output regarding to the input, especially at high frequencies [14]. Units of slew rate are Volts/Sec.

Table IV. Comparison of Slew Rate (v/µs)

Threshold Gates	CMOS	MTNCL	MTD^{3}L	SCL
TH12	32.80	36.59	23.81	37.07
TH22	25.56	31.65	16.19	32.43
TH13	35.27	38.62	29.63	35.64
TH23	26.30	26.45	19.56	28.95
TH33	18.67	20.70	19.85	22.94
TH23W2	23.77	31.18	19.82	33.76
TH33W2	31.46	47.47	21.97	51.98
TH14	21.34	25.46	11.20	26.46
TH24	30.52	48.49	26.23	49.38
TH34	37.64	46.27	18.63	51.47
TH44	18.49	20.67	15.20	21.67
TH24W2	25.06	32.86	2.99	34.79
TH34W2	18.80	18.98	2.35	18.35
TH44W2	23.51	25.66	9.48	26.55
TH34W3	18.61	20.08	5.26	21.37
TH44W3	24.32	26.03	7.08	27.39
TH24W22	30.23	32.77	11.21	33.76
TH34W22	19.02	22.89	5.67	22.97
TH44W22	15.58	13.46	9.48	14.38
TH54W22	26.08	27.53	11.26	27.73
TH34W32	25.12	30.23	10.23	30.47
TH54W32	15.13	17.62	4.67	18.64
TH44W322	23.56	27.00	8.32	28.71
TH54W322	20.63	24.74	15.69	25.44
THXOR0	20.09	32.27	4.62	32.33
THAND0	26.89	27.26	2.23	28.23
TH24comp0	5.15	5.51	2.98	6.98
Half Adder	25.17	26.19	11.95	27.49
Full Adder	42.45	44.63	16.02	48.49
Multiplexer	28.52	37.05	30.97	38.67

From table IV the evaluated results suggest that the SCL generates superior slew rate compared to CMOS, MTNCL and MTD^{3}Ldesigns and provides quicker response i.e, changes the state of the output with respect to input.

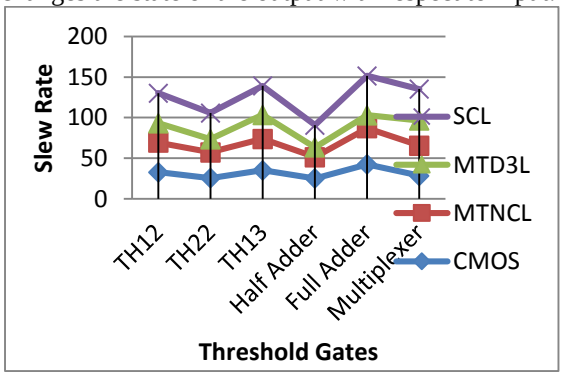

Figure 10: Comparison of Slew Rate

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3.4: Rise Time: Rise is the amount of time it takes the output voltage to go from 10% of the Logic "1" level to 90% of the Logic "1" level. It can be measured in nS. Rise time is an analog parameter of crucial significance in low power and high speed applications. Thus it is an assess of potential of a circuit to act in response to quick input signals.

From table V the simulation results suggest that the proposed SCL technique has higher slew rate than the other approaches. Hence it is the best approach for low power & ultra low power requirements of the circuits design.

Table V: Comparison of Slew Rate (nS) Between Various A synchronous Approaches

Threshold Gates	CMOS	MTNCL	MTD^{3}L	SCL
TH12	48.04	48.06	26.55	87.28
TH22	35.07	82.37	21.37	178.87
TH13	38.18	66.76	27.39	110.13
TH23	24.36	84.34	33.76	76.93
TH33	52.14	88.34	22.97	43.7
TH23W2	64.04	74.37	14.38	52.06
TH33W2	53.01	68.76	27.73	98.64
TH14	34.28	88.37	30.47	112.58
TH24	48.67	43.7	18.64	85.67
TH34	26.08	52.06	28.71	40.61
TH44	22.97	98.64	25.44	79.75
TH24W2	33.76	112.58	32.33	46.62
TH44W2	44.79	48.06	37.07	68.49
TH34W3	66.49	82.37	32.43	86.64
TH44W3	78.49	66.76	35.64	70.73
TH24W22	87.68	84.34	28.95	88.37
TH34W22	83.27	88.34	22.94	96.48
TH44W22	79.43	98.64	33.76	99.38
TH54W22	103.43	64.37	51.98	84.34
TH34W32	68.71	68.76	26.46	88.34
TH54W32	84.27	88.37	49.38	98.64
TH44W322	96.48	43.7	49.38	64.37
TH54W322	33.57	52.06	51.47	94.37
THXOR0	49.76	98.64	21.67	74.37
THAND0	68.09	112.58	34.79	68.76
TH24comp0	105.49	85.67	25.44	88.37
Half Adder	99.47	105.67	32.33	129.84
Full Adder	102.93	118.06	28.23	99.65
Multiplexer	87.51	99.63	65.98	149.86

: Fall time: Fall is the amount of time it takes the output voltage to go from 90% of the Logic "1" level to 10% of the Logic "1" level. The units of the fall time are S.

Table VI: Comparison of fall time among various techniques

Threshold Gates	CMOS	MTNCL	MTD^{3}L	SCL
TH12	23.81	80.04	26.03	86.64
TH22	16.19	70.94	32.77	70.73
TH13	29.63	50.49	22.89	88.37
TH23	19.56	35.47	13.46	96.48
TH33	19.85	50.03	27.53	99.38
TH23W2	19.82	40.72	30.23	84.34
TH33W2	21.97	66.49	17.62	88.34
TH14	11.20	63.76	27.00	98.64
TH24	26.23	85.65	24.74	64.37
TH34	18.63	38.76	32.27	94.37
TH44	15.20	32.79	27.26	74.37
TH24W2	2.99	46.49	5.51	68.76
TH34W2	11.21	40.46	19.56	88.37
TH44W2	5.67	42.69	26.85	129.8
TH34W3	9.48	90.04	36.82	85.67
TH44W3	11.26	70.06	21.97	40.61
TH24W22	10.23	94.20	11.20	79.75
TH34W22	4.67	38.06	66.76	46.62
TH44W22	8.32	53.07	84.34	79.54
TH54W22	15.69	80.06	88.34	68.49
TH34W32	68.71	85.54	74.37	88.34
TH54W32	84.27	94.04	68.76	98.64
TH44W322	96.48	63.17	88.37	64.37
TH54W322	66.76	92.36	43.7	94.62
THXOR0	84.34	71.06	52.06	74.04
THAND0	88.34	67.93	98.64	68.76
TH24como0	98.64	82.06	112.58	88.37
Half Adder	64.37	114.28	85.67	108.1
Full Adder	68.76	95.54	48.06	83.19
Multiplexer	88.37	95.17	82.37	112.0

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V. CONCLUSION

In this paper, we have implemented a low power design techniques and methodologies with the assistance of Multiplexers. The performances of dual rail low power asynchronous logics were compared in terms of power, delay, slew rate, rise time and fall time as shown in the above tabular forms. The Sleep Convention Logic has optimized for power as compared to other approaches. MTD^{3}L provides 50% of reduction in delay while compared with other techniques. SCL provides superior performance in terms of slew rate. By observing the performance, we can infer that the SCL has given better results in all aspects.

V. REFERENCES

[1] Karl M.Fant, "Logically Determined Design: Clockless System Design with NULL convention Logic", ISBN: 978-0-471-68478-7, January 2005.

[2] S.C. Smith and J. Di, "Designing asynchronous circuits using NULL Convention Logic (NCL)," Synthesis Lectures on Digital Circuits and Systems: Morgan & Claypool Publishers, 2009.

[3] Harish Gopalakrishnan, "Energy Reduction for Asynchronous Circuits in Soc Applications," dissertation, 2011.

[4] J. Sudhakar, A.Mallikarjuna Prasad and Ajit Kumar Panda, "Behavior of Self Timed Null Convention Logic Circuits with Threshold Variations", international Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 173-179 (2015).

[5] C.L.Seitz, .System timing,. An introduction to VLSI systems, Addison Wesley, pp.218-262, 1980.

[6] Gerald E. Sobelman and Karl M. Fant, CMOS circuit design of threshold gates with hysteresis,. IEEE International symposium on circuits and systems (II), pp.61-65, 1998.

[7] Gerald E. Sobelman and Karl M. Fant, CMOS circuit design of threshold gates with hysteresis,. IEEE International symposium on circuits and systems (II), pp.61-65, 1998.

[8] M. Shams, J. C. Ebergen, and M. I. Elmasry, "Modeling and comparing CMOS implementations of the C-element," Very Large Scale Integ. (VLSI) Syst., IEEE Trans. on, vol. 6, no. 4, pp. 563–567, Dec. 1998.

[9] Ortega, C.; Tse,J,; Manohar, R., "Static power reduction techniques for asynchronous circuits," Asynchronous circuits and systems (ASYNC), 2010 IEEE Symposium on, Vol., no., pp,52,61, 3-6 May 2010.

[10] Smith, S.C.; Farahad A. Parsan; Liang Zhon; Ravi Parameswaram. "Multi-Threshold NULL Convention Logic: An Ultra-Low Power Asynchronous Circuit design Methodology". J. Low Power electron. Appl. 2015. 5, 81-100.

[11] Jia Di, Scott Christopher Smith, "Ultra-Low Power Multi-Threshold Asynchronous Circuit Design", United States Patent Us 8664977 B2Mar 4, 2014.

[12] T.Verhoff, Delay insensitive codes. An overview,. Distributed computing, Vol.3, pp. 1-8, 1998.

[13] Michael Linder; Jia Di; Scott C. Smith. "Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic: A Low Overhead Secure IC Design Methodology". J. Low Power electron. Appl. 2013, 3, 300-336.

[14] J. Sudhakar, A. Mallkarjuna Prasad and Ajit Kumar panda, "Behavior of self timed NCL circuits with threshold variations", International Journal of Emerging Trends in Engineering Research(IJETER) vol. 3,no. 6,2015.

[15] J. McCardle, and D. Chester, "Measuring an asynchronous processor's power and noise," in Proc. Synopsys Users Group Conf. (SNUG), 2001, pp. 66–70.

[16] S.C. Smith, R.F. DeMara, J.S. Yuan, M. Hagedorn, and D. Ferguson, "Delay insensitive gate level pipelining," Integration, the VLSI journal, Vol. 30/2 pp. 103-131, October 2001.

[17] Harish Gopalakrishnan, "Energy Reduction for Asynchronous Circuits in Soc Applications", Ph.D. dissertation, Wright State University, 2005.

[18] F.A. Parsan, J. Zhao, S.C. Smith, "SCL Design of a Pipelined 8051 ALU", Circuits and Systems (MWSCAS), 2014 IEEE 57th International Mdweat Symposium on, Aug, 2014.