Mixed Signal Model of a 12-bit Pipelined ADC

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***Abstract*— ADC can be considered as the bridge between physical world and digital world;This work presents a behavioral modeling of 12-bit pipelined ADC in Verilog-A. The key advantage of circuit modeling using Verilog-A is that it provides a single language and simulator ecosystem that can be shared between analog system-level as well as device-level designers. Verilog-A leverages the superior speed and capacity offered by traditional Verilog and allows event-driven capabilities within analog model simulation, making it an attractive choice when simulating highly complex mixed-signal circuits such as PLLs, CDRs, ADCs, and DACs.Transient analysis for basic blocks and the overall converter are obtained in Cadence Virtuoso. This work also presents the design of a new version of two stage operational amplifier in 0.18 µm CMOS technology.**

***Keywords*— Pipelined ADC,comparator,CMOS Op Amp;**

I. INTRODUCTION

There are several major types of ADC architectures. A pipelined ADC balances the speed advantage offered by parallelism and area savings by serialism. The pipelined ADC uses a cascade of stages to resolve the input.The analog input which is to be converted is fed to the vin of the stage-1.Stage-1 outputs the digital output d1(MSB) and an analog ouput vout,which is the ouput of MDAC.This analog value is fed to the next stage.Each 1-bit stage is built using sample and hold,comparator and MDAC.This work explores the behavioral modeling and analysis of these blocks and the pipelined ADC as a whole.In addition to that a modified version of two stage CMOS op amp is used within the ADC as comparator circuit.

Section II describes the behavioral modeling of ADC using Verilog-A.Section III presents the modified two stage op amp which is used as the comparator in the ADC later and section IV,the simulated outputs.Section V summarizes the results.

II. VERILOG-A SYSTEM-LEVEL DESIGN

Verilog-A, an advanced analog and mixed signal hardware description language plays the most important role for our Pipelined ADC design in this report. The compatibility with pure HDLs as well as its system simulation ability catches our whole attentions.Each of the building blocks are modeled using verilog-A and simulated in Cadence Virtuoso.

A sample and hold circuit is an analog device that samples the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimum period of time.It samples the input when clock(clk) voltage is greater than the threshold voltage (vth). On clk's negative transition when it crosses vth,the circuit holds the sampled value till it crosses the vth next time. The simulation result of sample and hold circuit is on Fig.4.

A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. In this section we demonstrate a comparator modeled by the Verilog-A HDL. It has two input terminals vin and ref and one binary digital output vout. The simulation result of comprator is on Fig.5.

A multiplying DAC differs from a fixed-reference DAC in that it can apply a high-resolution digitally set gain to a varying wideband analog signal.It is one of the building blocks of the basic 1-bit ADC which is used for modelling the pipelined ADC.Based on the digital input(din) ,the analog ouput(vout) varies.This analog output is fed to the next stage of ADC as analog input.

Using the above mentioned sample and hold circuit,comparator and MDAC a 1-bit ADC is built.It is the main building block of the pipelined ADC modeled.

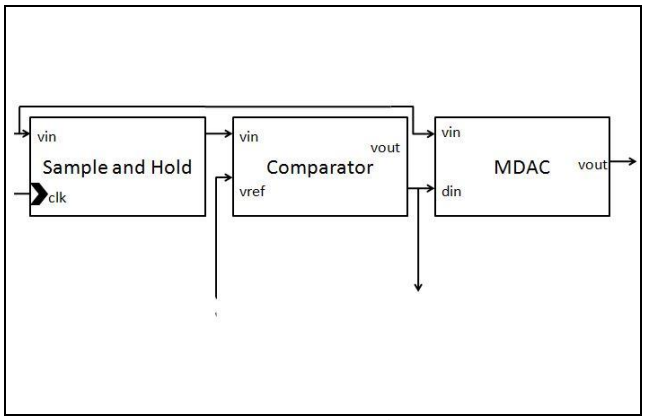

Fig.1. Block schematic of 1-bit ADC

The pipelined ADC uses a cascade of stages to resolve the input.The analog input which is to be converted

is fed to the vin of the stage-1.Stage-1 outputs the digital output d1(MSB) and an analog ouput vout,which is the ouput of MDAC.This analog value is fed to the next stage.

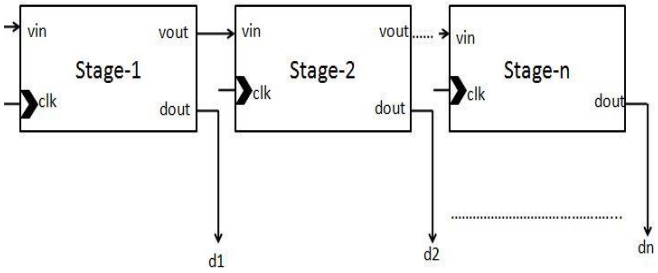

Fig.2. Block schematic of n-bit pipelined ADC

The number of stages decides the resolution of the pipelined ADC.Here each stage belongs to 1-bit;thus n-cascaded stages result in an n-bit pipelined ADC.

III. MODIFIED TWO STAGE OP AMP

Op amp is used as comparator and for sample and hold circuits in analog and mixed signal design. In this op amp[7],nmos1 and nmos2 are differential amplifier's driving transistors and are source coupled.Bias is provided to these transistors using nmos3 and nmos4 which work as current mirror circuits.Differential input voltage is converted into differential current by this transistors.PMOS1 and PMOS2 recover the amplified differential voltage.Second stage is the common source amplifier.This amplifies first stage's output.

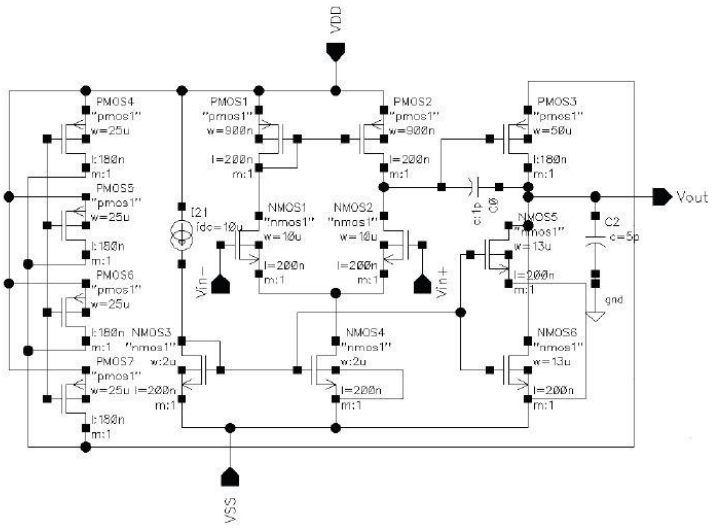

Fig.3. Modified two stage op amp

The transconductance of second stage is increased with the help of the transistors PMOS 4 to PMOS 7.Thus the gain can be increased.

IV. SIMULATION RESULTS

The simulation waveforms for various modules have been analyzed separately and further an integrated module has been designed and analyzed.The waveforms are shown below.

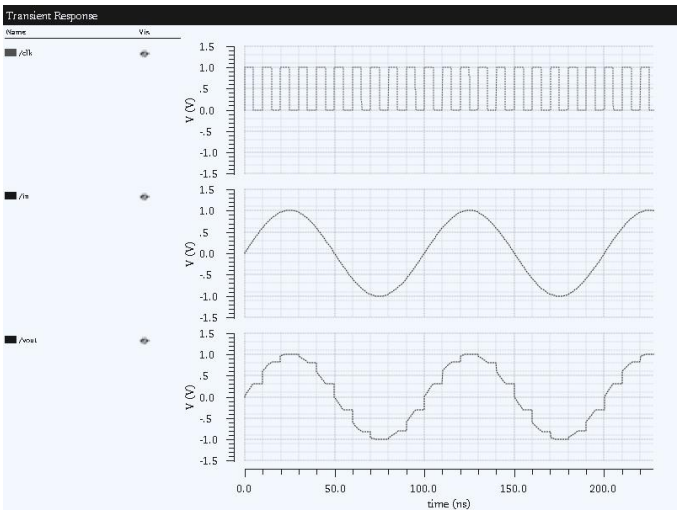

Fig.4. Transient response of sample and hold circuit

The above waveform in fig.4. shows clock signal, sinusoidal input and sampled output respectively. Here we have used the clock frequency higher than twice the frequency of the input signal.It samples the input when clock(clk) voltage is greater than the threshold voltage (vth). On clk's negative transition when it crosses vth,the circuit holds the sampled value till it crosses the vth next time.

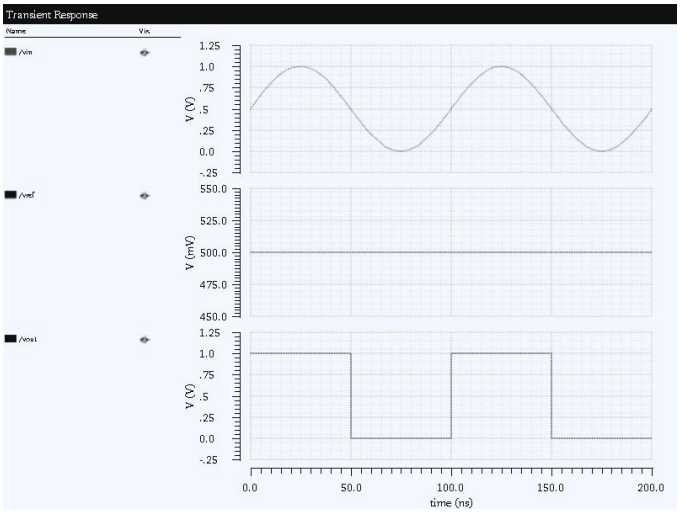

Fig.5. Transient response of comparator

Fig.5. shows the waveform for the comparator unit. The block give proper output depending on the reference voltage and input voltage given. Fig.6. shows the waveform of the MDAC block. Since input voltage is greater than the eference voltage,the output voltage vout=(V(vin)-((V(vdd)-V(vss))/2))*gain. .Fig.7. shows the MDAC output signal

when input voltage is less than the reference voltage.In this case vout= (V(vin))*gain.

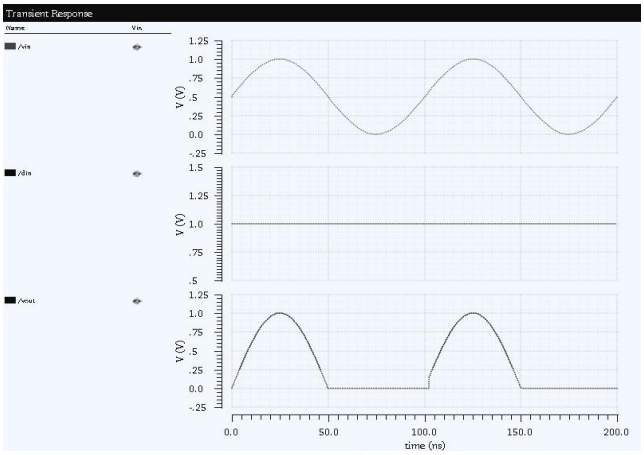

Fig.6. Transient Response of MDAC when din=1

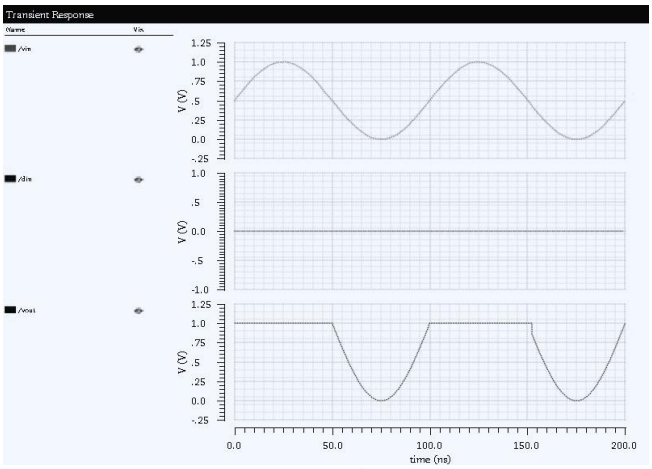

Fig.7. Transient Response of MDAC when din=0

Fig.8. shows the transient response of the above mentioned two stage opamp,when it work as a comparator.The output voltage level is rail to rail.

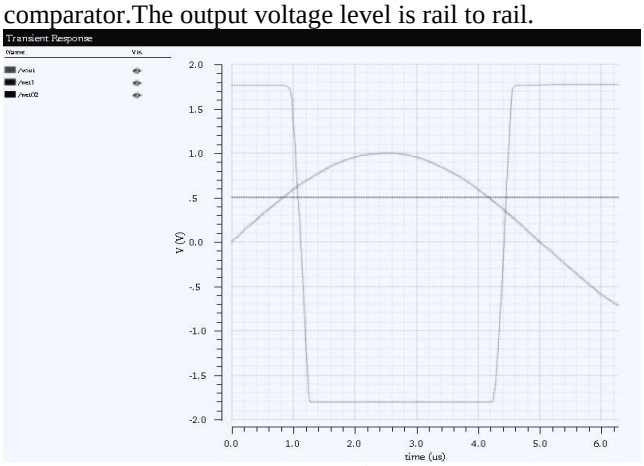

Fig.8. Transient Response of proposed Op AMP

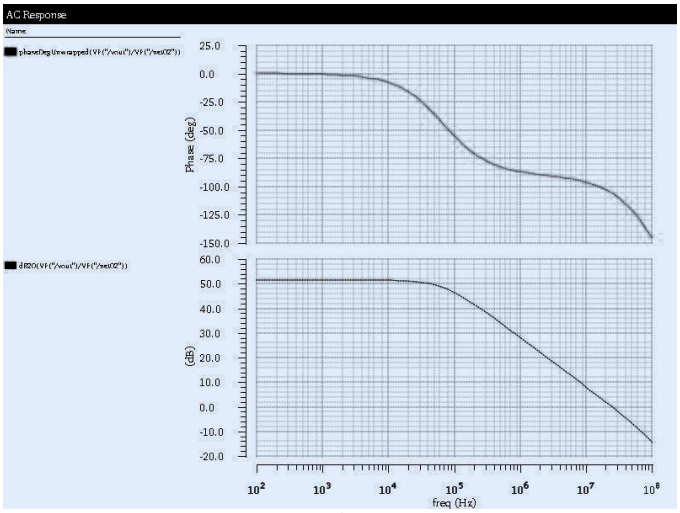

Fig.9. AC Response of Proposed Op Amp

AC analysis is performed to find the gain.The gain of this specific op amp is found to be 51.8 dB.The phase margin is 67.2^{o} and -3dB frequency is 19.34KHz.

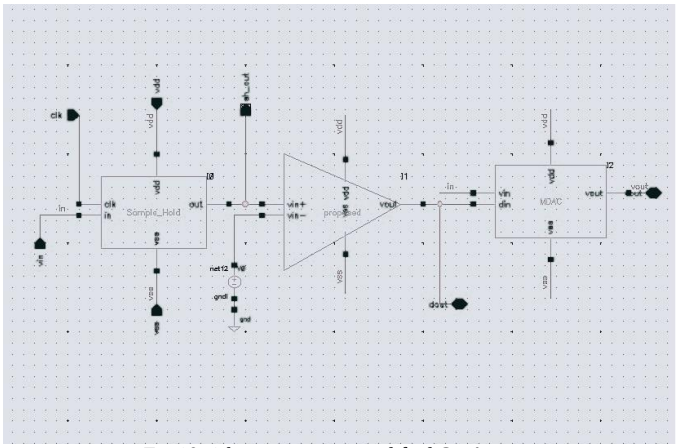

Fig.10. 1-bit stage using modified Op Amp

As shown in fig.10. the modified op amp is used as the comparator in each stage of the pipelined ADC.Fig.11. shows the schematic diagram of 12-bit pipelined ADC in Cadence environment.It consists of twelve stages with 1-bit per each stage.The analog signal which is to be coded is given to the first stage.The analog output of MDAC i.e the residue of one stage is given as the analog input of next stage.Each stage is synchronised with the same clock signal.Here the clock frequency is greater than twice the maximum input frequency.The transient response of 12-bit pipelined ADC modeled in Verilog-A is shown in fig.12.It contains the analog input signal,clock signal and the 12-bit digital output corresponding to the analog input at different instances .Here the simulation is done for 200ns in Cadence Spectre.In fig.13 same simulation is done for 1ns,where the lower significant bits(LSBs) changes are more clear.

Fig.11. Test Circuit Schematic of 12-bit Pipelined ADC

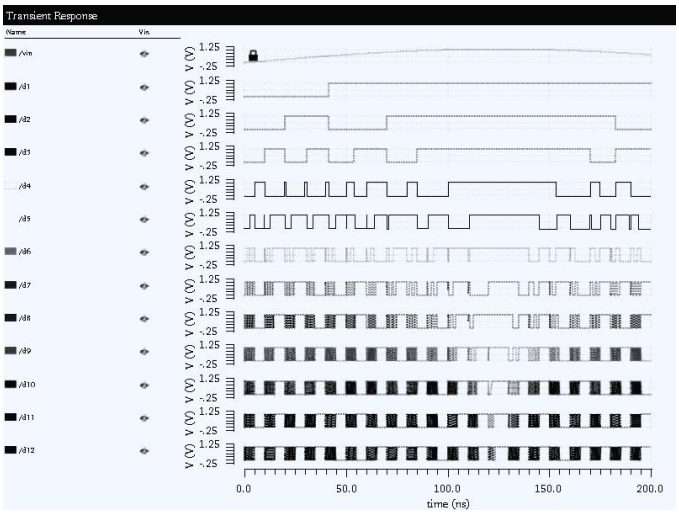

Fig.12. Transient Response of 12-bit pipelined ADC

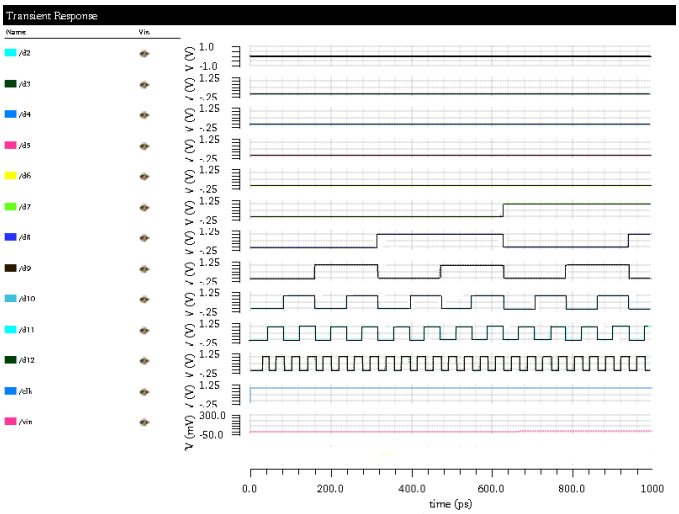

Fig.13. Transient Response for 1ns

V. CONCLUSION

Practical design of the Verilog-A Pipelined Analog to Digital Converter is experienced in this report to convince designers about the compatibilities of Verilog-A in Cadence environment.According to the system-level verilog -A models and simulations presented in this report, we can recognize several advantages of Verilog-A. First, due to that implementing system-level designs and simulations are necessary for the modern complicated mixed signal circuits. Verilog-A becomes a very excellent choice to accomplish this task. Second, modeling in Verilog-A the behavior functions of a block that is going to be designed is fully compatible with Verilog, a pure digital hardware design description language. We can take their merits such as fast design, easy to debug in software and reusable ability in the whole design process.

When ordinary two stage op amps are employed in the 12-bit pipelined ADC, the power is found to be 230.205 µW while with modified two stage op amps it is found to be 130.302 µW.

VI. REFERENCES

[1] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York McGraw-Hill, 2001.

[2] A. M. M. B. Othman and O. Shoaei, “A 0.18µm, 1.8-V CMOS High Gain Fully Differential OPAMP utilized in Pipelined ADC,” IEEE International conference on semiconductor Electronics(ICSE),2006.

[3] J. Mahattanakul, “Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer,” IEEE transaction circuits and systems—II: express brief, VOL. 52, NO. 11, November 2005.

[4] A. Gupta, D.K. Mishra, R. Khatri, U.B.S. Chandrawat and P. Jain, “A Two Stage and Three Stage CMOS OPAMP with FastSettling, High DC Gain and Low Power Designed in 180nmTechnology,”IEEE Computer Information Systems and Industrial Management Applications (CISIM), International Conference 2010.

[5] M. K. Hati and T. K. Bhattacharyya “Design of Low power Parallel Pipeline ADC in 180nm standard CMOS Process,” IEEE International Conference Communication and Signal Processing (ICCSP), 2011.

[6] D. Johns and K. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, 1997.

[7] Anindita Dash, Sushanta. K. Mandal, ” A Low Offset Fast Settling Rail-to-Rail Stable Operational Amplifier in 180 nm Technology” Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013