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Minimizing Power for Transition Faults Using Bs-LFSR and LOC

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Abstract—**In IC assembling there are numerous issues are caught by testing. In this task mostly concentrating on the transition deficiencies. Test cube merge consolidating methodology is already utilized for discover the transition issues and it will attain to low power by decreasing switching transition. Presently in this undertaking proposed two methods for transition faults named as BS-LFSR and LOC. In BS-LFSR, it will produce the pseudorandom designs with low power. The low power is accomplished by lessened switching transition. In launch off-capture system the low power test patterns are attained with expanding the controllability of flaws. With the assistance of Iscas'89 S27 benchmark circuit test results demonstrates that which method is superior to test merging strategy focused around the power and area estimation**

Keywords— ATPG-Automatic Test Pattern Generation. BS-LFSR-Bitswapping Linear Feedback Shift Register, CUT-Circuit Under Test,LOC-Launch-Off-Capture,VLSI- Very Large Scale Integration,SOC-System-On-Chip.

I. INTRODUCTION

Testing methodology is the one of the significant work in all the assembling procedure. In VLSI testing we are trying the fabricated IC. Amid testing process there are numerous faults are distinguished and amended. Here we are concentrating on the transition faults in IC. transition faults are only the stuck at 0/1 flaws. The yields of the entryways are stucked at either zero or one this is called transition faults.

For discovering the deficiencies ,testing methodology is part up into the two sorts. To begin with the first strategy is external testing and an alternate system is Built in self test (BIST). [7][8]This task for the most part concentrating on the BIST. BIST is only the individual test methodology, it is having the Automatic test pattern generator.

In testing, test patterns are created through the ATPG apparatus and it is connected to the CUT (circuit under test) and discovers the deficiencies. In that, test pattern era will devour high power, one of the principle reasons is high switching action, when the switching movement is lessened then power utilization will diminish.

For lessen the power utilization in testing we have to decrease the switching movement, there are numerous strategies are utilized before for accomplish low power utilization on the transition shortcoming finding. Static compaction system [9] [10] is utilized, it will combine the two test cubes shapes, favorable circumstances are low power is accomplished and test block check will be lessened however a few impediments are there normal number of transition is expanded and deferral will expanded.

Reasonable use of rationale [6] is utilized that implies that insertion of rationale entryways between the output cells, the fundamental favorable circumstances are move are diminished and low power utilization is attained to, detriments are test time is expanded and afterward region will be increment.

LS-TDF [3] and FLIS count are utilized here high switching patterns are separated and supplant the low switching patterns, favorable circumstances are switching transition is decreased and low power will be accomplished yet the drawbacks are test time expanded and test patterns check are expanded .Layout mindful compaction method [5] utilized it will produce the equally appropriated switching action in the patterns. Points of interest are deficiency scope expanded and delay disappointments lessened and weaknesses are test pattern number and power is expanded. Test information clamping method [4] is utilized to join the MT FILL and VPRL code, points of interest are information volume diminished and power decreased disservices are included muddling and impact of lapses in transmission.

Uniting test solid shapes accomplish test compaction. The quantity of transition in the sweep chain can be minimized. At the same time it will expand the intricacy. In this paper we are going to look at the execution of 2 methods BS-LFSR (bit swapping direct criticism movement register) and LOC (launch off-capture) for the transition flaws. Lastly this paper will close which system is better, based on the execution examination of zone, power.

II. EXISTING SYSTEM

In existing system test compaction systems are utilized. It is utilized to clamp the information .In this test compaction, for the most part we are union the test cubes shapes. LFSR produces the test cubes squares for transition issues lastly we fuse them for attain to the test compaction.

The principle objective of the current and our proposed paper is to attain to the low power. Fused test cubes shapes will discover the same set of deficiencies; it won't influence the flaw scope. Test cubes shapes are extricated from the practical expansive side tests.

To start with completely pointed out useful expansive side test set is created. What's more it is not a low power test set .Test solid shapes are removed from it for the transition issues. At that point the test solid shape saving some sign transition of the broadside test, from which they are removed.

The switching transition will expand the power utilization, so this current test cubes shape combining is principally centered around switching movement. 0s and 1s changes in the test set are known as the switching transition. In light of blending the test solid shapes the switching transition will diminish in the framework at last we will get the low power utilization.

In our proposed framework, we are utilizing 2 methods BS-LFSR and LOC; it will lessen the switching movement better than the test fusing method, so we will get low power contrasted with the current.

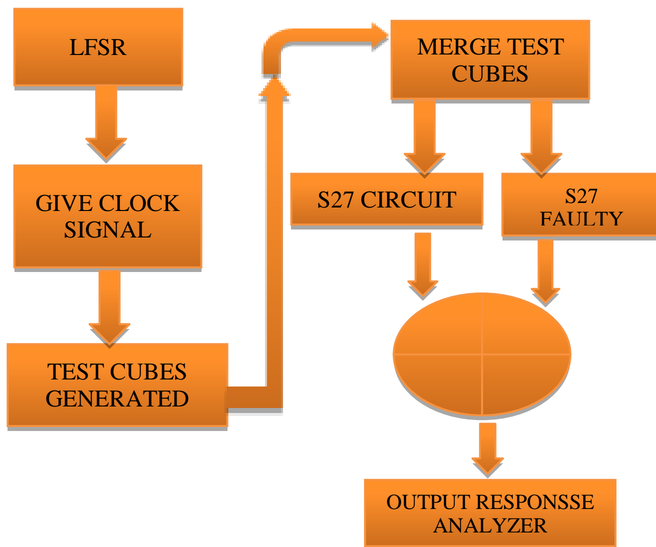

Fig 1. Test Cube Merging

III. PROPOSED SYSTEM

BS-LFSR TEST PATTERN GENERETION

A. CONVENTIONAL LFSR TEST PATTERN GENERATION:

In typical test pattern era, LFSR is structured by XOR and flip flop. It performing XOR on the yield of the two or more flip failure and afterward encouraging those yields back into the info of one of the flip flop and it create the PRPG , clock sign is the imperative one in the LFSR for test pattern era.

B. MODIFIED LFSR TEST PATTERN GENERATION:

In the modified LFSR it comprises of customary LFSR and 2*1 Multiplexer. BS-LFSR will decrease the switching transition contrasting with the customary procedures so we are attaining to the low power. Switching transition will typically expend more power in the traditional LFSR yet in the proposed BS-LFSR it will be lessening. So this is the one of the fundamental preference in BS-LFSR, for that we are utilizing the 2*1 multiplexer as a part of the structural planning.

Figure 1 graph demonstrates the building design chart for the Bit Swapping Linear Feedback Shift Register. It decreases the normal switching movement in test operation by decreasing the quantity of switching transition.

Bit Swapping LFSR outline is focused around some method that is utilized to portray the switching transition movement in BS-LFSR. By utilizing this method we can without much of a stretch characterize how switching transition of bits happens in pattern era.

There are numerous procedures to diminished power utilization there is some immediate methods are there for diminishing power yet it will expand the timing of test and are not relevant for decreasing top power. Bit-Swapping LFSR will lessen both normal and top power scattered by CUT.

In altered LFSR we apply the swapping property between the each pair of nearby cells of the ordinary LFSR for outline the BS-LFSR. In the n-bit maximal length LFSR is changed utilizing the swapping course of action, we pick one of its yield is to be a choice line that will swap the two neighboring bits.

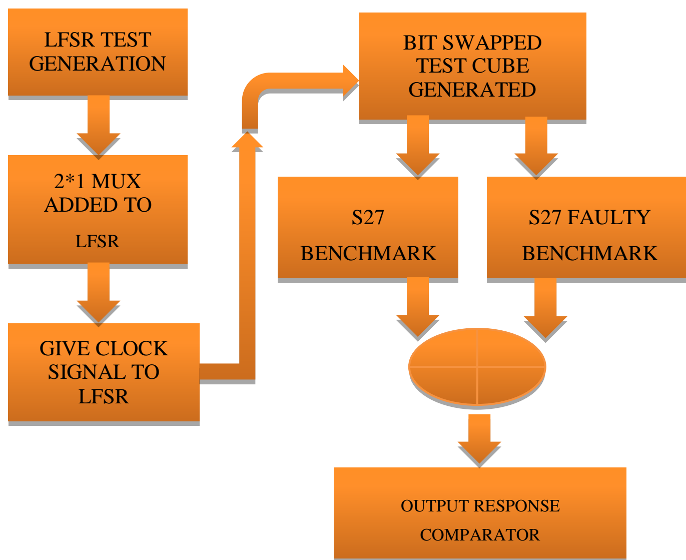

Fig 2. BS-LFSR ARCHITECHTURE

Properties:

1. Modified LFSR will create the precisely same as the typical LFSR however the test pattern produced request will be diverse.

2.BS-LFSR create same number of 0s and 1s in the yield of multiplexers in the wake of swapping of two nearby cells

3.BS-LFSR is utilized to create test patterns for the essential inputs of an output based successive circuit. At that point consider that bit1 will be swapped with bit2 and bit3 will be swapped with bit4...… ... bit n-2 with bit n-1 as indicated by the estimation of bit n which is joined with the choice line of the multiplexer.

4.For n-bit maximal length LFSR that begins with any seed and runs for 2n clock cycles until it comes back to the beginning seed quality.

5.Then the aggregate number of transitions is

$$T \text{ all out} = n*2(n-1)(1)$$

6.So in the wake of swapping the swap bit will subsequently spare power.

$$T \text{ spared} = 2\ (n-2)/\ (2*2(n-1))=25\%$$

7.The general transition in the essential data of the CUT will be diminished 25%

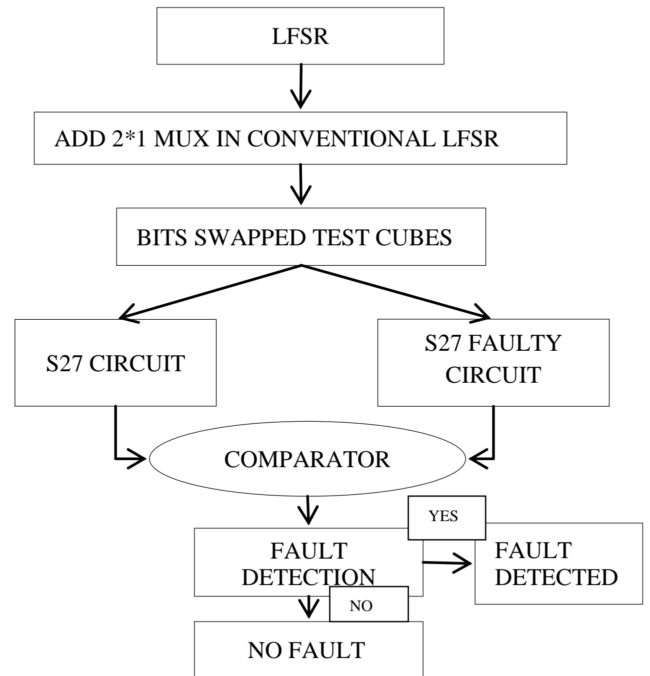

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Fig 4. Flow Char For BS-LFSR

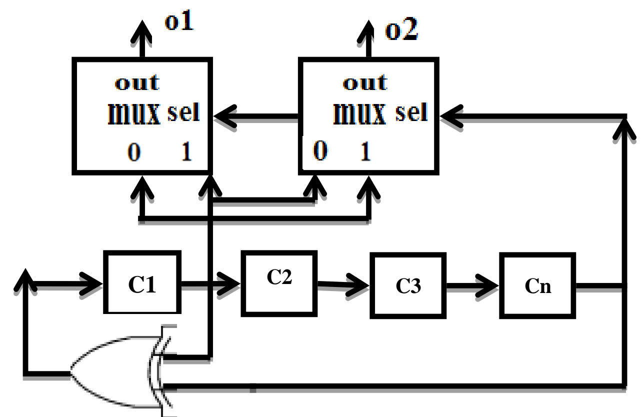

Fig 3. BIT-SWAPPING LFSR

IV. PROPOSED SYSTEM 2

LOC-(LAUNCH-OFF-CAPTURE)

In this paper we proposed two strategies BS-LFSR and LOC. Presently we are going to see about launch off-capture. The LOC system is for discovering the transition deficiencies, in this strategy uses the utilitarian reaction of the circuit to launch the transition at a target entryway terminal and spread the shortcoming impact to a noticeable point.

The principle objective of this paper is to decrease the power utilization. By utilizing the LOC system power utilization is lessened amid launch and capture operations in at- pace testing. This strategy is to reuse the patterns created by a routine power ignorant transition delay ATPG apparatus in place and apply them in a low power way.

The transition deficiency and way postpone flaw testing give a decent scope to defer incited imperfections. Transition issue model focuses on each one entryway yield in the outline for a moderate to climb and moderate to fall deferral shortcoming. Transition deficiency testing broadly utilized as a part of industry for essentially to oversee and control the issue number.

To test a transition blame, an pattern first is connected to introduce the circuit and an alternate pattern is utilized to apply a transition at a target terminal. The reaction is seen at the yields of the CUT (circuit under test). The output based test produced by a programmed test pattern generator (ATPG) is principally utilized as a savvy option to the at-rate practical pattern approach.

LOC is going to perform the transition issue test in sweep based strategy, an pattern pair V1 and V2 is connected to the circuit-under-test. In the first place design V1 is termed as the introduction pattern and V2 is termed as the launch pattern.v2 dispatches the sign transition (0 to 1 or 1 to 0) at the craved hub. It likewise serves to engender the yield transition to the yield of CUT (essential yields or output flip failures). The reaction of the circuit under test for the pattern V2 is caught at the utilitarian velocity. The aggregate operation can be isolated into the 3 cycles: 1. Introduction cycle, where the CUT is introduced to the specific state (V1 is connected) , 2. Launch cycle where the transition is propelled at the target entryway terminal (V2 is connected), lastly 3. Capture cycle, where the transition is proliferated and caught at the target door terminal (V2 is connected), lastly 3. Capture cycle, where the transition is proliferated and caught at a discernible point.

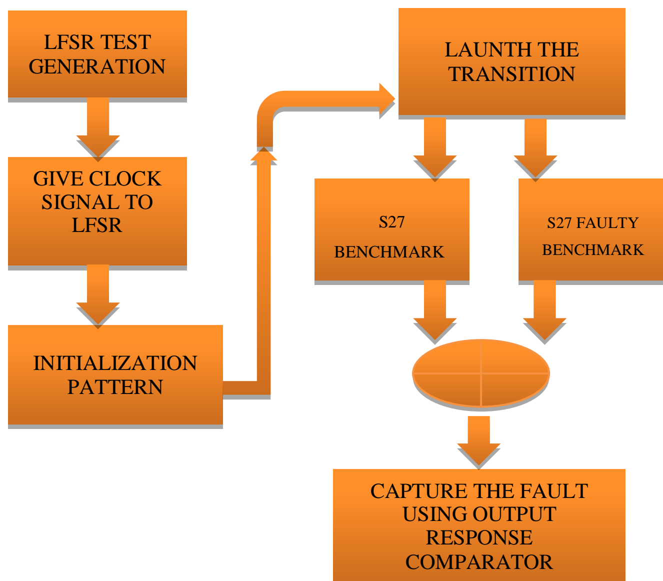

Fig 5. LOC- Launch-Off-Capture Architecture

V. ISCAS 89' – S27 BENCHMARK CIRCUIT

In this paper we are utilizing S27 circuit, which has a place with ISCAS 89' benchmark circuit family and it is absolutely consecutive circuit with four inputs. The circuit has been tried by utilizing Built As a part of Self Test. At first blames are embedded into the circuit. For every last blame pseudorandom patterns are connected comparing test vector will be taken. These vectors are isolated into two sub bunches for diminishment of transitions. The quantity of transitions are decreased the power utilization is diminished. On the off chance that the yield estimation of broken S27, and S27 typical circuit are distinctive then blame has been secured.

VI. EXPERIMENTAL RESULTS:

In this paper we are utilizing VHDL project, and we are going to utilize two product, MODELSIM, and Xilinx. Modelsim instrument is utilized for measuring the exact deficiency discovery, and Xilinx device is utilized for measuring the territory, power and postponement .We are utilizing ISCAS 89' S27 benchmark circuit. Figure7 will shows the fault detection output using MODELSIM. Figure 8,10 shows the power measurement using XILINX. Figure 9,11 shows the area measurement. Based on the results existing techniques power consumption is 29.03mW.and proposed BS-LFSR achieve 28.74mW.

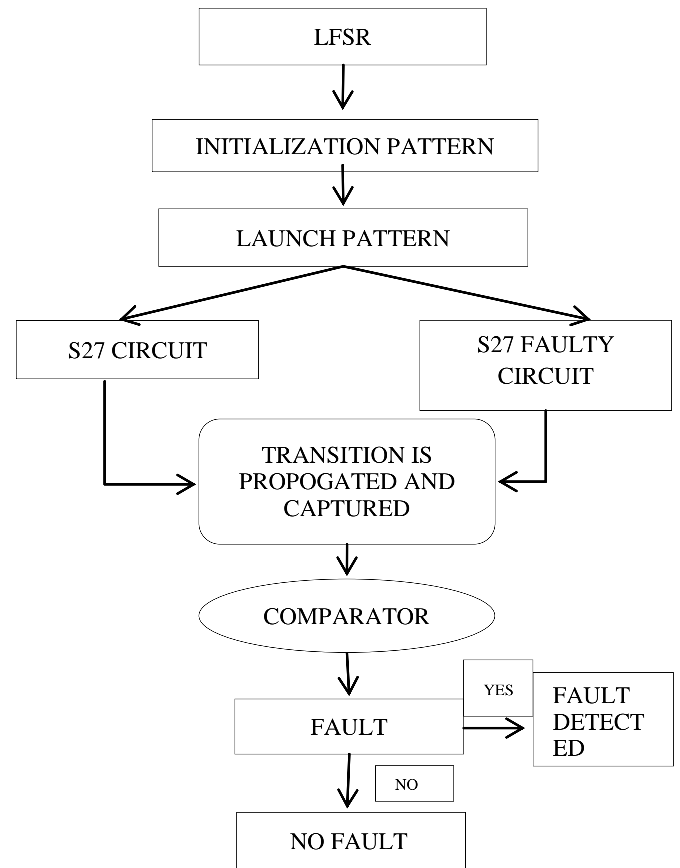

Fig 6. Flow Chart For Loc

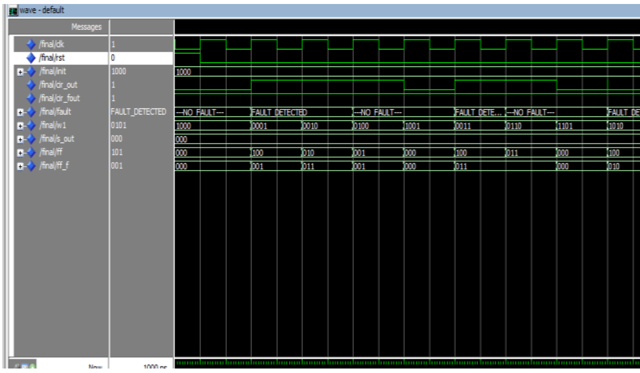

Fig 7. FAULT DETECTION OUTPUT USING MODELSIM

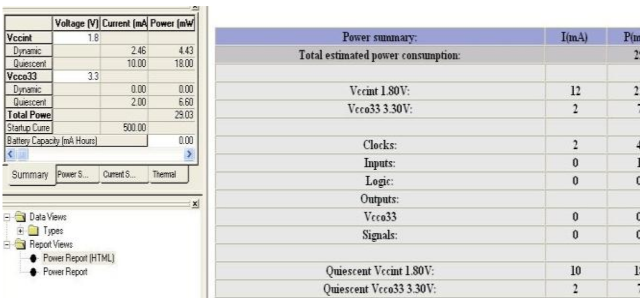

Fig 8: TOTAL POWER MESASUREMENT FOR TEST MERGING USING XILINX

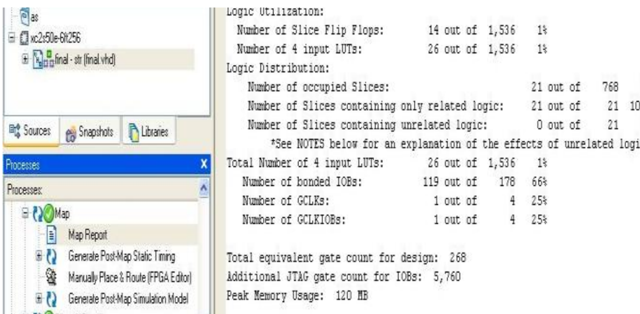

Fig 9. AREA MEASUREMENT FOR TEST MERGING USING XILINX

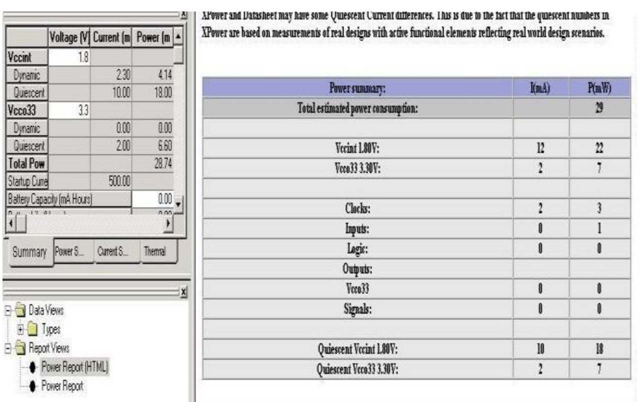

Fig 10. TOTAL POWER MESASUREMENT FOR BS-LFSR USING XILINX

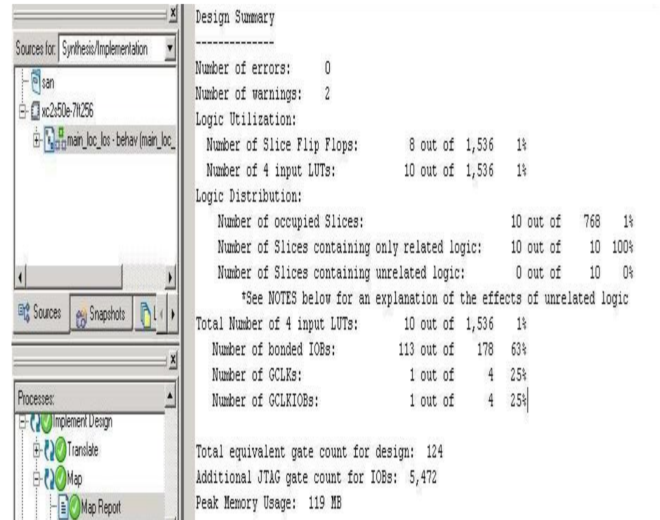

Fig. 11 AREA MEASUREMENT FOR BSLFSR USING XILINX

VII. CONCLUTION

In this paper we are created the test patterns for transition issues utilizing this proposed two strategy BS-LFSR and LOC. In BS-LFSR Bit Swapping strategy is connected to the customary LFSR and we utilized 2*1 multiplexer then as a part of LOC we are part the operation in 3 cycles initialization cycle, launch cycle, capture cycle. By utilizing these 2 proposed system we conclude that based on the area and power measurement of BS-LFSR is better than the test merging . Future work is to find the LOC measurement and fault detection.

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