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Micromachined MEMS Transmission Line Low Loss Phase shifter

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***Abstract*—The design, fabrication & measurement of surface micro machined true time delay distributed MEMS transmission line (DMTL) low-loss Phase shifter is described. The phase shifter is fabricated on a glass substrate consists of a high-impedance coplanar waveguide transmission line & a bunch of MEMS bridges at height g_o = 1.5 µm, from the center conductor. Numerical Simulation (using EM Simulator CST Microwave Studio) results along with wafer level measured results of the fabricated structure are presented. A phase shift of 120°/cm is measured with 0.39 dB/cm loss at 14GHz.**

I. INTRODUCTION

The field of RF-Micro Electro Mechanical Systems has seen enormous growth in recent years due to its potential for high performance in defense and commercial applications. Many microwave circuits using MEMS devices have demonstrated outstanding RF performance and low DC power consumption. MEMS Phase shifters are gradually becoming passive devices of great value due to its inherent advantageous of small size, low signal attenuation & low DC –power dissipation. Phase shifters loss directly impacts the signal's dynamic range. MEMS Phase shifters designed with MEMS switches to alter the signal paths [1,2] are inherently digital & are not suitable if large number of phase states are required. Phase array antenna for example requires high resolution phase control, which would lead to a large and lossy digital phase system. The fabrication of analog adjustable components like DMTL phase shifters requires several equal, tunable capacitances loading a transmission line [2,3]. An analog phase shifter that has high impedance CPW transmission line with bridges across the line acting as tunable capacitors are periodically loaded, which in turn changes the phase velocity and consequently varying phase shift, upon altering the height of the bridge through electrostatic actuation. This type of configuration referred to as distributed MEMS transmission line (DMTL) phase shifters are well documented by Barker [4,5]. Greg McFeetors & Michal Okoniewski have enhanced tuning range of capacitors by using oxide layers on electrodes (CPW – ground) & fixed bridge to form large capacitance [6]. The DMTL Phase shifter described in this paper is optimized for higher phase shift per dB loss. Phase shifters have many applications in instrumentation systems, wireless communication circuits and in phased array antennas for telecommunications and radar applications. RF MEMS phase shifter has advantage over traditional phase shifters based on ferrite material, PIN diodes & FET devices. MEMS phase shifters have low loss, consume less power, & have better performance.

II. DESIGN

The coplanar waveguide (CPW) transmission line is used as a foundation block for phase shifter. The planar attribute of CPW lines provides convenience for MEMS structure construction & on wafer characterization. Minimizing the transmission loss is one of the primary goals. Two major factors are the reflection and dissipation losses. To minimize the reflection loss, the characteristic impedance needs to match with that of the rest of the circuitry. The dissipation loss consists of three mechanisms: 1) The skin effect, 2) Metal conductive losses, & 3) Dielectric losses. By properly choosing a good conductor (gold), a micro-scaled MEMS device can have very low skin effect and conductive losses. The dielectric loss is inherently low due to the usage of glass substrate. A CPW line with input impedance Z_o= 49 Ω is used as feed lines with dimensions, width W=120 µm & gap G =15 µm Fig. 1. The DMTLs used has unloaded impedance of Z = 96 Ω, with center conductor width W =102 µm & gap G = 148 µm Fig. 1. The bridge has width w = 31.5 µm and gap g_p = 10 µm, between each bridge, bridge thickness t_b = 1 µm & seven bridges form one bunch Fig. 1. This line is loaded with 4 bunches of bridges spaced s = 518 µm Fig. 3. The tunable capacitive loading by bridges C_b divide by bridge spacing s along with per-unit length capacitance C_t influences the line impedance (1), as well as the phase velocity v_p (2). The bridge-variable MEMS capacitors have an electrostatic force as actuation principle. Nichrome DC bias pads are under the bridge. DC actuation does move the bridges by electrostatic actuation. The relationship between the actuation voltages V_p, spring constant k of the bridge, capacitor plate widths –center conductor width W, bridge width w & height of the bridge g_o, is indicate in (3). Fig. 1 show the dc bias-actuation line physically separate from the transmission line resulting in a good isolation between DC and microwave lines [7]. The per unit length inductance L_t and Capacitance C_t are 546 nH & 58 pF respectively. The parallel plate bridge capacitance $C_b = C_{ll} + C_f = 133 + 37 = 170$ fF, for the bridge height $g_o = 1.5$ µm & the loaded line impedance of DMTL line $Z_l = 37\ \Omega$. The load impedance $Z_l = 42\ \Omega$, for the bridge height go = 1 µm. Z_l is extracted by noting the S_{11} peak of 15 dB ($\Gamma = 0.18$) & knowing that the DMTL will act as a quarter wave transformer at this frequency. The substrate is glass($\varepsilon_r = 4.82$) with dimension 5124 µm x 2130 µm x 500 µm.

s - Space between bridges

C_t - Equivalent Transmission Line per Unit Length Capacitance.

L_t - Equivalent Transmission Line per Unit Length Inductance.

C_b - Bridge Capacitance

W –Width of the center conductor

w – Width of the bridge

ε_0 - Free space permittivity

k- Bridge spring constant

g_0 – Height between bridge and center conductor.

v_p – phase velocity.

V_p- Pull in Voltage.

$$Z = \sqrt{\frac{sL_t}{sC_t + C_b}} \qquad (1)$$

$$v_p = \frac{s}{\sqrt{sL_t\left(sC_t + C_b\right)}} \qquad (2)$$

$$V_p = \sqrt{\frac{8k}{27\,\varepsilon_0 W w}\, g_0^3} \qquad (3)$$

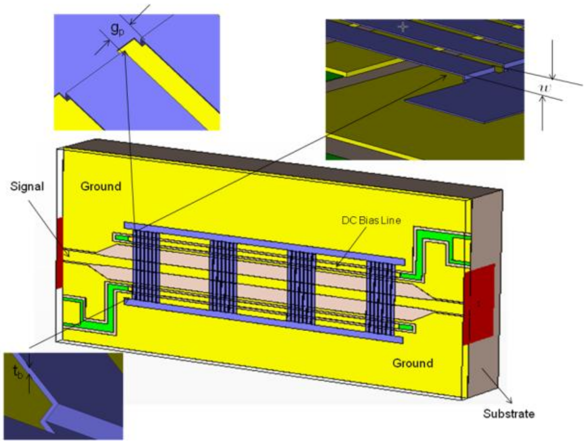

Figure 1. Electromagnetic Simulation Model.

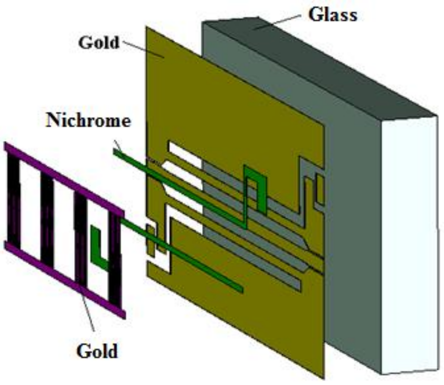

Figure 2. Layers of Electromagnetic Simulation Model

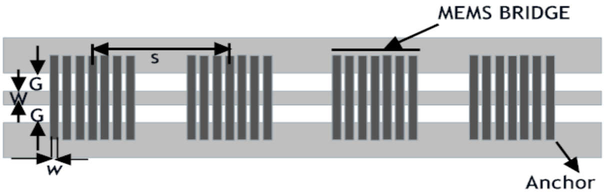

Figure 3. DMTL Layout model.

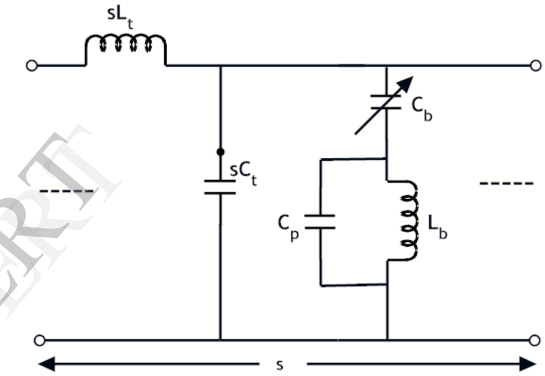

Figure 4. DMTL – Lumped Circuit equivalent unit section model of DMTL.

C_b - Bridge Capacitance (between Center Conductor and Bridge)

L_b - Bridge Inductance.

C_p - Capacitance between bridges. (Due to bridge thickness t_b and gap g_p)

III. SIMULATION

Computer Simulation Technology AG, Microwave Studio electromagnetic simulation tool was used for simulating the model Fig. 1. The bridges are constructed with a conductor layer of gold with conductivity.4.09e+007 S/m, the CPW center conductor and ground are made of gold Fig. 2. The layout model is created using the graphical interface available in the simulation tool. The simulated and wafer level measured S - parameter results of upstate bridge position (g_o = 1.5 µm), without applying actuation voltage are presented below.

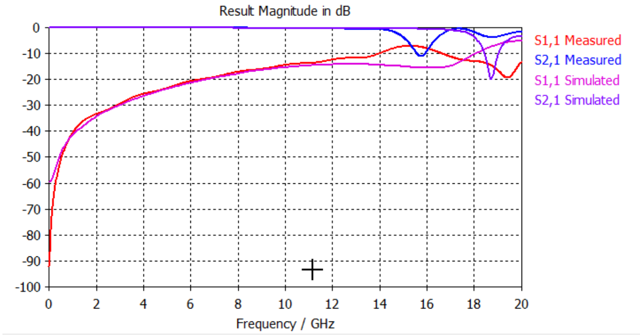

Figure 5. Measured and Simulated S- Parameter Results of DMTL- g_o = 1.5µm

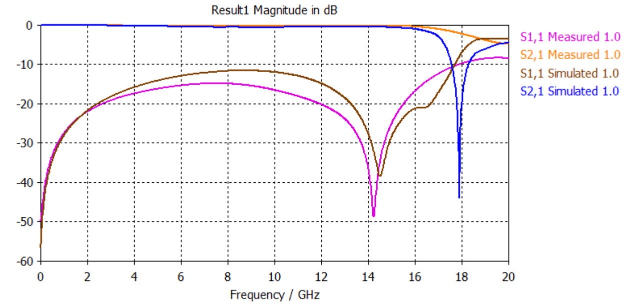

Figure 6. Measured and Simulated S- Parameter Results of DMTL- g_o = 1.0µm

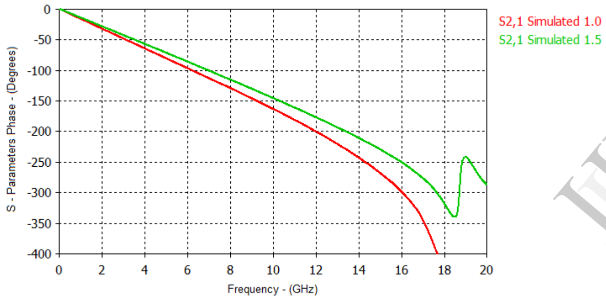

Figure 7. Simulated Phase Shift Results of DMTL- g_o = 1.5µm & g_o = 1.0µm

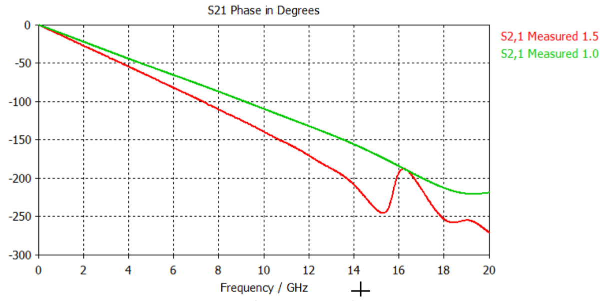

Figure 8. Measured Phase Shift Results of DMTL- g_o = 1.5µm & g_o = 1.0µm

IV. FABRICATION

Surface micromachining technology process is used, unlike bulk micromachining where a substrate is selectively etched to produce structures, surface micromachining is based on the deposition and etching of different structure layers [8,9]. Corning glass substrate is used.

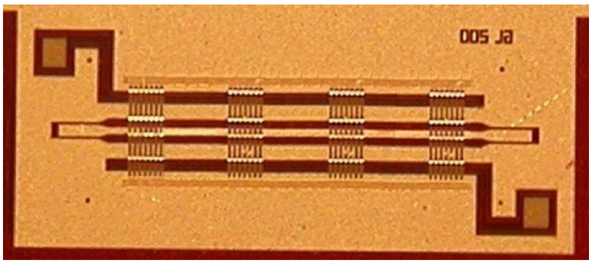

Figure 9. Fabricated DMTL phase shifter

$$\Delta\varphi = \frac{\omega Z_0 \sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) rad/m \qquad (4)$$

$\Delta\varphi$ – Phase shift.

Z_0 – Input impedance.

Z_{lu} – DMTL - Impedance when the bridge is in upper state- g_o – 1.5 µm

Z_{ld} – DMTL – Impedance when the bridge is in lower state g_o – 1.0 µm

ε_{eff} – Effective dielectric constant

c – Speed of light.

ω – Angular frequency

Loss:

The transmission line loss (α) for the unloaded CPW line is found from a conformal mapping technique, and is given by Hoffmann [10].

$$\alpha = \frac{8.686.10^{-2} R_s \sqrt{\varepsilon_{eff}}}{4\eta_0 S K(k) K(k')(1-k^2)} X \qquad (5)$$

Where,

$$X = \left[\frac{2S}{W}\left\{\pi + \ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right\} + 2\left\{\pi + \ln\left(\frac{4\pi S(1-k)}{t(1+k)}\right)\right\}\right] dB/cm$$

S = CPW line width (*W+2G*)

G- CPW line gap between center conductor and ground.

K(k) & *K(k')* = Complete elliptical integral of first kind

t = thickness of the conductor

Where t is the metal thickness, R_s is the surface resistance given by $R_s = \sqrt{\pi f \mu_0/\sigma},$ and σ is the conductivity of the metal. The CPW line is of thickness t = 3 µm of gold with a conductivity of approximately 4.09 x 10^7 Siemens / met.

μ_0 -free space permeability.

V. MEASUREMENTS

Wafer level measurements were taken using Cascade Microtech probe station & Agilent PNA 8362 B Network analyzer. The simulated and measured S-parameter results are in good agreement Fig. 5. The simulated and Measured S-Parameter results for g_o = 1 µm has mismatch due to the variation in height of the various bridges along fabricated structure Fig. 6. At 14 GHz. the calculated phase shift is 90^o/cm, using (4), the simulated phase shift is 97^o/cm. & the experimental / measured phase shift is 120°/cm. The discrepancy may be due to non-uniform height of the bridge along the structure. The loss at 14 GHz. S_{21} is 0.2 dB (Measured). The bridge has length of 762µm, the bridge inductance L_b = 235 pF, thickness of the bridge t_b = 1µm, the gap g_p between bridges is 10 µm & the parallel plate capacitance due to this gap between bridges is 5.31 aF (5.31e-18). The fringe capacitance is 25% of parallel plate capacitance [5]; hence the total capacitance C_p =6.63 aF. The effect of self resonance of the bridge inductor in parallel with capacitance is the cause of dip in S_{11} at 18.7 GHz. (Simulated) & at 15.7 GHz. (Measured) - Fig. 5.

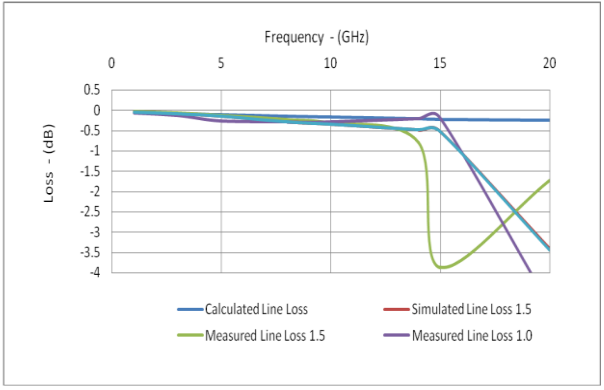

Figure 10: Measured, Simulated & Calculated Loss versus Frequency for Unloaded CPW line & Loaded DMTL on Glass with center conductor 102 µm wide (Zo = 96 Ω)

The Fig. 10 shows the line loss of CPW unloaded line calculated from (5), simulated line loss of DMTL and measured line loss of DMTL at g_o = 1.5 µm & 1.0 µm. The measured line loss at 1 µm over a frequency range is better than the measured line loss at 1.5 µm since the line impedance match is better. Z_l = 37 Ω at g_o = 1.5 µm & Z_l = 42 Ω at g_o = 1.0 µm, the calculated line loss is less compared to the simulated loss as it does not take care of the standing waves on transmission line. The standing waves increase the loss of the line. The rapid increase in line loss at 14 GHz for measure line loss at g_o = 1.5 µm, at 15 GHz for simulated line loss & measured line loss at g_o = 1.0 µm is due to self resonance of bridge inductor at 14 GHz & 15 GHz.

TABLE I. DMTL Comparison

Device	Loss	Phase Shift / cm	Phase Shift / dB	Frequency
Barker[4]	1.7 dB/cm	120° / cm	70° / dB	@ 40 GHz
W.Palei [11]	2.0 dB/cm	150° / cm	75° / dB	@ 20 GHz
This work	0.39 dB/cm	120° / cm	307° / dB	@ 14 GHz

VI. CONCLUSION

The measured results indicate a phase shift 120° /cm, 0.39 dB/cm losses at 14GHz with Figure of Merit of 307° / dB - Phase Shift / dB. This is the lowest loss for maximum phase shift reported in the literature. Work is underway to push the self resonance frequency beyond 30 GHz, by variation of bridge inductance, so that the reflections from the self resonance have less effect on the return loss in band up to 20 GHz.

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