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Methodologies used for Power Optimization

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Abstract: In any electronic device the most important aspect which is needed to be taken into consideration is reduction in power consumption. As the technology is improving it is also needed to concentrate on size of the device. Since the early days, switching capability of the MOS transistor has been exploited by a wide variety of applications. By applying a high voltage or low voltage on the gate contact, the current flow between source and drain can be switched on or off, respectively. The off-state current was supposed to be very small. This variation in input voltage leads in variation of threshold voltage.

The optimization of power can be done by reducing the power loss when the MOS is in stand by mode. The paper discus about methods used for power optimization.

Keywords: MOSFET, finFET, Sub-threshold level, leakage power

I. INTRODUCTION

As VLSI devices have grown in complexity and density, their power consumption has become a major design concern. In CMOS digital circuitry, power dissipation consists of dynamic and static components. Since dynamic power is approximately proportional to the square of supply voltage *V*&and static power is proportional to *Vdd*, lowering supply voltage is the most effective way to reduce power consumption as long as dynamic power k dominant. . Power optimization is the use of electronic design automation tools to optimize (reduce) the power consumption of a digital design, such as that of an integrated circuit, while preserving the functionality.

Low voltage operation is an appealing method to reduce the power consumption of VLSI circuits due to its quadratic saving in switching energy as supply voltage scales down. This quadratic reduction is dictated by the well-known EQ1.

$$E = \frac{1}{2} C V_{dd}^{2} \qquad [EQ1]$$

Supply voltage scaling down to near or below the threshold voltage (V_{th}) of the devices, which we refer to as near-threshold and sub-threshold operation [1].

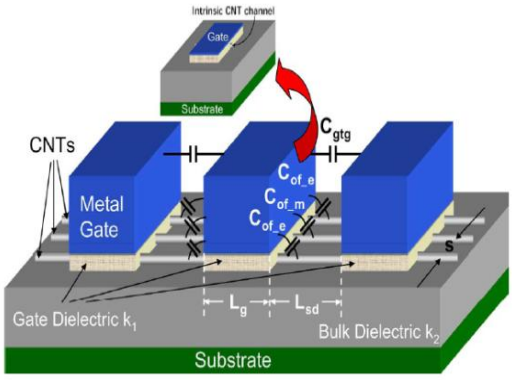
In the nanometer regime, physical factors that previously had little or no impact on circuit performance are now becoming increasingly significant. Particular examples include process variations, transistor mobility degradation, and power consumption. These new effects pose dramatic challenges to robust circuit design and system integration[2].

The rest of the paper is organized as follows. In section II comparison of simple MOS with other MOS transistor is given. Section III gives the overview of various methods used for power optimization IV gives the conclusion.

II. COMPARISON OF MOSFETS

MOSFETS are categorized in many types. Some research work has been done on these types by considering various parameters. In comparison with the MOSFETS bipolar transistors have some disadvantages such as, bipolar devices have lower input impedance, longer switching times, lower safe operating area due to second breakdown, and less efficient parallel operation due to current hogging and the need for resistors[3].

CARBON-NANOTUBE field-effect transistor (CNFET) technology has received a lot of attention in the past decadeas a promising candidate for future integrated circuits[4]. The paper analyses that in 32nm technology node, the random dopant fluctuation in a typical n-type MOSFET creates 1.1% on-current, 6.7% off-current, 0.23%input capacitance, and 1.6% threshold voltage variations, while the CNT density variation in a typical n-type CNFET with 10 CNTs in the channel creates 23% on-current, 22% off-current, 23% gate capacitance and only 0.011% threshold voltage variations. Based on this analysis, it is observed that although the threshold voltage variation in CNFET is very small, the overall variations in CNFETs are worse than the variations in MOSFETs.



FinFET devices promise to replace traditional MOSFETs because of superior ability in controlling leakage and minimizing short channel effects while delivering a strong drive current.In this paper gate sizing of finFET devices, and the paper provide a comparison with 32nm bulk CMOS. Wider finFET devices are built utilizing multiple parallel fins between the source and drain.

Independentgating of the finFET's double gates allows significantreduction in leakage current. We perform temperature-aware circuit optimization by modeling delay using temperature-dependent parameters, and by imposing constraints that limit the maximum allowable number of parallel fins. The work shows that finFET circuits are superior in performance and produce less static power when compared to 32nm circuits[5].

III. METHODOLOGIES USED

A. Algorithms Used

As the technology shrinks to nano-scale, CMOS transistors pose more challenges to circuit design. The CMOS technology scales down towards nanoscale dimensions, there are increasing transistor reliability challenges which impact the lifetime of integrated circuits. These issues are known as aging effects, which result in degradation of the performance of circuits. (Milana Ram San Francisco, California 2010).

Mixed Integer Linear Programming (MILP) –

Subthreshold circuits offer a promising solution for implementing highly energy-constrained systems for remote or mobile applications. When we scale the power supply voltage (Vdd) below the device threshold voltage (Vth), the subthreshold current ever so slowly charges and discharges nodes for the circuit's logic function[6]. This paper presents a method for minimum energy digital CMOS circuit design using dual subthreshold supply voltages. Stringent energy budget and moderate speed requirements of some ultra low power systems may not be best satisfied just by scaling a single supplyvoltage. Optimized circuits with dual supply voltages provide an opportunity to resolve these demands. The delay penalty of a traditional level converter is unacceptably high when the voltages are in the subthreshold range. Dual Voltage Design and Level Converters in Subthreshold Regime.

In this algorithm, design of minimum energy circuits with dual Vdd assignments without ALCs using mixed integer linear programing (MILP) [6]. Multiple logic-level logic gates eliminate the use of ALCs and allow VDDL gates to drive VDDH gates with affordable overheads in terms of delay and leakage power in a combinational circuit. First, the performance requirement (critical path delay Tc) of a system is given. Therefore, VDDH is determined to satisfy the system speed (or clock cycle time). The MILP automatically assigns the predetermined VDDH to gates on critical paths to maintain the performance and finds optimalVDDL for gates on non-critical paths to reduce the total energy consumption (i.e., minimum energy per cycle) by a global optimization. Inherently, CVS [8]and ECVS[9] are heuristic algorithms that tend to be non-optimal, because of the backward traversal from primary outputs through gates with time slack for assigning lower supply voltage VDDL.

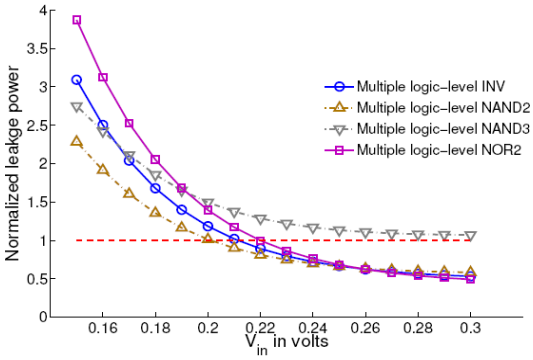


Fig.1 Multiple logic-level gate leakage power normalized to a standard INV in PTM 90nm CMOS

Power gating is one of the most effective ways to save leakage for a circuit. In this paper, using Hspice simulations in a 32nm predictive technology, the power dissipation of the design is compared with the power gated ISCAS85 benchmark circuits in both active mode and standby mode. The active power for benchmark circuits are measured with random digital input generated by Matlab and with power gating transistor on, whereas the standby powers are measured with digital input all "O"s and with power gating transistor off. The power of the design is based on N=20, R =20, and it may slightly vary depending on design specifications.

N: number of original power gating blocks
R: number of redundant power gating blocks

Clustered Voltage Scaling (CVS) –

The basic ideais to provide two different supply voltages: V_{DDL}(the reduced voltage) and V_{DDH} (the original voltage). Circuits with excessive slack are made to operate at V_{DDL}, while those along the critical paths are made to operate at V_{DDH}. As shown in fig.2 if the output of a circuit operating at $V_{DDL}$is connected directly to the input of a circuit operating at V_{DDH}, the static current flows in the V_{DDH} circuit at the input level "high". Since the voltage of the node N1 is not raised higher than V_{DDL} even at "HIGH"level[8].

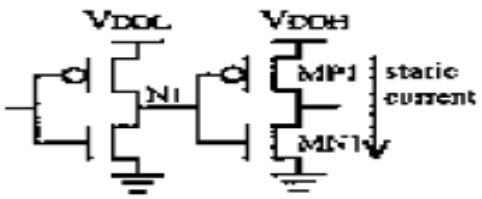


Fig.2 Direct Connection of V_{DDL} circuit and V_{DDH} circuits

Extended Clustered Voltage Scaling (ECVS) –

In CVS, the cells driven by each power supply aregrouped ('clustered') together and level conversion is needed only

at sequential element outputs (referred to as '*synchronous levelconversion*'). In ECVS, the cell assignment is flexible, allowinglevel conversion anywhere (not just at the sequential elementoutputs) in the circuit. This is referred to as '*asynchronous levelconversion*'. Since ECVS allows more freedom in VDDassignment, it has been suggested that it potentially providesgreater power reductions than CVS [3]. However there has beenno direct comparison between CVS and ECVS. In addition,nearly all subsequent work on dual-VDD synthesis has focused on CVS. In this work we demonstrate that ECVS is indeed far superior to CVS for a range of benchmark circuits in a 0.13µmCMOS technology[9].

Figure 3 depictsthe nature of the final topologies attained by CVS and ECVSwhen applied to a given circuit. From this figure, it is observed thatCVS partitions a circuit into two clusters – one having onlyVDDH cells and the other having only VDDL cells. The scenarioin which a VDDL driven cell directly feeds a VDDH driven cells clearly precluded in this partitioning. Whereas, ECVS
allows interspersing of VDDL and VDDH cells with insertion ofany required ALCs.

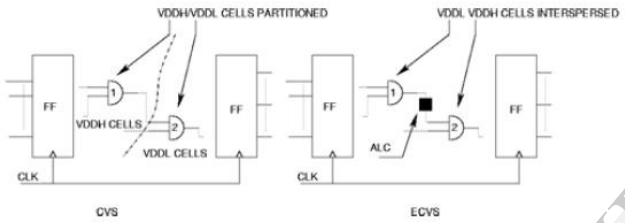


Fig.3 Circuit Structure after application of CVS and ECVS
Ultra Dynamic Voltage Scaling (UDVS) –

This paper describes a90-nm test chip that demonstrates the proposed concept of localvoltage dithering (LVD) and couples LVD with sub-threshold operation to achieve ultra-dynamic voltage scaling (UDVS). Author proposed local voltage dithering (LVD) to improve upon chip-wide voltage dithering. This section discusses the advantagesof voltage dithering at the local level and describes atest chip that demonstrates these improvements[10].

Fig. 4 illustrates the savings that LVD provides for the adder block on the test chip when the rate varies. The dotted line shows operation at the highest rate followed by ideal shutdown. The solid line shows the measured energy versus rate for DVS assuming continuous voltage and frequency scaling. Selecting two rates from the curve, 1 and 0.5 in the figure, and operating for the correct fraction of time at each rate results in the dashed line that connects the quantized points.

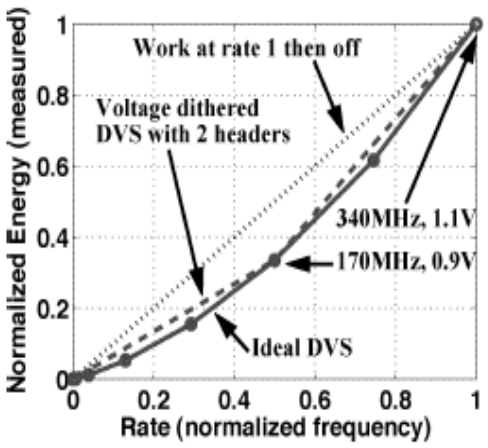


Fig.4Characterized Local Voltage Dithering

Since LVD works well for high-speed operation and operating at the minimum energy point is optimal for low performance situations, author propose ultra-dynamic voltagescaling (UDVS) using local power switches[11]. This approachuses local headers to perform LVD when high performance is necessary and selects a low voltage for sub-threshold operationat the minimum energy point whenever performance is not critical. Fig. 5 provides one example of measured UDVS characteristics for the adder.

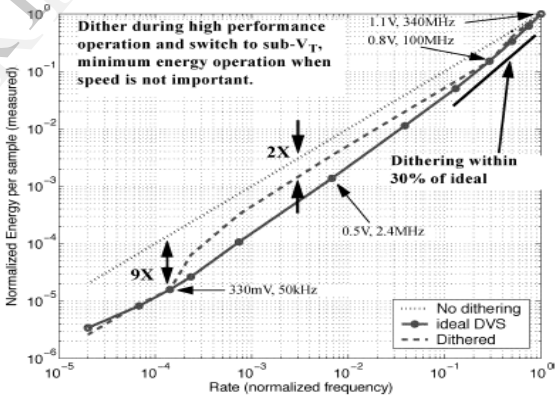


Fig.5 Ultra Dynamic Voltage Scaling With Two Headers

V. CONCLUSION

In designing of CMOS for reduction of power at different technological level work has been carried out with many methods such as Clustered Voltage Scaling, Mixed Intger Linear program.

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