

IJERT

ISSN : 2278-0181

International Journal of Engineering Research & Technology

Publish & Find Papers @



www.ijert.org

 **BROWSE**

OPEN  ACCESS

Call for Papers

Measure Delay Time When Changing the States of Ethernet Ports for Openflow Switch

Hoang Vu Tran
The University of Danang
University of Technology and Education,
Vietnam

Abstract- Currently, there are many ways to save energy for the switch such as turn off ports, change the operating modes for the Ethernet ports when there is no traffic flowing through the ports. The Ethernet ports will be turned on or be changed the operating modes with the speed higher when traffic flows pass through it. However, the changes of the states of the Ethernet ports will create DELAY-TIME. If we know DELAY-TIME, then we will make routing algorithms and get appropriately mechanisms to ensure no impact on the transmission of data and loss packets. In this paper, the author propose a method to measure DELAY-TIME when changes the operating states of the ports of OpenFlow switch based on NetFPGA platform.

Keywords—OpenFlow Switch; NetFPGA; Delay Time; Data Center Network; Green Networking.

I. INTRODUCTION

The rise of cloud computing applications and the traffic increase on the Internet network as well as data centers in recent years, the consuming energy to operate the core network infrastructure and data center systems also significantly increased. In [1], the energy consumption of British Telecom companies in 2008 was 2.6 TWh; accounting for 0.7% of the consumed energy in the UK and is the source of energy consumption Britain's biggest single. Similarly, the consumed energy by Deutsche Telekom, the telecommunications service provider Germany's largest, in 2007 was 3TWh. In the study by Baliga et al. [2], the energy consumption of the global Internet will increase dramatically in the near future (2010-2020) with a growth rate greater than the growth rate of power supply worldwide.

Besides, the current data center is designed to withstand the load at peak hours, when traffic reaches the maximum value. However, in the remaining period on normal network traffic is much lower than the maximum capacity. On the other hand, the current network equipment is designed to operate at full load all the time. Moreover, the energy consumption of a router at different load values typically differ quite a few, that is, the energy consumption on the network is hardly dependent on the load. This leads to the energy performance of network devices currently quite low. According to a study by Neilson [3], within 18 months of a capacity increase of about 2.5 times routing, network traffic on the Internet increased by 2 times, while the energy savings of the router increased only 1.65 times. It can be seen that the network devices are in use today generally not really save energy. With the rapid increase of traffic on the network energy consumption will surge the Internet.

Currently, there are several existing solutions to upgrade the energy efficiency of the network such as reduce the clock rate from 125 MHz to 62.5 MHz by changing the value of a hardware register according to input bit rate [4]. Another method reduces the operating frequency of the switch to lower levels from 125MHz to 3.096MHz following size of queue [5]. In addition, in [6] gives a different approach that changed the link rate on the ports (1GB/100Mb/10Mb) according to the queue length by reducing the frequency of Ethernet MAC to 25MHz.

However, the results in [4],[5] và [6] do not evaluate Delay Time when we change the states of Ethernet ports for Openflow Switch. Therefore, in this paper, the author presents a solution to measure Delay Time for Openflow Switch when changing the Ethernet port states and build the test-bed system for the experiments.

The main contributions of my work are the following:

- The solutions to change the states of Ethernet ports to save power consumption when there is no traffic flowing through the ports.
- The author proposes the remedy to measure the delay time for Openflow Switch when changing the Ethernet ports states.
- The author designs the test-bed system and measure the delay time when we change the states of Openflow Switch.

The rest of the paper is organized as follows. Section II describes related works. Section III presents the measurement of delay time for Openflow Switch. Section IV describes test-bed system and experimental results. Conclusions are drawn in section V.

II. RELATED WORKS

A. Openflow Switch

OpenFlow protocol is an open and standardized protocol for the network controller communicating with the switch [7]. In a classical router or switch, the fast packet forwarding (data path) and the high level routing decisions (control path) occur on the same device. An OpenFlow Switch separates these two functions. The data path portion still resides on the switch, while high-level routing decisions perform at a separate controller (Fig.1). The OpenFlow Switch and Controller communicate via the OpenFlow protocol, which defines messages, such as packet-received, send-packet-out, modify-forwarding-table, and get-stats.

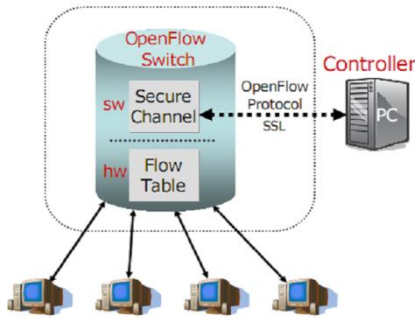


Figure 1. OpenFlow Switch structure

B. NetFPGA System

An OpenFlow Switch currently has two main parts, which are software portion on Linux OS (i.e. Centos), and hardware portion on a NetFPGA-1G Board as Fig.2.

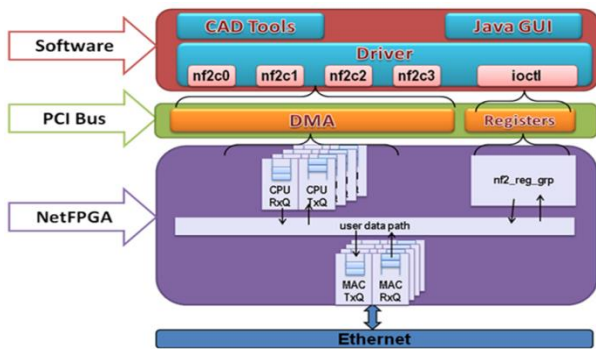


Figure 2. Diagram of the NetFPGA system

The former contains driver for OpenFlow Switch, and this part directly communicate to OpenFlow controller, such as NOX, POX. Software running on PC connects to Controller over a secured channel, on which all control messages go with defined OpenFlow protocol. This part is called as control-flow line. There is no data-flow carried or mixed on this secured channel.

The latter (data-flow section) is a NetFPGA-1G board containing a FPGA using Xilinx Virtex-II Pro 50 and four Gigabit Ethernet ports controlled by a shared Broadcom BCM5464 Network IC [8]. This part is configured as a packet-forwarding machine: communicating with the software portion on its host PC via a PCI slot, getting routing information, updating routing table and forwarding all packets from inputs to target outputs.

C. The solutions to change the states of Ethernet ports

In the paper [9], the author proposed the method to change the states of Ethernet port of Openflow Switch by turning on/off or changing three port states including 10Mbps, 100Mbps, 1Gbps. The author used MII Register to controller turn on/off ports, and set them to run at various bandwidth levels. (Fig.3)

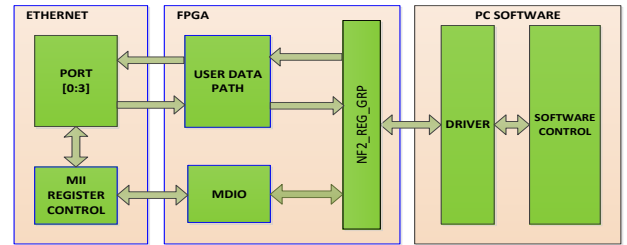


Figure 3. Diagram of the NetFPGA system

OpenFlow messages are sent between Controller and OpenFlow switches for managing, controlling them through OpenFlow channel.

- OFPT_PORT_MOD message:

Type of message: Controller to Switch

Length: 32 Bytes

Functions: Configure bandwidth of port on Switch.

Structure:

```
struct ofp_port_mod {
    struct ofp_header header;
    uint16_t port_no;
    uint8_t hw_addr[OF_ETH_ALEN];
    uint32_t config;
    uint32_t mask;
    uint8_t link_state;
    uint32_t advertise;
    uint8_t pad[3];
};
```

The *link_state* field stores the information to configure the port as shown in Fig.4. A value '1' in the flag bit will instruct the port to change its state. While {P₁, P₀} indicates port number, {B₁, B₀} is bandwidth of that port: "11" means port is running at 1Gbps, "10" means port is running at 100Mbps, "01" means port is running at 10Mbps, and "00" means port is on idle state.

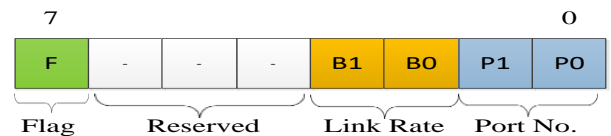


Figure 4. Link state field

III. DELAY-TIME MEASUREMENT FOR OPENFLOW SWITCH

In this section, the author presents the method to measure Delay Time of turning on the Ethernet ports or changing the Ethernet port states as 10Mbps, 100Mbps and 1Gbps.

A. Delay-Time Measurement Method

Delay time of turning on the Ethernet ports or changing the Ethernet port states as 10Mbps, 100Mbps and 1Gbps is defined from the time when the switch receives OpenFlow Switch control messages to turning on Ethernet ports to the time when data packets are transferred.

To verify the time when data packets are transferred through switches, the author found out the signal gmii_rx_dv at rgmii_io block [10]. In [10] gmii_rx_dv (Receive Data Valid) is driven by the PHY to indicate the PHY is presenting recovered and decoded data on the RXD (7:0). It is asserted during the entire data frame, and so provides an envelope signal for a valid data frame. When rx_dv = 1 the data frame pass through the Ethernet port, and rx_dv = 0 when port is turned off.

- Measure Delay Time of turning on Ethernet ports (DTTP)

To measure delay time when we turn on Ethernet ports, two counters are built, a counter is activated before turning on the Ethernet port, and a counter is activated after turning on the Ethernet port. Delay Time is the average value of two counters. The counters will be stopped if the signal rx_dv = 1. (Fig. 5)

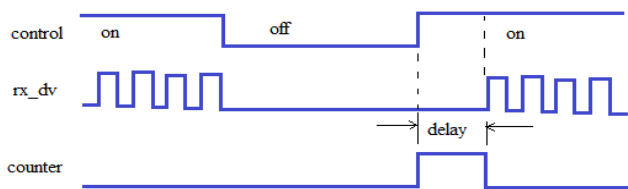


Figure 5. Measure DTTP

- Measure Delay Time of changing Ethernet port states(DTCP)

To measure the delay time of changing the Ethernet port states between 10Mbps, 100Mbps and 1Gbps, a counter is also built. However, rx_dv = 0 when the port is turned off while rx_dv = 1 at several times when it operates at 10Mbps or 100Mbps. Therefore, the parameter **-window** is defined with the condition as below:

$$\text{Maximum (IPG)} < \text{window} < \text{DTCP} \quad (1)$$

In which:

IPG: interpacket gap is the time between transmissions of Ethernet packets.

When Ethernet port state is changed between 10Mbps, 100Mbps and 1Gbps, if IPG = window then a counter will be activated until rx_dv = 1. (Fig. 6)

Hence,

$$\text{DTCP} = \text{window} + \text{counter} \quad (2)$$

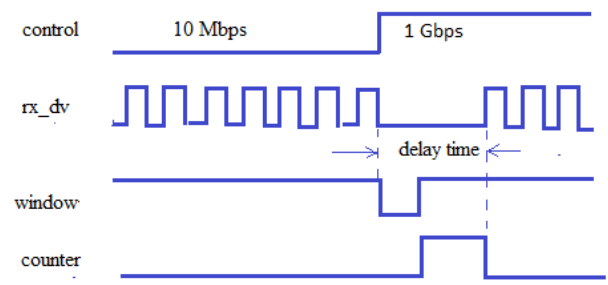


Figure 6. Measure DTCP

To write and read the value of registers, the author uses two functions Read_Reg and Write_Reg as Table 1.

Table 1: Read and Write function for registers

Function	Structure	Describe
READ_REG	int readReg (nf2device *nf2, unsigned int addr, unsigned int *val)	Read value of register in addr address and save this value in val register.
WRITE_REG	int writeReg (nf2device *nf2, unsigned int addr, unsigned int val)	Write value val to register at addr address.

IV. EXPERIMENTAL RESULTS

A. Test-bed system for measurement.

In order to measure DTTP and DTCP, a hardware test-bed is built as in the Fig.7 and Fig. 8.

- PC1: Generate packets to OpenFlow Switch.
- PC2: Control the change of Ethernet port state and measure the delay time.
- OpenFlow switch version 1.0.0.4 based on NetFPGA version 3.0.1 developed by Stanford is used.

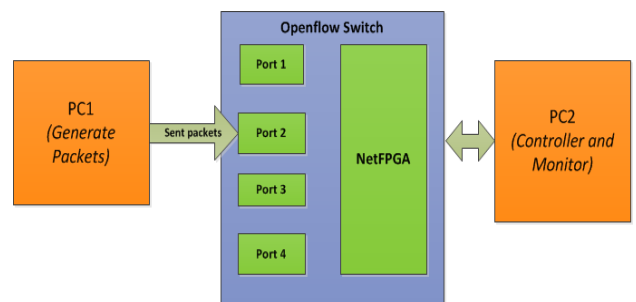


Figure 7. Test-bed system for measurement.



Figure 8. Real test system for measurement.

Configure the registers to measure DTTP

```
regwrite 0x440000 0x0900 # Turn off port 0
regwrite 0x2001100 0xFF # Reset all counter
regwrite 0x2001100 0xAA # Enable Portx counter 0
regwrite 0x440000 0x1140 # Turn on port 0
regwrite 0x2001100 0x00 # Enable Portx counter 1 and 0
# Read counter
regwrite 0x2001104 0 # Select Port0 counter 0
regwrite 0x2001104 1 # Select Port0 counter 1
```

Configure the registers to measure DTCP

```
regwrite 0x2001100 0x0000F0FF # Reset all counter
regwrite 0x2001100 0xFFFF0000 # Start counter with window filter = 65535 period
regwrite 0x440000 0x2100 # Change to 1Gbps port 0
# Read counter
regwrite 0x2001104 8 # Select Port0 counter down time
regread 0x2001110 # Read low DWORD
regread 0x2001114 # Read high DWORD
```

B. Measuremental Results

• Measure DTTP

The author measured 10 times when waking up the Ethernet port and the results are shown in the Table 2.

Table 2: Measure DTTP

Time	Counter 1(s)	Counter 2 (s)
1	1.7773	1.7761
2	1.8811	1.7793
3	1.8504	1.8789
4	1.7196	1.7279
5	1.7743	1.792
6	1.8605	1.8589
7	1.732	1.7309
8	1.8443	1.843
9	1.796	1.7959
10	1.7341	1.7327
Average	1.79696	1.79156

Average DTWP = 1.79426

• Measure DTCP

In this experiment, we measured 5 times when changing the Ethernet port states between 10Mbps, 100 Mbps and 1Gbps including 10Mbps -> 1Gbps, 100Mbps -> 1Gbps, 1Gbps -> 10Mbps and 1Gbps -> 100Mbps. The experimental results are shown in the Table 3.

Table 3: Measure DTCP

Time	10M - 1000M	100M - 1000M	1000M- 10M	1000M- 100M
1	1.7503	1.6954	1.5183	1.3019
2	1.7012	1.7091	1.531	1.3279
3	1.7242	1.7161	1.5404	1.3118
4	1.7239	1.7312	1.4731	1.3741
5	1.7406	1.7264	1.5816	1.3643
Average DTCP	1.72804	1.71564	1.52888	1.336

• Evaluation

From Table. 2, we can see that DTTP is about 1.8 second. And Table.3 shows that the maximum of DTCP is approximate 1.73 second when we change from 10Mbps -> 1Gbps while the minimum of DTCP is around 1.34 second when we switch from 1Gbps -> 100Mbps

C. Error Evaluation

There are several errors in our experiment including:

- Errors due to writing registers. To reduce this error, the author designed two counters to capture the delay time. This error is about 1.5 ms.
- Error due to counter: This error is around 1 clock, approximately 8 ns, which is very low.
- Error due to the time which rx_dv = 0. This error is the interpacket gap (IPG). To reduce this error, the author increased the transmission speed from PC1 to the switch. In the experiment, the author generated packets with the transmission speed is 234962 packets per second, about 4.25 us.

D. Proposed solution in the Future

In the future, my group will implement this solution to measure and evaluate delay time for Openflow Switch based on NetFPGA-10G [11]. The 10G NetFPGA platform provides 4 x 10 Gigabit Ethernet SFP+ interfaces which are operated by AEL2005 PHYs, and two Samtec expansion connectors which are operated by 20 GTX dual transceivers. The PHYs are connected to a Xilinx Virtex-5 TX240T and communicate to XGMAC cores on the FPGA in full duplex mode. (Fig 9)



Figure 9. NetFPGA-10G

V. CONCLUSIONS AND FUTURE WORK

In this paper, the author proposed the solution to measure the delay time for Openflow Switch when we change the states of Ethernet ports. The author also built the test-bed system and measured the delay time – DTTP and DTCP. These delay times are approximately from 1.3 to 1.8 second. The time is to configure PHY blocks as Setup PII, Auto-MDIX or Auto Negotiation.

In the future, the author will research and propose remedies to improve delay time for Openflow Switch when changing the Ethernet port states.

REFERENCES

- [1] Raffaele Bolla et al., "Energy Efficiency in the Future Internet: A Survey of Existing Approaches and Trends in Energy-Aware Fixed Network Infrastructures", IEEE Communications Survey and Tutorials, Second Quarter 2011
- [2] J. Baliga, R. W. A. Ayre, K. Hinton, R.S. Tucker, "Green Cloud Computing: Balancing Energy in Processing, Storage, and Transport," Proc. IEEE, vol. 99, no. 1, pp. 149-167, Jan. 2011
- [3] Neilson, D.T., "Photonics for switching and routing," IEEE Journal of Selected Topics in Quantum Electronics (JSTQE), vol. 12, no. 4, pp. 669-678, July-Aug. 2006
- [4] Lombardo, A., Panarello, C., Reforgiato, D., Schembra, G., "Power control and management in the NetFPGA Gigabit Router", Conf. FutureNetw, Berlin, p.1-8, July, 2012.
- [5] Wei Meng, Yi Wang, Chengchen Hu, Keqiang He, Jun Li and Bin Liu "Greening the Internet using Multi-Frequency Scaling Scheme" in 26th IEEE International Conference on Advanced Information Networking and Applications, 2012.
- [6] Y. S. Hanay, W. Li, R. Tessier, and T. Wolf, "Saving Energy and Improving TCP Throughput with Rate Adaptation in Ethernet", in IEEE International Conference on Communications (ICC), Ottawa, Canada, June 2012
- [7] "OpenFlow Switch Specification Version 1.1.0 Implemented (Wire Protocol 0x02)", February 28, 2011.
- [8] "NetFPGA-1G-CML™ Board Reference Manual "Revised January 28, 2014
- [9] T.H.Vu, P.N.Nam, "Research testbed system and new method to save energy for OpenFlow Switch" Journal of Science and Technology, The University of Danang, Vol. 1, No. 6 (79), pp.81-85, 2014
- [10] Dongwook Kim "Gigabit Media Independent Interface – Gigabit Ethernet Network" February, 28 2014.
- [11] http://netfpga.org/10G_specs.html