

MCML: Design and analysis of CMOS Invertor and MCML Invertor

Shankar Kumar Vijay¹

¹ Department of Electronics & Communication Engineering,
Ganga Institute of Technology and Management,
Kablana, Jhajjar, Haryana, INDIA

Abstract — In this paper, a new D-latch topology has been implemented in MOS Current Mode Logic (MCML) that works on lower supply voltage than the D-latch topology already implemented in MCML. The already implemented D-latch topology is called Traditional D-Latch Topology and the new D-latch topology that works on lower voltage is called low-voltage D-Latch Topology. Power consumed by MCML circuit is directly related to the supply voltage given to the circuit. For a particular amount of current drawn from the power supply, if supply voltage increases then power consumption of the circuit also increases and vice versa. Thus, the low-voltage D-latch topology consumes lesser power than the traditional D-latch topology.

Keywords- MCML, D-latch, VLSI, Low Power, MOSFET, Tiraditional D-latch.

I. INTRODUCTION

The demand for electronic circuits with extremely low supply voltages and power consumption is important in development of microelectronic technologies. In many applications, additional requirements appear, particularly the extreme speed or the accuracy of signal processing. Simultaneous fulfilment of the above demands is problematic. In the last two decades, the evolution of modern applications of analog signal processing has followed the trends of so-called current mode, where signals, representing the information, are in the form of electric currents. In contrast to the conventional voltage mode, which utilizes electric voltages, the current mode circuits can exhibit under certain conditions among other things higher bandwidth and better signal linearity. The current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage mode circuits due to their potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed [1]. The continued growth of market of mobile and satellite communication as well as multiple optical fiber system, demands for the implementation of high performance MCML circuit. In many applications, the D-latch gate is the basic circuit used to implement a number of fundamental blocks, whose performance strongly depends on D-latch gate performance.

The traditional implementation of MCML D-latch is based on stacked source-coupled pairs of MOSFETs. To keep its speed performance as high as possible, transistor operation

in the saturation region has to be ensured by using a high enough supply voltage according to the number of stacked MOSFET. In addition, a high bias current must be used to improve the speed performance, thereby determining a high static power dissipation that reduces the battery life time in portable devices and limits the feasibility of complex circuits [2].

MCML D-latch topology has been developed to reduce the supply voltage by decreasing the number of stacked MOSFET. This topology will be accordingly referred as the low voltage topology. The interest in MOS current-mode logic (MCML) is increasing because of its ability to dissipate less power than conventional CMOS circuits at high frequencies, while providing an analog friendly environment. It is used as a technique for obtaining low power mobile wireless systems operating in GHz range. MCML is a logic style for high speed, low power circuits. This type of logic was 1st implemented using bipolar transistors and extended for application with MOS transistors. MCML circuits with constant bias current are intended for accurate high-speed mixed signal application [3]. MCML dissipates constant static power and requires techniques more analogous to analog design. However, MCML requires smaller dynamic power than that of the conventional logic because of the smaller output swings. MCML seems to be promising in both reducing power consumption and providing an analog friendly environment. The reduced output swing and a faster switching makes MCML a promising candidate for certain mixed-signal applications. The constant supply currents, lower cross talk between analog and digital circuits of MCML improve the accuracy of mixed-mode systems.

II. BASIC CONCEPT OF MCML

MCML in general consists of three main components, as shown in the Fig 2.1, which includes the pull-up load, the pull-down network (PDN) and a constant current source.

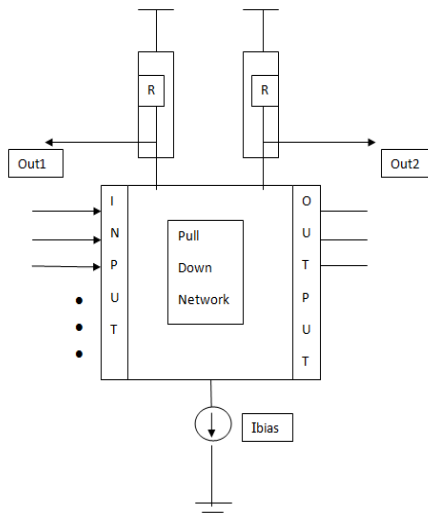


Fig. 1: Basic blocks of MCML

MCML is a completely differential logic, i.e. all signals and their complements are required. Depending on the logic implemented by PDN, all the current flows through one of the two branches, providing complementary output signals. Voltage at the output of branch with no current reaches VDD, whereas for the other branch some voltage drops across the load, resistor and the output voltage becomes $VDD - I_{bias} \cdot R_L$. Due to the reduced swing, it has smaller dynamic power dissipation.

MCML circuits are faster than other logic families, because it uses NMOS transistors only. Due to its differential nature, it is highly immune to common mode noise. It has almost flat power curve over a wide range of frequency as opposed to other logic styles where power consumption increases directly with frequency. Therefore at very high frequencies its power consumption is comparable or lower than other logic styles. This makes it a good choice for high speed and low power integrated circuit design

III. COMPARISON BETWEEN CMOS AND MCML CODE

Till recently, CMOS technology was being used extensively to implement digital circuits. CMOS has the advantage that its static power consumption is extremely less. It uses power only when charging and discharging. That is, dynamic power consumption of CMOS logic is considerable.

Now a day's frequency of operation of the digital circuit is increasing day by day. With the increase in frequency, dynamic power consumption of CMOS circuit increases considerably. Hence at higher frequency of operation, power consumption of CMOS circuits is substantial. Another problem with CMOS logic is that its operation is relatively slow

IV. INVERTERS OF THE CMOS LOGIC

The data plotted there was obtained by SPICE simulations using the parameters of $0.18\mu\text{m}$ CMOS transistors with a 1.8-V supply voltage. The MCML is faster than CMOS logic because of its smaller input capacitance and smaller

signal amplitude. Because the CMOS logic uses power only when charging and discharging, its power consumption is generally less than that of the MCML. The power consumption of this CMOS logic is the product of the operation frequency and the charging and discharging power unit switching.

On the other hand, the power consumption of the MCML is the sum of the penetration currents of MN1 and MN2 in the figure, which is the same as the drain current of the current source transistor MC1. Since MC1 operates at saturation region, this drain current is mainly determined by the gate bias and the contribution of the voltage at the common-source node NC is small. Moreover, the operation frequency has little effect on the voltage at NC because of the power consumption of the MCML is nearly independent of the operation frequency. In the Fig.4.1 and Fig. 5.1, there are two MOSFETs in the CMOS logic and five in the MCML.

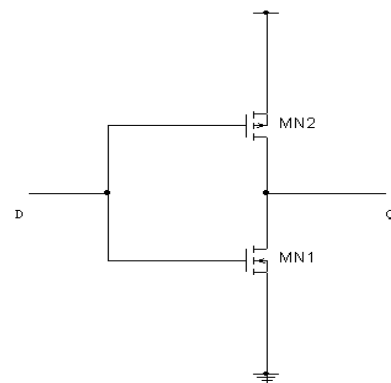


Fig.2 CMOS Inverter

V. CONVENTIONAL MCML

In addition, the MCML requires two lines for each signal. Therefore, a chip area with a given function is about two to four times larger in the MCML than in the CMOS logic.

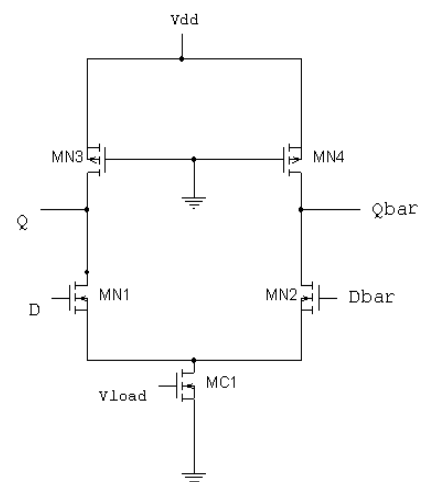


Fig.3 MCML Inverter

VI. TRADITIONAL D-LATCH

A MOS current mode logic (MCML) D-Latch consists of a source-coupled pair driven by the input CLK, that alternatively activates the transistor pair M3-M4 or M5-M6. When CLK is high, M2 is OFF, hence the bias current I_s flows through M1 and is then steered by transistors M3-M4 according to the value of input D. Being the output set by input D, the latch is said to be in the transparent state. When CLK is low, the bias current flows through transistor M2 and cross-coupled transistors M5-M6, that store the previous output value by virtue of their positive feedback connection, and the latch is in hold mode which is shown in fig.6.1

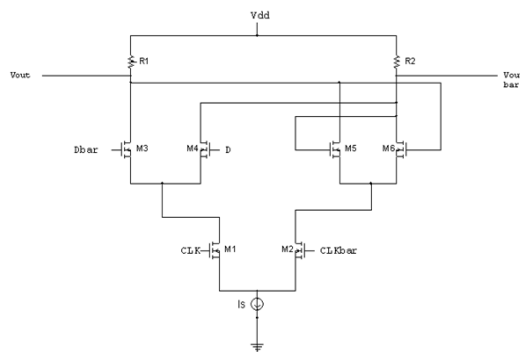


Fig. 4 Traditional D-Latch

VI. RESULT AND ANALYSIS

A. Inverters of the CMOS logic

The CMOS logic has the advantage of low power consumption, but its operation is relatively slow. For example, the maximum toggle frequency of a conventional 0.18μm CMOS inverter is only about 3.5 GHz. Simulated inverter delay time as a function of fan-out and power consumption is a function of an operation frequency for the CMOS logic and the MCML are shown in the Fig.7.1.

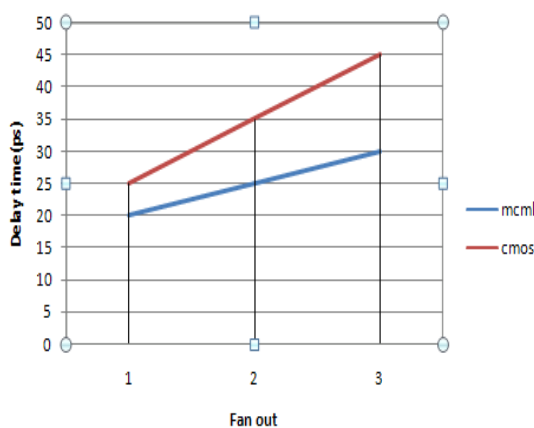


Fig 5 Delay Vs Fan out of MCML and CMOS inverter

The data plotted there was obtained by SPICE simulations using the parameters of 0.18μm CMOS transistors with a 1.8-V supply voltage. The MCML is faster than CMOS logic because of its smaller input capacitance and smaller

signal amplitude. The data plotted there was obtained by SPICE simulations using the parameters of 0.18μm CMOS transistors with a 1.8-V supply voltage.

B. Conventional MCML

Spice simulations were performed using the parameters of 0.18-μm CMOS transistors. However, in the gigahertz frequency range, the power consumption of the CMOS logic

becomes larger than that of the MCML, as shown in the Fig7.1[b]. From the graph it is clear that the MCML is suitable for low-power operation in the gigahertz frequency range

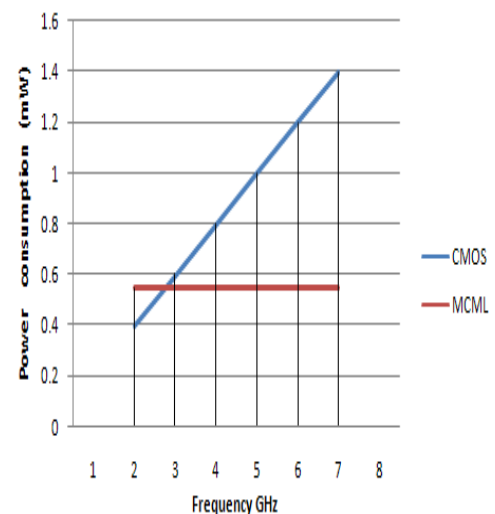


Fig. 6 Power dissipation Vs Frequency for CMOS and MCML

C. Simulation result for D-Latch

When data is high all the current passes through one branch, as a result the voltage at the drain of that transistor drops to a voltage level ($V_{DD} - I_s R_L$). As the other transistor is in cut off and no current is flowing through it, the voltage at the drain of that transistor becomes high (V_{DD}). When clock goes low, the hold pair is activated.

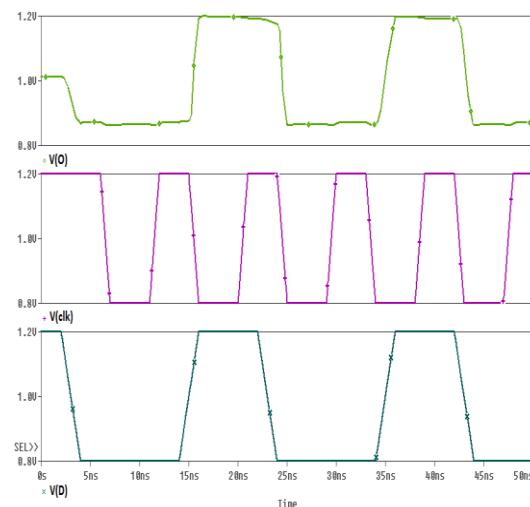


Fig. 7. Simulation result for D-Latch

VII.CONCLUSIONS

The concept of MOS current mode logic is explained in. CML logic is very useful for high frequency application because power consumption of CMOS based circuit increase in high frequency. MCML based Low Voltage D-latch topology has been developed and compared to the traditional implementation of MCML D-Latch in terms of supply voltage. It allows for a supply voltage reduction by a factor of 25 % with respect to the traditional topology, which could be exploited to achieve power savings.

REFERENCES

- [1] M. Sumathi, Kartheek, "Performance and analysis of CML Logic gates and latches" IEEE 2007 International Symposium on Microwave, Antenna, Propagation, and EMC Technologies for Wireless Communications
- [2] FERRI, G., GUERRINI, N. C. Low-voltage low-power CMOS current conveyors. London: Kluwer Academic Publishers.2003.
- [3] B. Razavi, Y. Ota, and R. G. Swartz, "Design techniques for low-voltage high-speed digital bipolar circuits," IEEE J. Solid-State Circuits, vol. 29, pp. 332–339, Mar. 1994.
- [4] Hassan, Mohab Anis, Mohamed Elmasry, "MOS Current Mode Circuits Analysis, Design" IEEE transactions on very large scale integration (vlsi) systems, vol. 13, no. 8, august 2005.
- [5] K.Kishine, Y.Kobayashi, H.Ichno, "A high speed low power by polar digital circuit for Gb/LSI: current mirror control logic",IEEE solid state ckt(1997).
- [6] M. Alioto, R. Mita, G. Palumbo, "Analysis and Comparison of Low-Voltage by CML D- Latch" 0-7803-7596-3/02,2002 IEEE
- [7] TOUMAZOU, C., LIDGEY, F.J., HAIGH, D.G. Analogue IC Design: The current mode approach. IEE Circuits and Systems Series 2, Peter Peregrinus Ltd., 1990.
- [8] M. Yamashina and H. Yamada, "An MOS current mode logic (MCML) circuit for low- power sub-GHz processors," IEICE Trans. Electron., vol. E75-C, no. 10, pp. 1181–1187, Oct. 1992.
- [9] J. Musicer and J. Rabaey, "MOS current mode logic for low power, low noise CORDIC computation in mixed-signal environments," in Proc. Int. Symp. Low Power Electronic Design (ISLPED'00), Jul. 2000, pp. 102–107.
- [10] M. Alioto and G. Palumbo, "Design strategies for source coupled logic gates," IEEE Trans. Circuits Syst. I, vol. 50, pp. 640–654, May 2003.
- [11] B. Razavi, Design of Analog CMOS Integrated Devices. New York: McGraw-Hill, 2001.
- [12] M. Alioto - G. Palumbo, "Modeling and optimized design of current mode MUX/XOR and D Flip-Flop," IEEE Trans. on CASpart II, V. 47, No.5, pp.452-461, May2004