Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 03, March-2017

# Matlab Code for LTE Convolutional Code and Viterbi Decoder

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***Abstract*—LTE system needs a powerful method for error control on the transmission channel. The error control method is based on adding parity bits to the signal data stream. These parity bits are used to detect the error in bits and also to correct them. Meanwhile, Convolution Encoding with Viterbi Decoding is a powerful method for Forward Error correction and Detection. In this paper, Matlab simulation Model as well as hardware architecture of LTE Viterbi decoder was designed with specifications according to 3GPP standard, where the code rate 1/3.**

***Keywords— LTE; Convolution Encoder; Viterbi Decoding; 3GPP.***

## I. INTRODUCTION

The goal of designer is to create a communications system that transport a message signal from a source across channel has noise to a user at the other end of the channel with the following objective: The data is delivered to the user both efficiently and reliably, submit to certain design restrictions: Permissible transmit power, available bandwidth channel, and low cost of building the system. Convolution coding is a popular error-correcting coding technique used in digital communications. A data is convoluted, and then transmitted into a noisy channel. This convolution process encodes some redundant bits into the transmitted signal, thereby improving the data capacity of the system channel. The popular method used to decode convolutional coded messages is Viterbi algorithm. The algorithm tracks down the most likely sequences the encoder went through in encoding the data, and uses this information to discover the original message.

## II. LITERATURE REVIEW

An exhaustive literature survey has been carried out related to the titled work to find out the current research. In [11], K.Cholan, introduced new method of Viterbi decoder to improve in terms of area and speed. The design is based on reconfigurable FPGA technology, by adopting parallel pipeline features of the hardware resources. The overall system performance improved in terms of area and speed. In [9], Soreng B., a Convolution Encoder and Viterbi decoder of code rate1/2, and constraint length 7 was presented. It shows a large improvement in terms of area overhead. In [10],Gohe l implemented a Viterbi decoder based on FPGA using a constraint length of 7 and a code rate of 1/2.Itshowed an improvement in the design by using trace back implementation of survivor sequence memory management for low power decoder design. In this paper an enhancement in the implementation of a soft decision Viterbi decoder on Virtex-6 FPGA XC6VLX240T is introduced to overcome problems of complex implementation and area.

## III. CONVOLUTIONAL CODES

Convolutional codes technique differ from block codes technique in that the encoder contains memory and the n encoder outputs at any time unit depend on the **k** inputs and m previous input blocks. An **(n, k, m)** convolutional code can be implemented with a **k** input, **n**-output with input memory **m**. typically, **n** and **k** are small integers with **k<n**, but the memory order **m** must be large to achieve low error probabilities. In the important special case when **k=1**, the data sequence is not divided into blocks and can be processed continuously.

A convolutional code is generated by passing the information to be transmitted through a linear limited-state shift register. In general, the shift register contains **K (k-bit)** stages and **n** linear algebraic function generators.

- **k**: number of bits shifted into the encoder at one time **k=1** is usually used!!
- **n :** number of encoder output bits corresponding to the **k** information bits
- **Rc = k/n** : code rate
- **K :** constraint length
- **m :** encoder memory
- **K = m+1**

Each encoded bit is a function of the present input bits and their past ones. [1]

## IV. VITERBI ALGORITHM

Both the algorithm and operation behind the proposed 64 state Viterbi decoder, depicted in Fig. 1, are presented [2]. When a new symbol is received, the branch metric unit calculates the Euclidean distances (ED) for all possible trellis state transitions. The encoder is flushed with zeros at the end of each frame. The decoder performs frame by frame decoding. The computation of branch metrics is based on a comparison of the current input symbol with the expected value. The path metrics are identified as letters at different nodes of the trellis [3].

The Viterbi algorithm is a maximum likelihood method to find the most probable sequence of hidden states based on a given sequence of detected outputs in Hidden Markov model. However it reduces the computational load by taking the advantage of special form in code trellis. The algorithm involves calculating a measure of distance between the

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 03, March-2017

received signal at the time t1 and the come in trellis path entering each state at time t1. The most likely path through the trellis will maximize this metric. The early refusal of the unlikely paths reduces the decoding complexity. Advantage of Viterbi algorithm is that it has self- rectification of the code, minimization of transmitting Energy, minimization of BW and very good capability to correct wrong transmitted bits, [4]

## V. TYPES OF VITERBI DECODING

The two decoding algorithms used for decoding the convolution codes are Viterbi algorithm and Sequential algorithm. The sequential decoding has an advantage that it can perform very well with long constraint length. The Viterbi decoding is the best technique for decoding the convolution codes but it is limited to smaller Constraint lengths [5].In order to realize a certain coding scheme a suitable measure of similarity or distance metric between two code words is vital. The two important metrics used to measure the distance between two code words are the Hamming distance and Euclidian distance adopted by the decoder depending on the code scheme, required accuracy, channel characteristics and demodulator type [6].

### *A. Hard Decision Viterbi Decoding:*

In hard-decision decoding, the path through the trellis is determined using the Hamming distance measure. Thus, the most favorable path through the trellis is the path with the minimum distance. The Hamming distance can be defined as a number of bits that are different between the detected symbol at the decoder and the sent symbol from the encoder. Also, the hard decision decoding applies one bit quantization on the received bits [6].

### *B. Soft-Decision Decoding:*

Soft- decision decoding is used for the maximum likelihood decoding, when the data is transmitted over the Gaussian channel. On the contrary to the hard decision the demodulator input is now an analog waveform and is usually quantized in to different levels in order to help the decoder decide more easily. Using soft- decision decoding interest is to provide decoder with more information, which decoder then use for regains the message sequences. It provides better error performance than hard-decision type. Viterbi decoding also has a performance improvement of approximately 2 dB in the required S/N ratio compared to the two level quantization processes, for a given Gaussian Channel. Disadvantage of using soft decision decoding is the increase in required memory size at the decoder and the reduced speed [4].

## VI. LTE CONVOLUTIONAL ENCODER

### *A. Downlink Physical Data and Control Channels*

Unlike the data, control information (such as is sent on the Physical Downlink Control CHannel (PDCCH) and Physical Broadcast CHannel (PBCH)) is used a convolutional code to coded, as the code blocks are significantly smaller and the additional complexity of the turbo coding operation is therefore not worthwhile.[7]

#### *a. Physical Broadcast Channel (PBCH)*

In perfect cellular systems the basic system information which allows the other channels in the cell to be configured and operated is carried by a Broadcast Channel (BCH). So the achievable coverage for reception of the BCH is crucial to the successful process of such cellular communication systems; LTE is no exception. [7]

#### *b. Physical Downlink Control Channel (PDCCH)*

A PDCCH carries a data known as Downlink Control Information (DCI), which contains resource assignments and other control information for a user equipment or group of user equipment. In general, several PDCCHs can be transmitted in a subframe. [7]

### B. Tail biting convolutional coding

#### a. convolutional encoder

A convolutional encoder (k, n, m) is composed of a shift register with m stages. At each time instant, k information bits enter the shift register and k bits in the last position of the shift register are dropped. The set of n output bits is a linear combination of the content of the shift register. The rate of the code is defined as Rc = k/n. The following Figure shows the convolutional encoder used in LTE with m = 6, n = 3, k = 1 and rate Rc = 1/3. The linear combinations are defined via n generator sequences G = $[g_0, \ldots \ldots \ldots g_{n-1}]$ where
g = $[g_{l,0}, g_{l,1} \ldots \ldots \ldots, g_{l,m}]$.
The generator sequences used in the following Figure are
g0 = [1 0 1 1 0 1 1], g1 = [1 1 1 1 0 0 1], g2 = [1 1 1 0 1 0 1]
or using octal notation
g0 = [133] (Oct), g1 = [171] (Oct), g2 = [165] (Oct). [7]

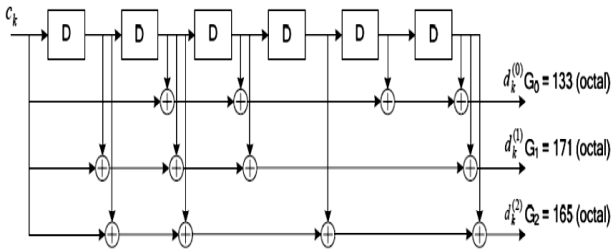


Figure.1: Rate 1/3 tail biting convolutional encoder

The convolutional coded transport channels and control information rate matching consists of interleaving the three bit streams $d_k^{(0)}$, $d_k^{(1)}$, $d_k^{(2)}$Followed by the collection of bits and the generation of a circular buffer as shown in the following Figure the output bits are transmitted as described in sub clause.[8]

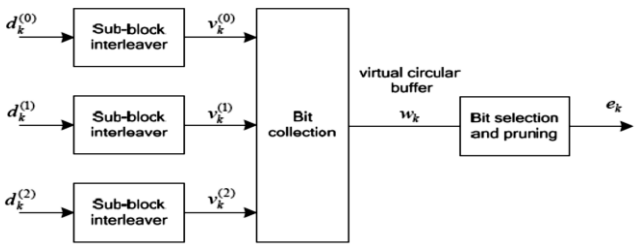


Figure.2: Rate matching for convolutionally coded transport channels and control information.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 03, March-2017

b. Sub-block interleaver

The bit stream $d_k^{(0)}$ is interleaved in accordance with the sub-block interleaver with an output sequence sort out as $v_0^{(0)}, v_1^{(0)}, v_2^{(0)}, \ldots\ldots, v_{K_{\Pi-1}}^{(0)}$

The bit stream $d_k^{(1)}$ is interleaved in accordance with the sub-block interleaver with an output sequence sort out as $v_0^{(1)}, v_1^{(1)}, v_2^{(1)}, \ldots\ldots, v_{K_{\Pi-1}}^{(1)}$

The bit stream $d_k^{(2)}$ is interleaved in accordance with the sub-block interleaver with an output sequence sort out as $v_0^{(2)}, v_1^{(2)}, v_2^{(2)}, \ldots\ldots, v_{K_{\Pi-1}}^{(2)}$ .[8]

```
%% Interleaver Part
if ( (mod(length(VtCode),96))~=0 )
    pd = zeros(1,96-mod(length(VtCode),96));
    block  = [VtCode pd];
else
    block  = VtCode;
end
```

TABLE 1: INTER-COLUMN PERMUTATION PATTERN FOR SUB-BLOCK INTERLEAVER

| Number of columns $C_{subblock}^{cc}$ | Inter-column permutation pattern $< P(0),P(1)\ldots..,P(C_{subblock}^{cc}) >$ |
|---|---|
| 32 | < 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31,0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30 > |

c. Bit collection and selection

The circular buffer of length $K_w$=3$K_\pi$ are generated as follows:

$w_k$=$v_k^{(0)}$ for $k = 0,\ldots, K_\pi - 1$

$w_{K_\pi+k}$=$v_k^{(1)}$ for $k = 0,\ldots, K_\pi - 1$

$w_{2K_\pi+k}$=$v_k^{(2)}$ for $k = 0,\ldots, K_\pi - 1$

Denoting by $E$ the output sequence length rate matching, the rate matching output bit sequence is $e_k, k = 0,1,\ldots, E-1$.[3]

```
%% BitCollection Part
bc = zeros (1,WL96);
for i=1:1:WL32
    bc (i*3 -2)  = interlever_sb1(i);
    bc (i*3 -1)  = interlever_sb2(i);
    bc (i*3   )  = interlever_sb3(i);
end
```

d. Modulation

Physical Broadcast CHannel (PBCH) and Physical Downlink Control CHannel (PDCCH) that coded with a convolutional code are used QPSK modulation. [7]

```
%% Modulation Part
TXout = zeros(1,4848);
NRZ = -2*bc + 1;
fc=1000;
fs=10000;
ts=1/fs;
nts=(0:0.1:10).*ts;
Eb=1;A=sqrt(Eb);
k=1;
for i=1:2:WL96
    Q = NRZ(i);
    I = NRZ(i+1);
    y = Q*A*sqrt(2*fs)*cos(2*pi*fc*nts) + I*A*sqrt(2*fs)*sin(2*pi*fc*nts);
%     stem(nts,y),xlabel('nts'),ylabel('y'),title('TX QPSK Wave '),grid
    TXout(k:k+100) =  y;
    k = k + 101;
end
```

e. Viterbi decoder

```
%% Branch Metric
%       BCblok;
      cd = zeros(1,3);
      t  = 1;
      BM0 = zeros(64,32);
      BM1 = zeros(64,32);
      for i = 1:3:96
          cd(1:3) = BCblok(i:i+2);
          for j = 1:1:64
              BM0(j,t) = sum( (xor( cd,OPSt0(j,1:3) )).*1 );
              BM1(j,t) = sum( (xor( cd,OPSt1(j,1:3) )).*1 );
          end
          t = t + 1;
      end
```

```
%% Path Metric

      PMa = zeros(64,33);
      PMb = zeros(64,33);
      PM  = zeros(64,33);
      for i = 2:1:33
          for j = 1:1:32
              PMa (j,i) = PM(psa(j),i-1)+BM0(psa(j),i-1);
              PMb (j,i) = PM(psb(j),i-1)+BM0(psb(j),i-1);
              PM  (j,i) = min(PMa(j,i) , PMb(j,i));
          end
          for j = 33:1:64
              PMa (j,i) = PM(psa(j),i-1)+BM1(psa(j),i-1);
              PMb (j,i) = PM(psb(j),i-1)+BM1(psb(j),i-1);
              PM  (j,i) = min(PMa(j,i) , PMb(j,i));
          end
      end
```

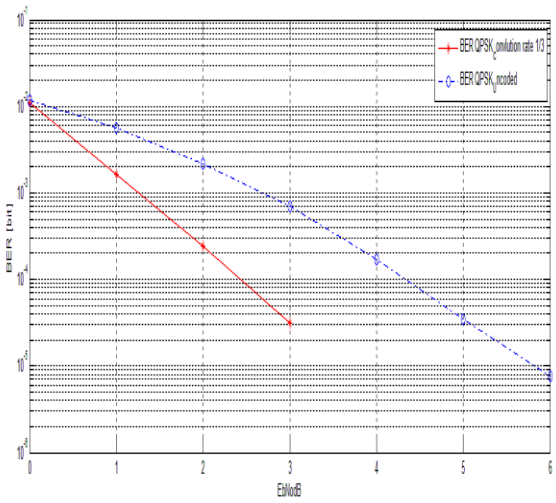


Figure 4: BER versus SNR for coding rates 1/3

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 03, March-2017

## VII. FLOW CHART OF MATLAB CODE

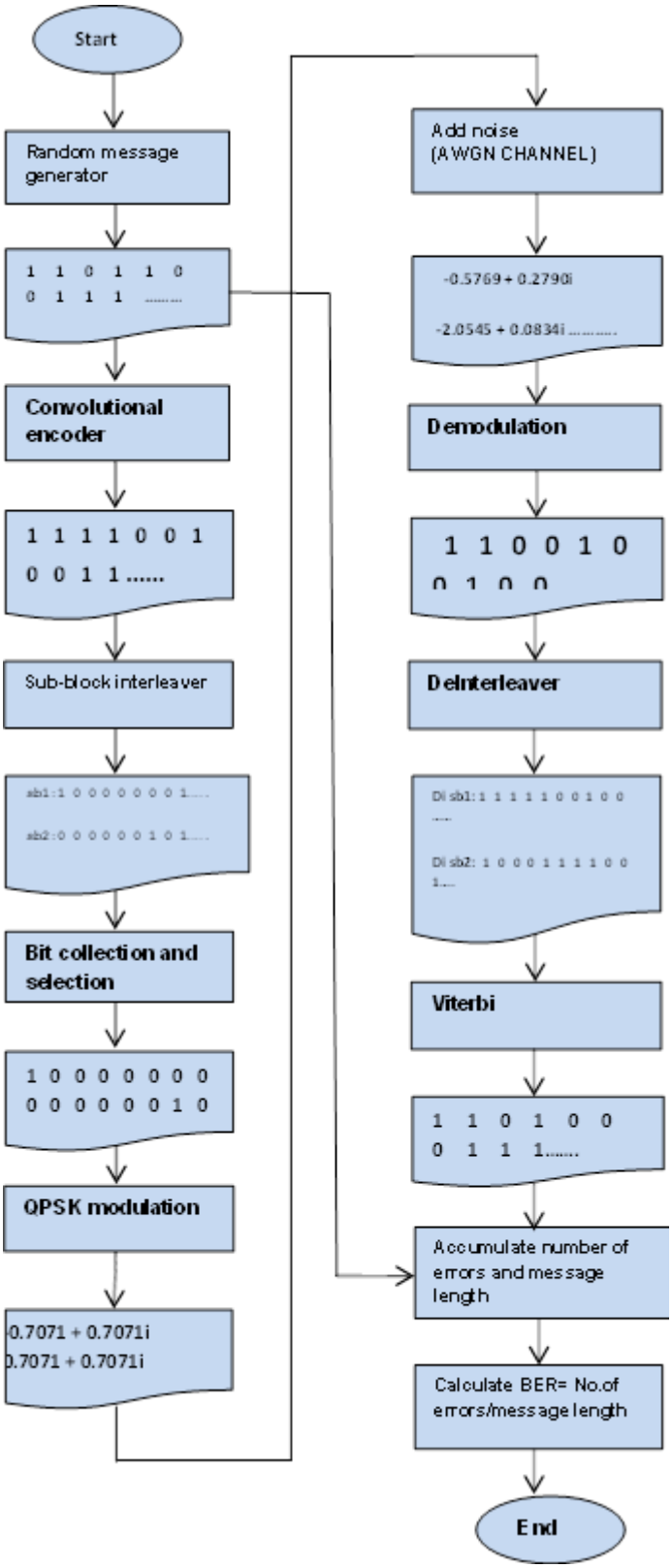


Figure.3: Flow chart of Matlab code

## VII. CONCLUSION

The performance of the Viterbi decoder can be evaluated through comparing the recovered message with the original message and calculating the bit error rate (BER) at a specific energy per bit to signal to noise ratio(SNR) according to the Formula: BER = Number of errors / total message length.

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