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LTspice-Based Analysis and RCD Clamp Implementation for Performance Improvement in a Planar Transformer Flyback Converter

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Abstract - **High-frequency flyback converters are attractive for compact isolated power supplies, yet transformer parasitics can introduce severe voltage stress on the primary switch. In planar transformers, tight geometric constraints improve repeatability and thermal behavior, but leakage inductance remains a dominant cause of drain-voltage overshoot during turn-off. This paper presents an LTspice-based study of a planar-transformer flyback converter and evaluates a series RCD clamp as a practical improvement to limit drain stress. The transformer is modeled using coupled inductors to represent magnetizing and leakage effects, and key waveforms are examined, including gate drive, drain voltage, primary current, and output voltage. Simulation results show that the RCD clamp reduces the peak drain-voltage overshoot (from the kV range down to approximately the 1.0–1.1 kV range in this design) while maintaining stable output regulation around 5 V. The presented workflow provides a rapid, reproducible approach for assessing stress-mitigation circuits in high-frequency planar flyback converters.**

Keywords: Flyback converter; planar transformer; leakage inductance; RCD clamp; LTspice; drain-voltage overshoot

I. INTRODUCTION

Flyback converters remain a preferred isolated DC–DC topology for low-to-medium power applications because they combine isolation, wide conversion ratios, and a low component count [1]. As switching frequency increases, passive components can be reduced, improving power density; however, switching transitions become more sensitive to parasitics, especially those associated with the transformer and device capacitances [2]. Planar transformers are often selected in high-frequency designs due to their low profile, predictable winding geometry, improved heat spreading, and good manufacturing repeatability [3]. Even with planar structures, leakage inductance is unavoidable and becomes a critical stress source in flyback converters: when the primary switch turns off, energy stored in leakage inductance cannot transfer to the secondary and instead produces a drain-voltage overshoot at the switching node. If unmitigated, this overshoot can exceed device ratings or force the use of higher-voltage devices with worse on-resistance, reducing efficiency and increasing cost. Several mitigation techniques exist, including RC snubbers, RCD clamps, and active clamp approaches [1], [4]. Among them, the RCD clamp is widely used in practice because it is simple, robust, and can substantially reduce peak drain stress with minimal design effort [4]. This work targets a rapid, simulation-driven evaluation suitable for thesis-to-paper conversion: a planar-transformer flyback converter is modeled in LTspice, baseline operation is verified, and an RCD clamp is added as the single explicit improvement. The contribution of the paper is twofold: (i) a clear coupled-inductor modeling approach for planar transformer behavior in LTspice, and (ii) a waveform-based comparison that quantifies drain-voltage stress reduction while confirming that output regulation remains intact.

II. SYSTEM DESCRIPTION

The simulated converter is a high-frequency flyback stage designed around a planar transformer model. The input is a 24 V DC source and the target output is approximately 5 V. A MOSFET switch is driven by a 0–10 V gate pulse (Fig. 3), storing energy in the magnetizing inductance during the on-time. During the off-time, the secondary rectifier conducts and transfers energy to the output capacitor and load. Key waveforms for validation include the switch-node/drain voltage, primary current, output startup response, and steady-state output ripple. Two configurations are analyzed: (a) baseline (no clamp), and (b) improved design with a series RCD clamp connected at the switching node to limit turn-off overshoot (Fig. 2).

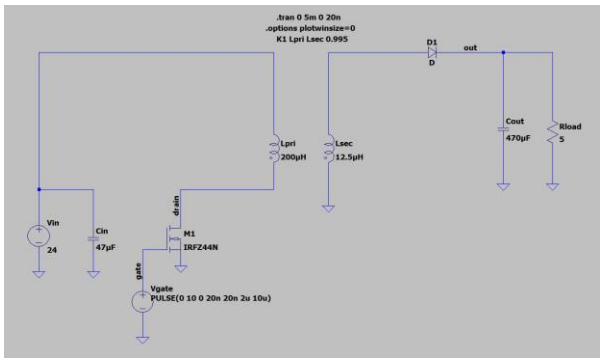

Fig. 1. Planar-transformer flyback converter (baseline, no clamp).

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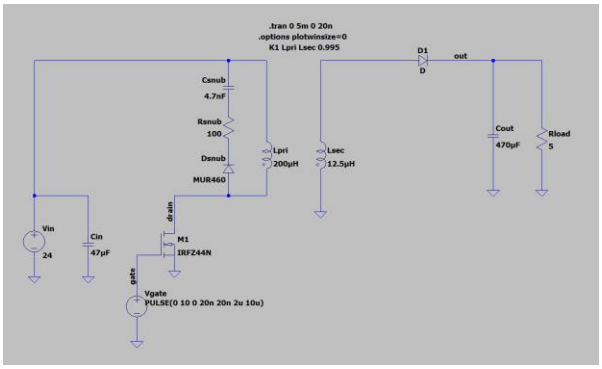

Fig. 2. Planar-transformer flyback converter with series RCD clamp at the switch node.

III. PLANAR TRANSFORMER MMODELLING

In LTspice, the planar transformer is represented using coupled inductors (Lpri and Lsec) with a coupling coefficient k close to unity to emulate tight coupling, while still allowing non-zero leakage inductance. The magnetizing inductance Lm primarily sets the energy storage per switching cycle, whereas leakage inductance Llk shapes the turn-off transient and dominates the drain-voltage spike. Using a coupled-inductor model enables fast iteration without requiring field-solver geometry extraction, which is appropriate for a simulation-focused study. Transformer dot convention is selected to maintain correct polarity: when the primary dotted terminal is driven positive during the on-time, the secondary dotted terminal becomes reverse-biased, preventing energy transfer until the switch turns off. This ensures that the rectifier conduction and output charging occur in the off-time, consistent with flyback operation.

IV. RCD CLAMP IMPLEMENTATION

The RCD clamp used in this work is a series network comprising a fast recovery diode, a capacitor, and a resistor. The diode provides a unidirectional path from the switching node into the clamp capacitor during the turn-off transient. When the MOSFET turns off, the leakage inductance current attempts to continue flowing, momentarily raising the switching-node voltage. Once the clamp diode becomes forward-biased, part of the leakage energy charges the clamp capacitor, limiting the peak drain voltage. The resistor then discharges the clamp capacitor between cycles and dissipates the captured energy as heat [4]. This mechanism trades a controlled dissipation for reduced voltage stress on the primary switch. Because the objective of this paper is a minimal-change improvement, the RCD clamp is selected rather than an active clamp, which would require additional control and components.

V. SIMULATION RESULTS

This section summarizes the principal LTspice waveforms used to validate operation and quantify the effect of the RCD clamp. Figures are presented in a sequence that follows the energy flow and stress mechanisms: gate drive, drain voltage (baseline vs. clamped), primary current, output startup, and output ripple.

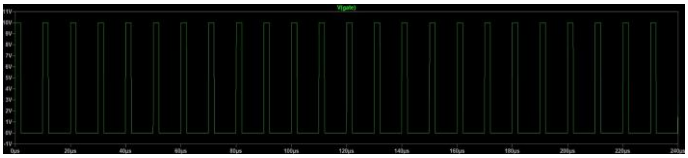

Fig. 3. Gate-drive waveform (0–10 V pulse).

The gate signal provides the switching action required for flyback operation; a clean pulse waveform confirms correct excitation of the primary switch.

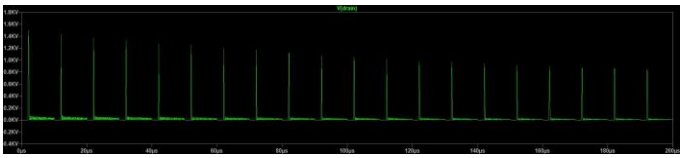

Fig. 4. Drain voltage without clamp (baseline).

Without a clamp, the drain voltage exhibits a pronounced overshoot at turn-off due to leakage inductance energy, reaching the kV range in this simulation.

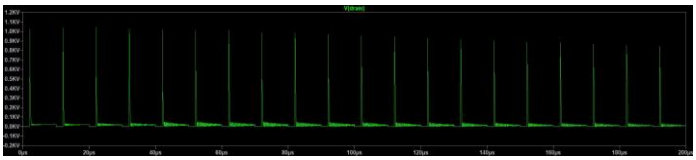

Fig. 5. Drain voltage with series RCD clamp.

With the RCD clamp, the peak overshoot is reduced (to approximately the 1.0–1.1 kV range here) while the steady-state level around the reflected output remains similar.

Fig. 6. Primary current waveform I(Lpri).

The primary current shows the expected ramp behavior during on-time (energy storage in magnetizing inductance) and a discontinuous behavior consistent with flyback transfer.

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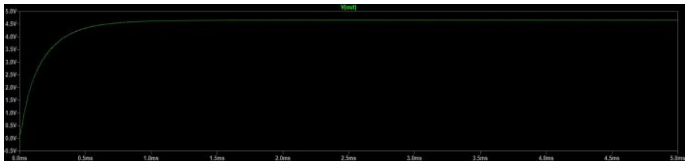

Fig. 7. Output voltage startup response.

The output voltage rises smoothly and settles to the regulated level, indicating stable energy transfer and adequate output filtering.

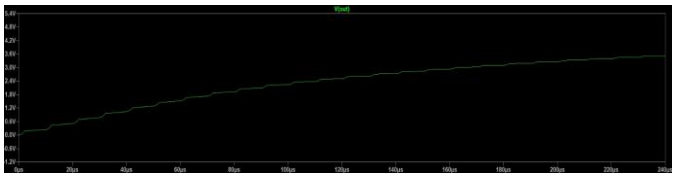

Fig. 8. Output voltage ripple in steady state.

The steady-state ripple remains small relative to the nominal 5 V output, confirming that the clamp does not degrade regulation in the simulated operating point.

A direct comparison of Fig. 4 and Fig. 5 highlights the improvement: the baseline configuration shows higher peak drain stress, whereas the clamped configuration limits the maximum voltage excursion by diverting leakage energy into the RCD network. In both cases, output regulation is maintained (Fig. 7–Fig. 8), indicating that the clamp primarily affects the turn-off transient rather than the average energy transfer.

VI. DISCUSSION

The simulations demonstrate that leakage-inductance-induced overshoot can dominate device stress in high-frequency flyback converters, even when planar transformer structures are used. The RCD clamp reduces this stress by providing a controlled path for leakage energy, which improves robustness at the expense of additional dissipation in the clamp resistor. In practical designs, the clamp component values are chosen to balance peak-voltage reduction and power loss; the LTspice workflow used here enables rapid value sweeps before hardware implementation. Although active clamp solutions can further recover energy and improve efficiency, their additional complexity is not always justified for time-constrained or cost-sensitive designs. Therefore, the RCD clamp remains a practical first improvement for limiting drain-voltage stress in planar flyback converters.

VII. CONCLUSION

An LTspice-based study of a planar-transformer flyback converter was presented, with a focus on reducing drain-voltage overshoot caused by transformer leakage inductance. A series RCD clamp was implemented as a minimal-change improvement and shown to reduce peak drain stress (from the baseline kV-level overshoot to approximately the 1.0–1.1 kV range in the simulated case) while preserving output regulation near 5 V. The proposed modeling and evaluation flow is suitable for rapid converter development and provides a clear basis for selecting stress-mitigation circuits in high-frequency planar flyback designs.

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