# LSSR : LECTOR Stacked State Retention technique A novel Leakage reduction and State retention Technique in low power VLSI design

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**Abstract—The advent of digital integrated circuits is dominated by higher power consumption. In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Leakage power consumption plays a significant role in current CMOS technology. International Tech-nology Roadmap for semiconductors reports that leakage power consumption dominates the total chip power consumption as technology advances to nano scale. In mobile computing and mobile communication applications powered by battery, the battery life is a premier concern. Leakage power loss is critical in CMOS VLSI circuits as it leaks the battery even when devices are in idle state. To reduce subthreshold leakage power as well as total power in CMOS logic gates and circuits a new circuit technique called LSSR Technique is proposed in this work. This technique reduces maximum amount of leakage power during deep sleep mode, maximum power reduction during dynamic (clocked) mode and has a provision of preserving state in low power sleep mode i.e state retention. This paper presents leakage current mechanisms and different leakage reduction techniques to reduce leakage power consumption. We propose a novel leakage reduction technique named LSSR which can achieve better leakage reduction by maintaining exact logic state(state retention) than the other techniques discussed in this paper**

## I. INTRODUCTION

Power consumption has become one of the major concerns of VLSI circuit design with the rapid launching of battery operated applications. Low power has emerged as a principal theme in todays electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two Components determine the power consumption in a CMOS circuit; Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging power and short circuit power. VLSI fabrication technology is still in the process of evolution which is leading to smaller feature size and to higher packing density of circuitry on a chip. CMOS technology feature size and threshold voltage have been scaling down for decades in order to achieve high performance. Scaling down the feature size and threshold voltage increases sub threshold leakage current. This leads to short channel effects which increases sub threshold leakage current exponentially [1]. This Sub threshold leakage current ultimately increases the leakage power. There are several VLSI techniques for reducing leakage power. Each Technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel LSSR technique that reduces not only leakage power but also dynamic power. We summarized and compared the previous techniques with our new approach

## II. REVIEW OF EARLIER LOW LEAKAGE POWER TECHNIQUES

Techniques for leakage power reduction can be grouped into two categories.

state-preserving techniques; where circuit state is retained and

state destructive techniques; where the current Boolean output value of the circuit might be lost. A state preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state.Some well known techniques for leakage reduction and state retention are reviewed in this section.The most well-known traditional approach is the sleep approach. In the sleep approach, a ”sleep” PMOS transistor is placed between Vdd and the pull-up network of a circuit and a ”sleep” NMOS transistor is placed between the pull-down network and Gnd.These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage. Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor

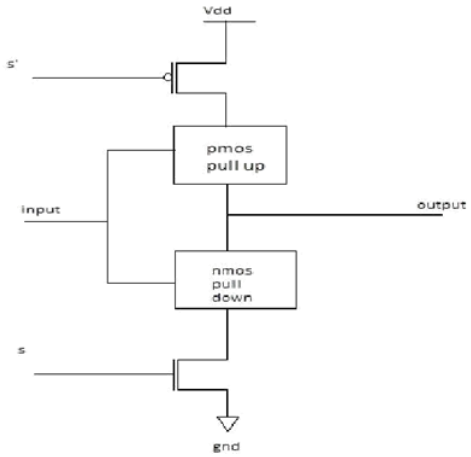


Fig. 1. Sleep Pass

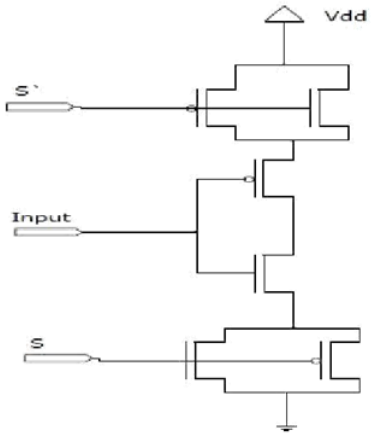


Fig. 3. Dual sleep

into two half size transistors.Transistors in pull-up and pull-down networks are replaced as two half size transistors The sleepy stack approach [5] (Figure 2) combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors.During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active Mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S, which are sleep signals.Another technique called Dual sleep approach (Figure 3) uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit

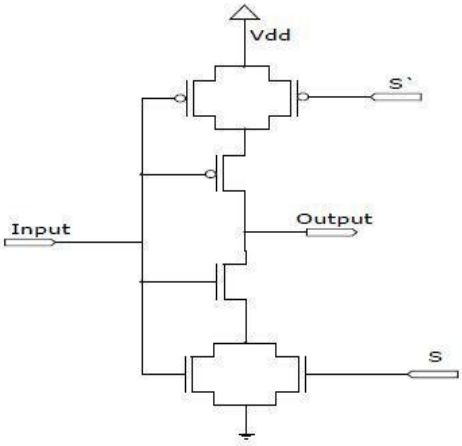


Fig. 2. Sleepy stack

Now we deal with another approach called as Dual stack approach.It is also compared with well-known previous approaches, i.e., the sleepy stack, dual sleep and sleep transistor methods. First we explain the circuit operation for a chain of 4 inverters (Figure 4) in sleep mode. In sleep mode, the sleep transistors are off, i.e. transistor N5 and P5 are off. We do so by making S=0 and hence S=1. Now we see that the other 4 transistors P6, P7 and N6, N7 connect the main circuit with power rail. Here we use 2 pmos in the pull-down network and 2 nmos in the pullup network. The advantage is that nmos degrades the high logic level while pmos degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit. As we know that static power

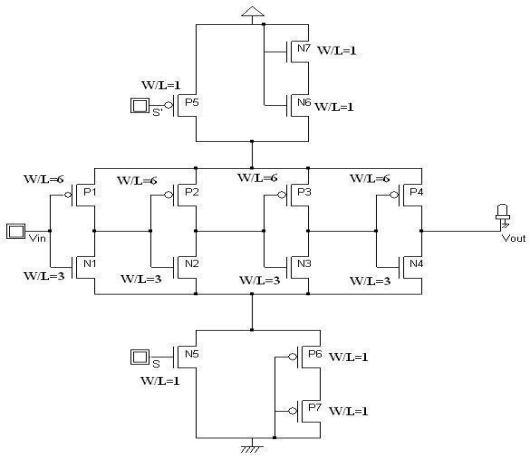


Fig. 4. Dual stack approach (a chain of 4 inverters)

is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N6, N7 and P6, P7. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence

low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current. As a result of stacking, P6 and N6 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S=0, both the sleep transistors (N5 and P5) and the parallel transistors (N6, N7 and P6, P7) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

## III. PROPOSED LOW POWER STATE RETENTION TECHNIQUE

A novel leakage power reduction technique is proposed in this work i.e LSSR [LECTOR(Leakage Control TransistOR (LECTOR)) Stacked State Retention] The LECTOR method [2] inserts two extra Leakage Control Transistors (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other.This technique have very good low leak operation but there is no provision of sleep mode of operation,to over come this problem.extra retention transistors are connected to the output so that during sleep mode the logic state is main-tained.Hence we combine the advantages of LECTOR method and the Forced Stack Technique to reduce the overall power dissipation without compromise with the loss of state (state destructive).so, we call this as a state-preserving technique; where circuit state is retained.

### A. LECTOR

The LECTOR method inserts two extra Leakage Control Transistors (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other. This is stated based on the observation from [3], [2] and [4] that a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path. The number of OFF transistors is related to leakage power as shown in Figure 5. the arrangement of

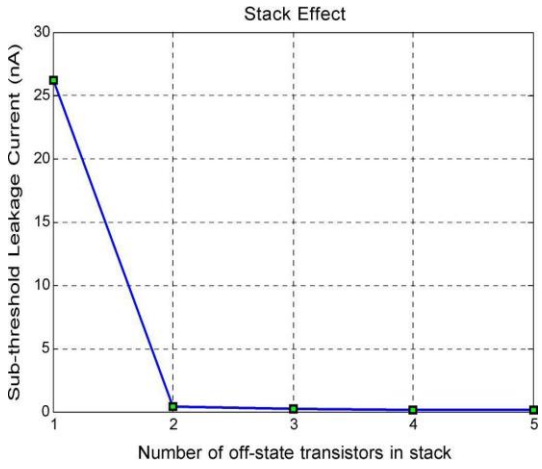


Fig. 5. Stack effect on leakage current

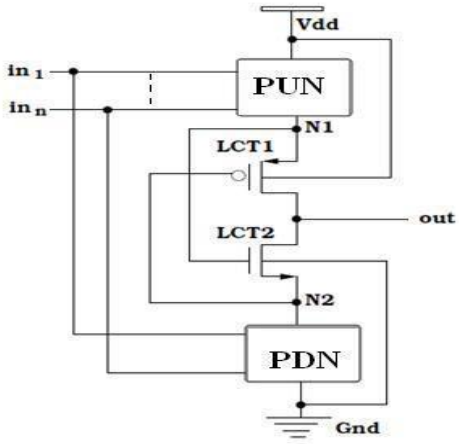


Fig. 6. LECTOR Technique

LECTOR is as shown in fig 6.

### B. Forced Stack Technique

Another technique to reduce leakage current is Forced stack technique.in which a transistor is replace by two half size tran-sistors[6],as shown in fig 7, both pmos and nmos,Transistors in PULL UP and PULL DOWN networks are replaced as two half sized transistors.When the two transistors are turned off together induced reverse bias between the two transistors results in sub threshold leakage current reduction.However divided transistors increase delay significantly.

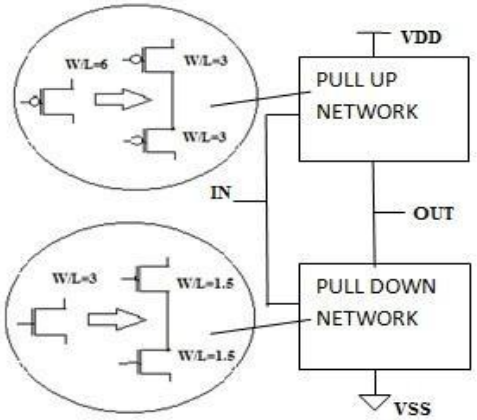


Fig. 7. FORCED STACK technique

### C. Proposed LSSR

In this section we introduce a new leakage current reduction technique for CMOS circuit design. Fig 8 shows LECTOR stack technique which combines the LECTOR and Forced stack techniques. As it combines the features of the above mentioned techniques, two gated leakage transistors are introduced between pull up and pull down networks with high threshold voltage, then stack effect is added to pull up and pull down networks by dividing each transistor in

to half size transistors (i.e., W/2). As more stack effect can be introduced, due to high threshold voltage gated leakage transistors and half size stacked transistors, ultimately more leakage current reduction can be achieved with the proposed technique. Though the leakage reduction techniques

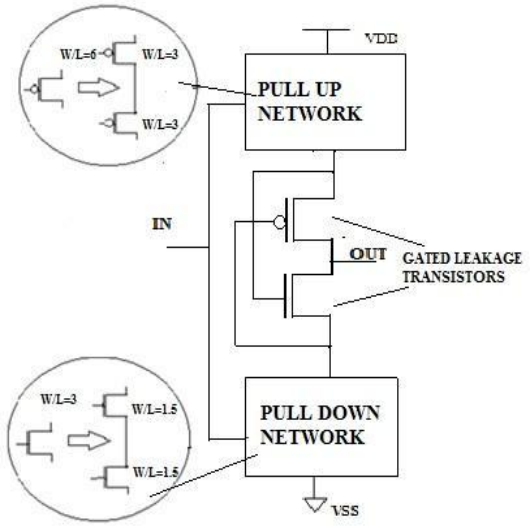


Fig. 8. LSSR stack technique

discussed in above section 2 could achieve leakage current reduction with the penalty of delay but the proposed technique can achieve more leakage current reduction without delay penalty. from fig 9 we can explain modes of operation of

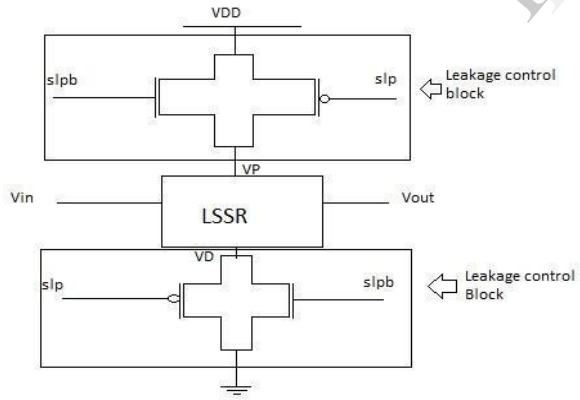


Fig. 9. LSSR Logic

LSSR. The LSSR logic gate has four modes of operation.

a) : Active Mode: both sleep control signals slp = 0 and slpb = 1 are used to switch on the sleep transistors in leakage control block. Thus the virtual ground node VG is at ground potential and the virtual power node VP is at VDD. The gate thus sees good potential difference across nodes VP and VG. The gate functions as per the truth table with good output logic levels.

b) : Deep Sleep Mode: The sleep signals are held at slp = 1 and slpb = 0 states to switch off all the sleep transistors in both pull up and pull down leakage control blocks. Thus the actual power and ground path are broken and the circuit experiences lower voltage across the nodes VP and VG. A very high resistance path is established between VDD and ground due to the parallel combination of the off resistance of sleep transistors and the leakage current flowing through the circuit
reduces significantly and hence lowest power dissipation.

c) : State Retention Mode 1: The sleep signals are maintained at slp = 0 and slpb = 0. The circuit sees a higher than ground voltage at the node VG and full VDD at the node VP. The state retention takes place with low leakage current with the output at good logic 1 level.

d) : State Retention Mode 0: The sleep control signals are maintained at slp = 1 and slpb = 1. The connection to actual ground is complete, the node VP is at lower VDD. Thus the state retention takes place with low leakage current with the output at good logic 0 level.

## IV. Conclusion

Scaling down the CMOS technology feature size and thresh-old voltage has increased leakage power tremendously. In this paper we have presented a novel technique called LECTOR Stack which can achieve more leakage current reduction without penalty for the delay. The implementation of the other techniques like base case, forced stack and LECTOR techniques are also presented. Forced stack and LECTOR techniques can also achieve good leakage current reduction with the delay penalty. When the speed is not the criteria, then definitely designers can choose the other techniques like stack and LECTOR.The proposed LECTORstack technique is best in terms of speed and leakage power consumption.

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