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Low Voltage Digital ECG Acquisition System

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***Abstract*— Nowadays biomedical devices play a major role in hospitals. This is due to the fast development in integrated circuit fabrication. These devices can be used as wearable and implantable appliance as well as monitoring equipment. In all these applications, the bio signal is first processed and converted to digital format. In conventional method, the signal conditioning is mainly done with amplifiers and filters and then the amplified signal is converted to digital format with the help of an ADC which requires high supply voltage and causes more power consumption. So this work aims to implement an ECG (electrocardiogram) acquisition system having a digital architecture for reducing the power consumption and area of the chip. This is compatible with CMOS technology and hence can be operated at low voltages. Here instead of ADC, a Time to Digital Converter (TDC) is used to convert the analog voltage into a digital format. Conversion usually takes place through two stages. First the input voltage is converted into a time interval using a voltage to time converter (VTC). This time interval is then converted into digital form using TDC. This work is carried out in .18um CMOS technology.**

***Keywords*— VTC, Low power, scaling, TDC**

I. INTRODUCTION

Nowadays biomedical devices play major role in hospitals. This is due to the fast development in integrated circuit fabrication. These devices can be used as wearable and implantable appliance [1] as well as monitoring equipment. In all these applications, the bio signal is first processed and converted to digital. So this work aims to implement an ECG (electrocardiogram) acquisition system having a digital architecture for reducing the power consumption and area of the chip. ECG is the graphical representation of our heart's electrical activity and also the most recognized biological signal. Cardiovascular abnormalities in a person can alter the ECG wave shapes which can be identified by the doctor through proper diagnosis. The ECG signal taken from a patient may get corrupted due to several external factors like noises, skin resistance, movement of body etc. So this signal must be preconditioned for getting the correct information. In conventional method, the signal conditioning is mainly done with amplifiers and filters and then the amplified signal is converted to digital format with the help of an ADC which requires high supply voltage and causes more power consumption.

But nowadays since CMOS technology gets advanced, scaling is possible. That is supply voltage can be reduced which decreases the power consumption. But SNR (Signal to Noise Ratio), CMRR (Common Mode Rejection Ratio) and gain of analog parts [2] of the system will get negatively affected when supply voltage is reduced. Hence it is necessary to get new digital architectures that are completely compatible with CMOS technology scaling. Thus digital system plays an important role in our today's life. It usually stores and process data in two states: 0 and 1. These are called bits. In digital systems information storage is much easier than in analog systems and also since it has good noise immunity, thus the data can be stored and retrieved perfectly.

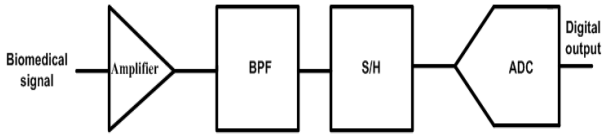

Fig.1. Conventional ECG acquisition system [1].

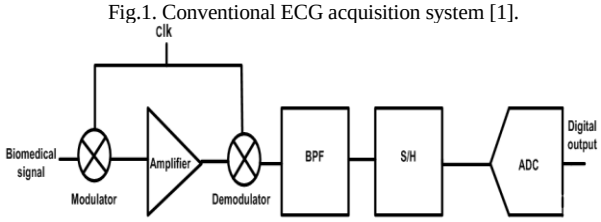

Fig.2. Chopper based ECG acquisition system [4].

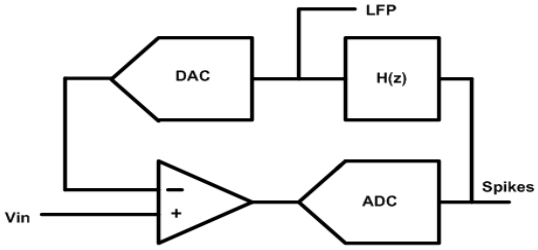

Fig.3. Mixed signal feedback architecture [5].

Different bio-signal acquisition systems are discussed in literature [1]-[5]. Fig. 1 shows the block diagram of conventional ECG acquisition system [1]. In this, the amplified signal from the front end amplifier is given to BPF (Band Pass Filter) for removal of unwanted noise and then given to ADC (Analog to Digital Converter). Since large capacitors which requires more area are required for ac coupling the amplifier [3] with electrode to reduce the offset, this method is not desirable. Fig. 2 shows a chopper based technique [4] which reduces the flicker noise but is more difficult in low power design. Fig. 3 shows a mixed signal feedback technique [5]. This is a digitally enhanced approach. Even though this technique helps in removing unwanted interferences, the amplifier which is the only analog block in the system consumes more power. All the above mentioned systems consist of at least one analog block and passive elements which increases the power and area. So in this work a digital architecture for ECG acquisition system is proposed. The conditioning of the signal is mainly done in time and digital domain using active electrode, VTC (Voltage to Time

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Converter) and is given to TDC (Time to Digital Converter). This work is carried out in 180 nm CMOS technology with 0 .9V supply voltage.

II. DIGITAL ARCHITECTURE

Fig. 4 shows the block diagram of the digital [6] system. This mainly consists of an active electrode, Voltage to Time Converter (VTC) and Time to Digital Converter (TDC).

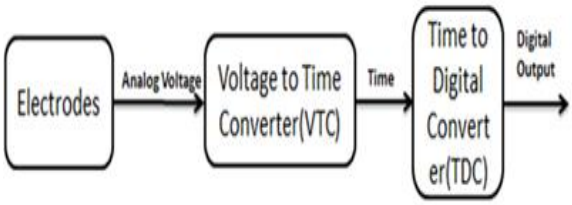

Fig.4. Digital architecture

In this system apart from the voltage domain, bio signal conditioning is done in the time and digital domain and not affected by the supply voltage scaling. Hence the digital CMOS technology can be well utilized. Here first the ECG signal is given to an active electrode which acts as a transducer and converts ECG signal into an electrical signal with a good amplification. Active electrode [2] consists of some active elements and is mainly used to match with the high skin impedance. Then the amplified signal is given to a voltage to time converter which converts the input voltage to a time domain signal. Then the signal is given to a Time to Digital Converter. Here instead of normal ADC, a Time to Digital Converter (TDC) [7] is used to convert the analog voltage into a digital format. This is because since the digital gates are not affected by reduced power supply, the TDC resolution is much better with CMOS scaling.

A. Active Electrode

In ECG acquisition systems, an external electrode attached to our skin captures the electrical activity of the heart. A charge is associated with each cell membrane of our heart. During every heart beat this charge gets depolarized which appear as tiny ECG signals which are captured by the electrodes. Hence the electrodes act as transducers and converts ECG signals into electrical signals. An electrode mainly consists of electrical conductors in contact with aqueous ionic solutions. The interaction between the ionic solution and the electrons in electrode greatly affects the signal captured and change the concentration of ions in solution near the metal surface. This will alter the charge neutrality in the region and the electrolyte around the metal will be at another potential. Thus a half cell potential called electrode offset [2] is generated between the metal and electrolyte and the input signal get superimposed on these offsets.

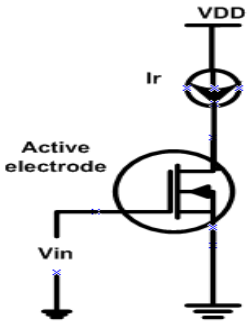

Fig.5. Active electrode

Generally passive electrodes are used in most of the ECG readings because they are cheap to manufacture and maintain. But these types of electrodes require a special skin preparation before the electrodes are attached to the skin to lower the high skin impedance which makes them more difficult. So in this work, active electrodes are used instead of passive electrodes to avoid the offsets. For this, no special skin preparation is required. Inside the electrode, a preamplifier is placed and then attached to the skin so that the high skin impedance can be avoided by the high input resistance of the amplifier. This circuit functions properly at low supply voltages since active loads (current source) providing a high voltage gain is used.

Safety is another reason to use active electrodes since electrocution is much smaller compared to passive electrodes.

B. Voltage to Time Converter (VTC)

Nowadays due to the reduction in supply voltage, there are lots of challenges in voltage domain ADC designs. Since the digital gates are not affected by reduced power supply, the TDC resolution is much better with CMOS scaling. A TDC converts an input voltage into a digital form. Before the signal is given to TDC [8], it is first given to a voltage to time converter where it converts the input voltage into a time domain signal. There are different types of VTC circuits [9] like comparator based VTC, moving average and current starved inverter based VTC. In this work a simple current starved inverter based voltage to time converter is used since it provides less power consumption.

A simple current starved inverter as shown in Fig. 6 [9] is the main part of most of the VTC's. Current starving is a technique to control an inverter's delay by adding two extra transistors as shown in Fig. 6. When the clock is at high and V_{in} decreases, the delay gets increased by increasing the effective drive resistance of the inverter. The delay of the falling edge of the clock signal is controlled by the input voltage (V_{in}) through transistors M2 and M3 by controlling M1's discharging current.

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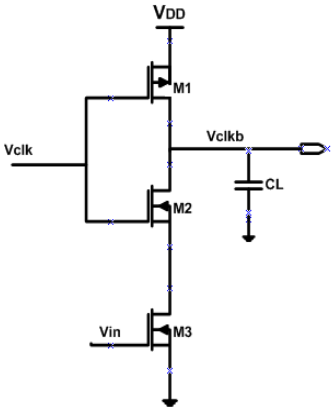

Fig.6. Simple current starved inverter

Fig. 7 shows the block diagram of the circuit. In this the input voltage V_{in} is given to the rising and falling current starved inverter circuit. In the rising circuit, V_{in} controls the rise time of the inverter through transistor PM2. When V_{in} approaches V_{DD}, PM2 is in off condition. Then the alternative current path is provided by a weak transistor PM3. Similarly in the falling circuit, V_{in} controls the fall time of the inverter through transistor NM2. When V_{in} is less than the threshold voltage of NM2, transistor NM1 provides an alternative current path.

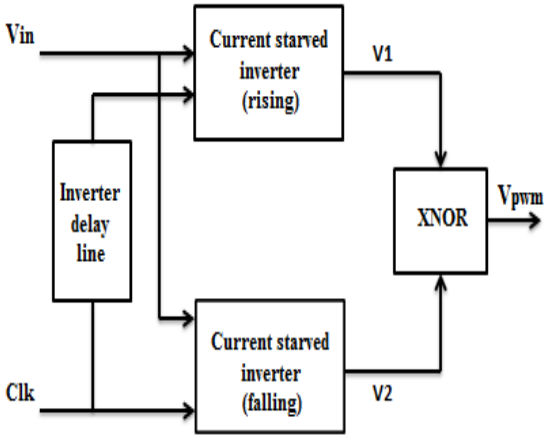

Fig.7. Block diagram of VTC

The clock pulse is directly given to the falling CS inverter circuit. Hence V2 is an inverted version of the clock pulse and the delay of the falling edge is controlled by V_{in}. On the other hand, clock pulse is first given to an inverter delay before it is applied to the falling CS inverter circuit. Hence voltage V1 is a delayed version of clock pulse. The voltages V1 and V2 are then applied to XNOR gate to get the pulse width modulated output.

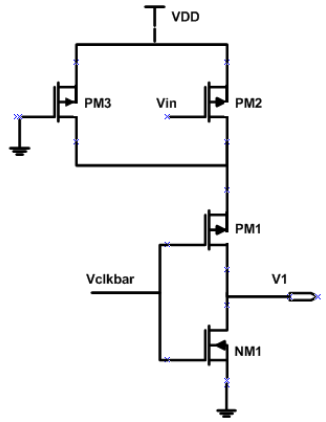

Fig.8. T_{rise} current starved inverter circuit

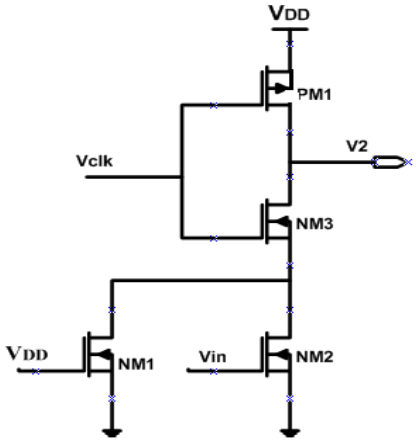

Fig.9. T_{fall} current starved inverter circuit

The PWM output has two pulses. The pulse width of first pulse is

$$\Delta + T_{rise} - T_{fall} \ldots\ldots\ldots\ldots (1)$$

where

Δ = delay in inverter line
T_{rise} = rising delay
T_{fall} = falling delay

In this the input voltage inversely controls the rising and falling delays. Here the rising delay increases as V_{in} increases because the V_{gs} (Gate to source voltage) of transistor PM2 (V_{DD}-V_{in}) decreases. Also the falling delay decreases as V_{gs} of transistor NM2 increases.

Sizing of the transistors are chosen to achieve minimum power consumption. Transistors PM3 and NM1 are small size transistors. All the other transistors are larger than these by 2.5X. The VTC circuit [10] is then followed by a Time to Digital Converter which converts the pulse width into a digital form.

C. Time to Digital Converter

Generally an ordinary ADC (Analog to Digital Converter) in an ECG acquisition system converts the amplified analog signal into a digital form. The analog domain signal information is mainly indicated by voltage or current. But for this, in order to detect the digital code for an analog signal, one or more comparators followed by sample and hold circuit is necessary. Also the performance of voltage domain ADC

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depends on the gain and SNR of transistors which gets reduced during CMOS scaling. So in order to avoid these challenges, in this work a TDC is implemented for converting analog input voltage into digital format. In TDC [11], the performance (timing resolution) mainly depends on the switching speed and not on the gain of transistors. Hence the resolution of TDC increases with reduced gate delay in contrary to amplitude resolution.

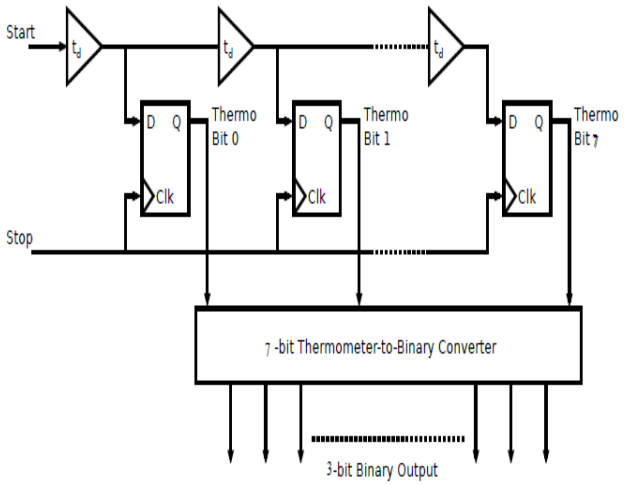

Fig.10. Block diagram of TDC

In this work, a delay line based TDC is used as shown in Fig. 10. It is one of the simple TDC and can be considered as another form of flash ADC in time domain. For this, 2^{N-1} delay stages are required for an N-bit operation. The delay stages consist of buffer and D-flip flops. The sampling elements can be either latches or flip flops.

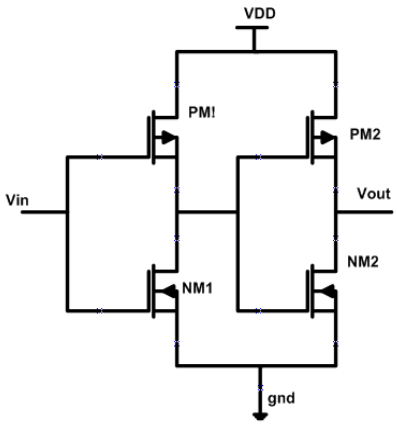

Fig.11. Buffer circuit

Fig. 11 shows a buffer circuit. It has only a single input and output and acts opposite to NOT gate. A buffer generally passes the input to the output without any changes but provides a propagation delay [12] between them by driving large capacitive loads.

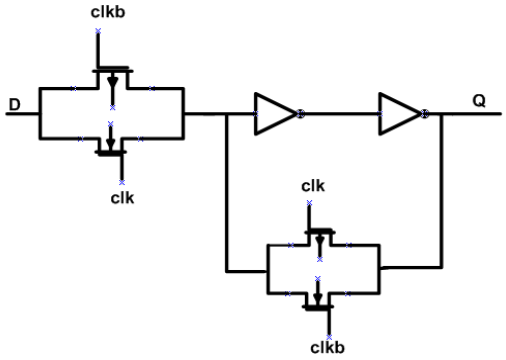

Fig.12. D flipflop

Fig. 12 shows a D flip flop which is also called a delay flip flop since it introduces a propagation delay in the circuit. That is the data comes at the output after a certain delay. The D flip flop is obtained by providing a NOT gate in between the S and R input signals of SR flip flop.

In this work, seven delay stages are needed since a 3-bit TDC is used. So it consists of seven buffer stages in cascaded form and the output of each buffer stage is connected to the data input of D flip flop. The two inputs start and stop signal operates the block [13]. All the flipflops and buffer output resets when the start signal is at logic low. When the start signal is at logic high state, it propagates through the delay chain. Thus each buffer output is a delayed version of start signal. When the stop signal arrives, the delayed versions at the output of buffer stages gets sampled and the data [14] is recorded by the flip flops. The resulting data is in the form of a thermometer code and gets converted into 3-bit binary form through a thermobit to binary encoder.

III. Simulation Results and Discussions

To investigate the power consumption, delay and area for the above digital ECG acquisition system, first the circuit simulations was carried out using cadence virtuoso tool in 180 nm technology and the output waveform was obtained. Then the average power consumption, delay and area of the entire digital architecture was analyzed and compared with conventional analog ECG system. The below graphs show the output waveforms obtained for active electrode, VTC, TDC and finally the combined output. The system operates in 0.9 V supply voltage and 100 MHz frequency.

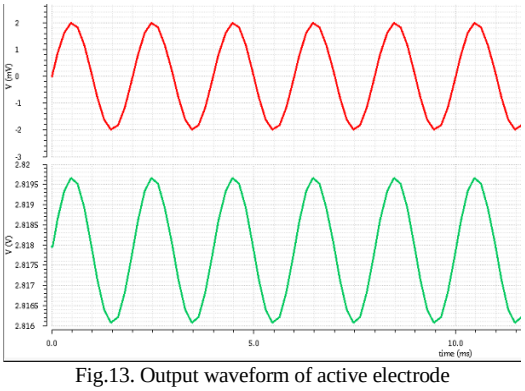

Fig.13. Output waveform of active electrode

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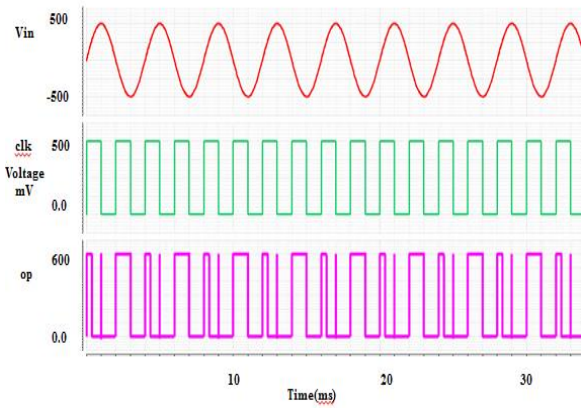

Fig.14. Output waveform of VTC circuit

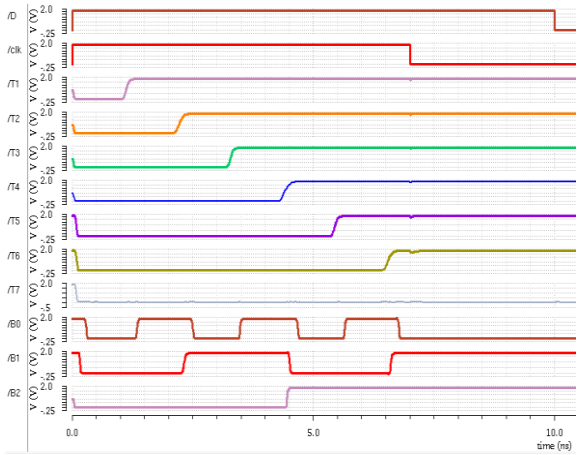

Fig.15. Output waveform of TDC

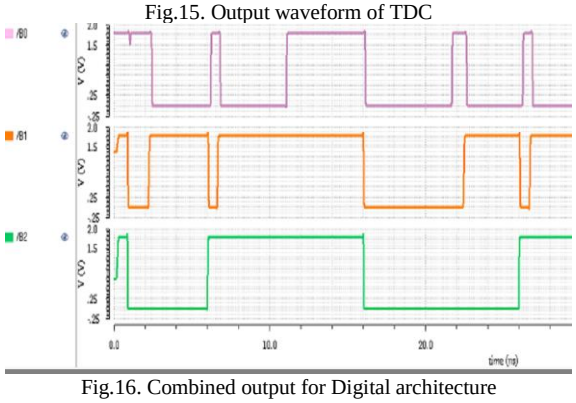

Fig.16. Combined output for Digital architecture

TABLE I. ANALYSIS TABLE

ECG Acquisition System		Power Consumption (mw)	Delay (ns)	No. of transistors
Conventional ECG Acquisition System (using normal ADC)		585.1	5.62	135
Digital Architecture (VTC based TDC)				
1	Comparator based VTC	167.6	-	10
2	Moving average VTC	55.66	-	18
3	Current starved inverter based VTC	13.51	-	10
Proposed System (using CS VTC and TDC)		303.2	6.21	125

From the above table, it was observed that, for a conventional ECG acquisition system using normal ADC, the power consumption was 585.1 mW which is very high since analog blocks which require high supply voltages are mostly used in the system. Also silicon area used is high since more number of passive elements are needed. But for the proposed digital system using VTC based TDC, the power consumption and area is reduced even for all the VTC circuits shown in the Table. I. The current starved inverter based VTC is used in the system since a small capacitance is discharged through input signal dependent current source which leads to less power consumption (13.51 mW). Thus a 48% of power reduction is observed in the proposed system along with a reduction in the silicon area used.

IV. CONCLUSION

In the future expectation of the dominance of CMOS technology, in this work a digital architecture for ECG acquisition system is implemented. The simulation was carried out using standard cadence virtuoso tool with 180 nm technology. In conventional ECG acquisition systems, a normal ADC along with passive elements which requires high supply voltage was used which leads to high power consumption and area. In the proposed system, VTC based TDC is used leading to less power consumption since TDC depends more on switching speed rather than transistor characteristics and hence compatible with CMOS technology and operates at low supply voltage. An active electrode which helps in offset cancellation is also introduced. Also passive elements, LNA and analog filters are not used that leads to the reduction in chip area.

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