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Low-Power Two-Stage Miller-Compensated CMOS OTA in 45 nm Technology with a 180 nm Comparison for Active Low-Pass Filter Applications

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Abstract - This paper presents a low-power two-stage CMOS operational transconductance amplifier (OTA) designed in 45 nm technology, together with the same architecture built in 180 nm technology for comparison. The OTA has an NMOS differential input stage with a PMOS current-mirror active load, followed by a common-source second stage with Miller compensation. The 45 nm design runs from a 1.1 V supply at a 10 µA bias current and has been taken through the complete flow of schematic simulation, layout, LVS, post-layout simulation and process-corner analysis. It gives a DC gain of 60.9 dB, a unity-gain frequency (UGF) of 17.4 MHz, a phase margin of 75.8° and a power of 42.7 µW at the schematic stage, and 61.0 dB, 11.9 MHz, 59.3° and 42.9 µW after layout. Across SS and FF corners from −40 to 125 °C, the gain stays between 58.9 and 61.3 dB. The 180 nm design uses the GPDK 180 nm process at 1.8 V. Its bias current was swept from 5 µA to 30 µA and 20 µA was chosen as the operating point, giving a DC gain of 66.01 dB at 36 µW. It has been taken through layout, DRC and a clean LVS, while its post-layout simulation is still to be done. The suitability of the OTA as the transconductance element of a Gm-C active low-pass filter is also discussed.

Keywords - CMOS OTA, Two-Stage OTA, Miller Compensation, 45 nm CMOS, 180 nm CMOS, Bias Current, Post-Layout Simulation, LVS, Active Low-Pass Filter.

I.INTRODUCTION

The rapid advancement of portable electronic devices, wireless communication systems, and biomedical applications has significantly increased the demand for low-power and high-performance analog integrated circuits. Although digital circuits dominate modern electronic systems, analog circuits remain indispensable because real-world signals are inherently analog in nature. Among various analog building blocks, the Operational Transconductance Amplifier (OTA) is one of the most important components due to its versatility and wide range of applications in active filters, data converters, sensor interfaces, phase-locked loops, and analog signal processing systems.

A two-stage CMOS OTA is widely employed in analog circuit design because it provides high voltage gain, improved output swing, and better driving capability compared to single-stage amplifiers. The first stage generally consists of a differential amplifier that offers high input impedance and initial voltage amplification, while the second stage provides additional gain to meet the requirements of modern analog applications. However, the inclusion of multiple gain stages introduces additional poles in the frequency response, which may lead to instability if appropriate compensation techniques are not incorporated.

Miller compensation is one of the most widely adopted methods for improving the stability of two-stage OTAs. By introducing a compensation capacitor between the two gain stages, the dominant pole is shifted to a lower frequency while the non-dominant pole moves to a higher frequency. This pole-splitting effect enhances the phase margin and ensures stable operation without significantly compromising the amplifier's bandwidth. As a result, Miller-compensated two-stage OTAs have become a preferred choice for designing reliable and efficient analog integrated circuits.

Another critical factor influencing OTA performance is the bias current. The bias current directly affects the amplifier's transconductance, gain, bandwidth, slew rate, and overall power consumption. Proper optimization of the bias current enables designers to achieve an effective balance between power efficiency and circuit performance. This aspect is particularly important in battery-powered and portable devices, where minimizing power consumption while maintaining satisfactory performance is a key design objective.

Technology scaling has pushed analog designers towards lower supply voltages, which leaves less voltage headroom and lowers the intrinsic gain of each transistor. A two-stage OTA is a practical way to get the gain back at such nodes. The main design in this work is therefore in 45 nm CMOS, where the supply is only 1.1 V. The 180 nm node, on the other hand, is still widely used in academic work and low-cost products because of its higher supply voltage, reliable device models and low fabrication cost, which makes it a useful reference for the same circuit at a more relaxed voltage.

In this work we design a low-power two-stage Miller-compensated OTA in 45 nm CMOS and take it through the complete flow in Cadence Virtuoso: schematic design, AC and transient simulation, layout, LVS, post-layout simulation and process-corner analysis. The same architecture is then built in 180 nm CMOS (GPDK 180 nm) for comparison. For the 180 nm design the bias current was optimized by sweeping it from 5 µA to 30 µA, and the design has been taken through layout, DRC and LVS. The two designs are compared at the schematic level, and the suitability of the OTA for active low-pass filter applications is discussed.

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II. RELATED WORK

The Operational Transconductance Amplifier (OTA) has become one of the most widely used analog building blocks in integrated circuit design because of its ability to provide high gain, low power consumption, and compatibility with CMOS technology. Two-stage OTA architectures are extensively employed in analog signal processing applications such as active filters, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), sensor interfaces, biomedical instrumentation, and communication systems. In recent years, researchers have proposed several techniques to improve OTA performance by optimizing gain, bandwidth, phase margin, slew rate, and power consumption through different circuit topologies and compensation methods

In paper [1] presented a high-performance two-stage OTA designed for biomedical applications. Their work emphasized low-power operation and high voltage gain while evaluating the amplifier through DC, AC, and transient analyses. The proposed design demonstrated that a properly optimized two-stage OTA can satisfy the stringent power requirements of biomedical systems.

In [2] proposed a bulk-driven two-stage CMOS OTA with cascode loading to improve wideband performance and stability. The use of bulk-driven input transistors reduced the supply voltage requirement, whereas the cascode configuration increased gain and bandwidth. However, the additional circuit complexity makes the design less suitable for simple low-power analog applications.

In paper [3] introduced an ultra-low-power two-stage OTA operating at 0.4 V using self-cascode composite transistors and intrinsic current-buffer Miller compensation. Their design achieved nanowatt power consumption while maintaining high gain and stability, making it suitable for ultra-low-power sensor applications.

In paper [4] developed a two-stage OTA employing series-cascode-Miller compensation with an anti-pole-splitting technique for broadband RF receivers. The proposed compensation method significantly enhanced bandwidth and stability for high-frequency applications but increased design complexity compared to conventional Miller compensation.

Alan and Ergin [5] designed an adaptive active filter using CMOS Operational Transconductance Amplifiers implemented in 65 nm technology. Their work demonstrated the importance of OTAs in active filter applications by achieving electronically tunable filter characteristics with improved frequency response.

Tripathy [6] proposed a high-performance two-stage OTA for low-frequency signal amplification in power-constrained systems. The amplifier achieved high voltage gain and stable operation while maintaining low power consumption, making it suitable for low-frequency analog signal processing applications.

Danesh [7] introduced an isolated frequency compensation technique for ultra-low-power low-noise two-stage OTAs. The proposed compensation approach improved phase margin and reduced noise while preserving bandwidth, offering better stability than conventional compensation techniques.

Jayachandran [8] designed a second-order low-pass filter using an inverter-based CMOS OTA based on the gm/ID methodology. Their work demonstrated that OTA optimization directly influences the filter's frequency response and power efficiency, highlighting the importance of amplifier design in analog filter implementation.

In paper [9] presented a Class-AB bulk-driven quasi-floating gate two-stage OTA operating with nanowatt power consumption. The proposed architecture achieved significant power savings and high gain, making it suitable for energy-constrained biomedical and portable electronic applications.

Although recent studies have introduced advanced compensation methods, bulk-driven architectures and ultra-low-power techniques, many of them add circuit complexity or target specialised applications such as biomedical devices or RF receivers. In contrast, this work uses a conventional two-stage OTA with Miller compensation. The main design is in 45 nm CMOS and is verified through post-layout simulation and process corners, and the same circuit in 180 nm CMOS, tuned through a bias-current sweep, serves as a comparison. The aim is a balanced trade-off between gain, bandwidth, stability and power that is simple enough to reuse in active low-pass filters.

III. PROPOSED OTA ARCHITECTURE

The proposed circuit is a conventional two-stage CMOS OTA, chosen for its simplicity, well-understood compensation behaviour and suitability for low-voltage, low-power operation. It is designed in 45 nm CMOS at a 1.1 V supply as the main design, and the same topology is built in 180 nm CMOS at 1.8 V for comparison. The first stage is a differential pair biased by a tail current source, and an active current-mirror load converts the differential input voltage into a current. This stage sets the input transconductance of the amplifier and provides most of the low-frequency voltage gain along with a high input impedance.

The second stage is a common-source gain stage driven by the output of the first stage. It provides additional voltage gain and supplies the current needed to drive the output load capacitance, extending the achievable output voltage swing beyond what the first stage alone could provide. Biasing throughout the amplifier is established using current-mirror reference circuitry, so that the tail current of the differential pair and the bias current of the second stage are derived from a common reference current, allowing the overall bias current to be adjusted as a single design variable during optimization.

A Miller compensation capacitor (Cc) is connected across the second gain stage, between its input and output nodes, to control the frequency response of the amplifier. This capacitor splits the two dominant poles of the two-stage structure, pushing the first pole to a lower frequency and the second pole to a higher frequency, which is essential for maintaining adequate phase margin when the amplifier is used in a closed-loop configuration such as an active filter.

Both designs use the same topology, so only the transistor sizes, the bias current and the compensation values change between the two nodes. Fig. 1 shows the schematic of the 45 nm design and Fig. 2 shows the 180 nm design.

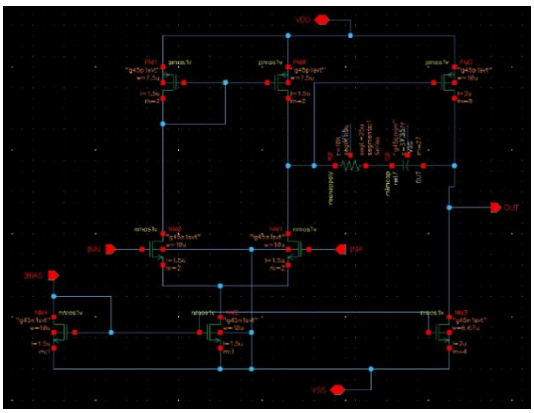


Fig. 1. Schematic of the proposed two-stage CMOS OTA in 45 nm technology.

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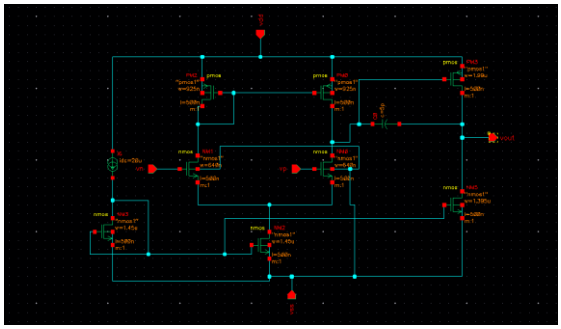


Fig. 2. Schematic of the two-stage CMOS OTA in 180 nm technology (GPDK 180 nm).

IV. CIRCUIT DESIGN AND MATHEMATICAL ANALYSIS

The design of the proposed OTA is grounded in standard square-law MOSFET behaviour in strong-inversion saturation. For a MOSFET biased in saturation, the drain current is related to the overdrive voltage (Vov = VGS − VTH) by

$$Id = \tfrac{1}{2}\,\mu n Cox\,(W/L)\,Vov^2 \qquad (1)$$

where μn is the carrier mobility, Cox is the gate-oxide capacitance per unit area, and W/L is the transistor aspect ratio. The corresponding small-signal transconductance is obtained by differentiating the drain current with respect to the gate-source voltage, giving

$$gm = 2Id / Vov \qquad (2)$$

Equations (1) and (2) show that, for a fixed overdrive voltage, transconductance scales directly with bias current, while for a fixed bias current, transconductance can be increased by reducing the overdrive voltage — that is, by increasing the transistor W/L ratio. Both relationships are central to the bias-current and sizing optimization discussed in Section V.

For a single common-source gain stage, the small-signal voltage gain can be approximated as the product of the transconductance and the output resistance seen at the drain node,

$$Av \approx gm\ ro \qquad (3)$$

The overall DC gain of the two-stage OTA is the product of the gain of the first (differential) stage and the gain of the second (common-source) stage. Each stage follows the form of (3) at its own output node, where ro is made up of the output resistances of the transistors connected to that node, so the exact expression follows from the schematic.

The unity-gain frequency (UGF) of a Miller-compensated two-stage amplifier is set, to first order, by the transconductance of the first stage and the value of the compensation capacitor, since the dominant pole is determined by Cc acting on the high-impedance first-stage output node. Increasing gm1 (through bias current or sizing) raises the UGF, while increasing Cc lowers it. The gain-bandwidth product (GBW) follows the same dependence and is distinct from the UGF only in that GBW refers to the product of low-frequency gain and bandwidth of the dominant pole, whereas UGF is the frequency at which the open-loop gain magnitude crosses 0 dB; for a single-dominant-pole response the two coincide.

Miller compensation works by feeding back the output of the second stage to its input through Cc, which — due to the Miller effect — presents an effectively much larger capacitance at the first-stage output node. This pushes the dominant pole to a lower frequency while simultaneously pushing the second (non-dominant) pole to a higher frequency, a mechanism referred to as pole splitting. The phase margin (PM) is obtained from the open-loop AC response as the difference between 180° and the magnitude of the phase angle at the frequency where the loop gain crosses 0 dB,

$$PM = 180° + \varphi(\text{at 0 dB crossover}) \qquad (4)$$

using the standard convention in which φ is negative for a stable, negative-feedback system. A larger phase margin corresponds to a more heavily damped, more stable closed-loop response, at the cost of reduced bandwidth.

The slew rate (SR) of the amplifier is limited by the maximum current available to charge or discharge the compensation capacitor during a large-signal transition, and can be approximated as

$$SR \approx I / Cc \qquad (5)$$

where I is the current available to the compensation node (typically the first-stage bias current in the class-A two-stage topology). This relationship shows that slew rate can be improved either by increasing the bias current or by reducing the compensation capacitance, both of which interact with the gain, bandwidth, and stability trade-offs discussed in Sections V and VI.

Total static power consumption of the amplifier is approximated as the product of the supply voltage and the total supply current drawn by the biasing branches,

$$P \approx VDD \times I_supply \qquad (6)$$

where I_supply is the sum of the individual branch bias currents (tail current of the differential pair and the bias current of the second stage), distinguished here from any single branch current quoted in isolation.

V. BIAS CURRENT OPTIMIZATION

Bias current and transistor sizing decide how well the OTA balances speed against power. As shown in Section IV, the bias current sets the transconductance of the input pair for a given overdrive voltage, and the transconductance in turn determines the DC gain (through Av ≈ gm ro), the unity-gain frequency (through gm1 and Cc) and the slew rate (through I/Cc). Raising the bias current also raises the total supply current and therefore the static power, per P ≈ VDD × I_supply. Speed and power pull in opposite directions, so the bias current cannot simply be increased.

Transistor width also plays a coupled role. For a fixed drain current, increasing W/L reduces the required overdrive voltage and increases transconductance, per (1) and (2); this is beneficial for gain and for reducing the input-referred thermal noise. However, excessively increasing transistor width also increases the gate and junction parasitic capacitances at each node, which lowers the frequency of the non-dominant pole and can erode the phase margin achieved through Miller compensation. Widening transistors indefinitely is therefore not a strictly beneficial strategy; beyond a certain point, the parasitic-capacitance penalty outweighs the transconductance benefit, and the

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amplifier's stability and effective bandwidth degrade even though its DC gain may still improve marginally.

The 45 nm design was sized to meet the gain and stability targets at a 1.1 V supply and a 10 µA bias current. The detailed bias-current sweep described here was carried out on the 180 nm design, which was optimized iteratively rather than through a single closed-form calculation. Starting from an initial bias current of about 20 µA and exploratory transistor dimensions, including aspect ratios near W/L ≈ 1.83 µm / 0.5 µm for the PMOS devices and W/L ≈ 1.395 µm / 0.5 µm for the NMOS devices, the bias current and device widths were varied in Cadence Virtuoso. DC gain, unity-gain frequency, phase margin, slew rate, output swing and power were checked after each change, and each iteration was compared with the others to see which direction of change improved the metrics of interest without badly degrading the rest.

TABLE II: Effect of bias current on DC gain and unity-gain frequency (180 nm design)

Ibias (uA)	Gain (dB)	UGF (MHz)
5	78.09	251.189
10	75.20	570.082
15	72.24	805.525
20	66.01	811.265
25	57.142	747.51
30	47.74	630.95

VI. MILLER COMPENSATION AND STABILITY ANALYSIS

The purpose of the Miller compensation capacitor Cc is to guarantee closed-loop stability of the two-stage OTA by controlling the location of its dominant and non-dominant poles. Without compensation, the two gain stages each contribute a pole at a comparatively low frequency, and the two poles can lie close enough in frequency that the amplifier accumulates nearly 180° of phase shift before its loop gain falls to 0 dB, leaving little or no phase margin.

Connecting Cc across the second (high-gain) stage exploits the Miller effect: from the perspective of the first-stage output node, the compensation capacitor appears multiplied by approximately one plus the gain of the second stage, creating a large effective capacitance at that node. This pushes the first pole down in frequency, making it the new dominant pole. Simultaneously, the feedback path provided by Cc modifies the impedance at the second-stage output, pushing the second (non-dominant) pole up in frequency. This simultaneous separation of the two poles is known as pole splitting, and it is the mechanism by which Miller compensation restores adequate phase margin.

The value chosen for Cc directly affects the trade-off between stability and bandwidth. Increasing Cc pushes the dominant pole to a lower frequency and the non-dominant pole to a higher frequency, generally improving phase margin, but it simultaneously lowers the unity-gain frequency, per the discussion in Section IV, and reduces the achievable slew rate, per SR ≈ I/Cc. Conversely, reducing Cc raises the bandwidth and slew rate at the cost of reduced phase margin and a greater risk of instability when the amplifier is embedded in a feedback loop, such as the active filter application discussed in Section X. Increasing Cc therefore does not uniformly improve every performance metric; it must be chosen as part of the same iterative trade-off process described in Section V, alongside the bias current and transistor sizing.

For the 180 nm design, compensation capacitor values of 2 pF and 10 pF were tried in different iterations, together with load capacitances of 1 pF, 1.5 pF and 2 pF. The phase margin varied a lot between iterations. Some intermediate designs had a badly degraded phase margin and would be unstable or only marginally stable in closed loop, while one iteration showed a crossover phase of about −65°, which corresponds to a much healthier phase margin. The phase margins of the final designs are reported in Section VIII. The 45 nm design uses an R-C Miller network, in which the series resistor moves the right-half-plane zero created by Cc to a harmless location.

VII. SIMULATION METHODOLOGY

All simulations were done in Cadence Virtuoso. The 45 nm design uses the 45 nm process design kit with a 1.1 V supply, a 10 µA bias current and a 1 pF load. The 180 nm design uses the GPDK 180 nm kit with a 1.8 V supply. A mix of DC, AC and transient analyses was used to characterize each design, as summarized below.

A. DC Operating-Point Analysis

A DC operating-point (DC-OP) analysis was performed first for every design iteration to confirm that each transistor operates in its intended region — saturation for the signal-path devices — and to verify the bias currents and node voltages against their expected values. This step is a prerequisite for meaningful AC and transient results, since small-signal parameters such as gm and ro are only valid around a correctly established operating point.

B. AC Frequency-Response Analysis

An AC analysis was used to obtain the open-loop magnitude and phase response of the amplifier. This analysis directly yields the DC (low-frequency) gain, the unity-gain frequency (the frequency at which the magnitude response crosses 0 dB), and the phase margin (the phase at that same crossover frequency, referenced to the −180° stability boundary). The AC analysis is essential because it is the only means of directly verifying frequency-domain stability margins before the amplifier is placed in a closed-loop or filter configuration.

C. Transient Analysis

Transient analysis, using a step or pulse input, was used to observe the large-signal settling behaviour of the amplifier and to extract the slew rate from the slope of the output during the fastest portion of the transition. Transient analysis complements the AC analysis because it captures large-signal, nonlinear effects — such as slewing — that a small-signal AC analysis cannot represent.

D. Power-Consumption Analysis

Power consumption was evaluated from the DC-OP and transient simulations by computing the product of the supply voltage and the total current drawn from the supply, consistent with P ≈ VDD × I_supply. This analysis verifies that the amplifier meets its low-power design objective and allows different bias-current iterations to be compared directly on a power basis.

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E. Phase-Margin / Stability Analysis

Phase margin was extracted from the AC phase response at the unity-gain crossover frequency, as described above. This analysis is required because DC gain and bandwidth alone do not guarantee stable closed-loop operation; a design with high gain and wide bandwidth but insufficient phase margin can still be unusable in a feedback application such as the active filter of Section X.

F. Unity-Gain-Frequency Measurement

The unity-gain frequency was read directly from the AC magnitude plot as the frequency at which the open-loop gain falls to 0 dB. This value is required both to characterize amplifier bandwidth and, in the filter application, to relate the OTA's transconductance to the achievable filter cutoff frequency.

G. Layout Implementation

After schematic-level verification, each amplifier was implemented as a physical layout in Cadence Virtuoso, as discussed in Section IX. Layout brings in the parasitic effects and matching issues that a schematic simulation does not capture.

H. LVS and Post-Layout Simulation

Each layout was checked against its schematic with LVS. For the 45 nm design, parasitics were then extracted from the LVS-clean layout and the AC, transient and power simulations were repeated on the extracted netlist. The 180 nm design has reached a clean LVS, and its extraction and post-layout simulation are still to be done.

I. Process-Corner Analysis

After layout, the 45 nm design was also simulated at the SS and FF process corners over a temperature range of −40 to 125 °C to see how far the gain, UGF, phase margin, slew rate and power move. Corner analysis has not yet been run on the 180 nm design.

VIII. SIMULATION RESULTS AND DISCUSSION

This section reports the simulation results of the two designs. The 45 nm design is the main design of this work and is reported first, including post-layout simulation and process corners. The 180 nm design follows at the schematic level, and the two are then compared. Results from the different 180 nm optimization iterations (Sections V and VI) are treated as observations from the optimization process and are not mixed into the final results below.

A. 45 nm Design (Main Design)

Table III gives the performance of the completed 45 nm design at the schematic stage, after layout extraction, and across corners. At the schematic stage the OTA clears the 60 dB target with 60.9 dB, and it also gives a phase margin of 75.8° and a UGF of 17.4 MHz, as shown in Fig. 3. The transient response in Fig. 4 settles cleanly, with slew rates of 7.59 V/µs rising and 7.29 V/µs falling in magnitude.

TABLE III: Performance of the 45 nm OTA

Parameter	Schematic	Post-layout	Corners*
Gain (dB)	60.9	61.0	58.9–61.3
UGF (MHz)	17.4	11.9	9.0–14.9
PM (°)	75.8	59.3	45.4–73.0
Slew rise (V/µs)	7.59	7.33	5.8–8.7
Slew fall (V/µs)	−7.29	−6.46	−7.6 to −5.5
Power (µW)	42.7	42.9	41.7–44.2

*Post-layout, SS/FF, −40 to 125 °C. VDD = 1.1 V, IBIAS = 10 µA, CL = 1 pF, 27 °C.

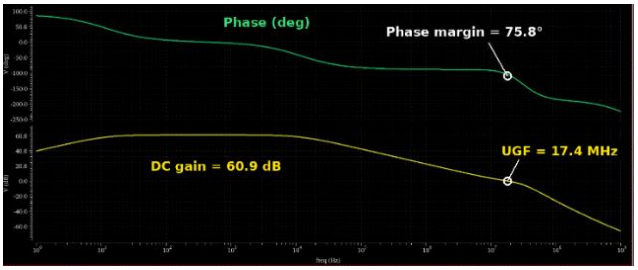


Fig. 3. AC response of the 45 nm OTA (schematic): DC gain 60.9 dB, UGF 17.4 MHz, phase margin 75.8°.

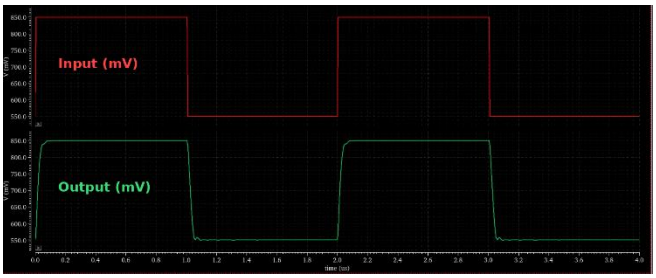


Fig. 4. Transient response of the 45 nm OTA (schematic).

After layout and LVS (Fig. 5), the extracted netlist gives essentially the same gain of 61.0 dB, but the UGF falls to 11.9 MHz and the phase margin to 59.3°. Power barely changes, at 42.9 µW. Across the SS and FF corners the gain moves by only about 2.4 dB, from 58.9 to 61.3 dB, so the DC gain holds up well against process and temperature. The phase margin is more sensitive and ranges from 45.4° to 73.0°, while the UGF ranges from 9.0 to 14.9 MHz. Dividing power by supply voltage gives a total supply current of about 39 µA at the schematic stage (42.7 µW at 1.1 V).

The drop in UGF and phase margin after layout fits with extra parasitic capacitance and resistance from the routing, which load the internal nodes and move the poles. The DC gain is mostly unaffected because it depends on transconductance and output resistance rather than node capacitance. A phase margin of 59.3° is close to the usual target of about 60° for fast settling with little ringing, but the worst-case value of 45.4° at the corners is below it, so the compensation network should be re-tuned or the layout made more compact to improve the worst corner.

B. 180 nm Design (Comparison Design)

The 180 nm design, biased at 20 µA from a 1.8 V supply, was simulated at the schematic level. Its AC response is shown in Fig. 6 and its transient response to a 10 mV, 100 kHz sinusoidal input in Fig. 7. Table IV gives its final performance. Layout, DRC and LVS are

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complete for this design, but post-layout simulation has not been run, so all numbers below are schematic-level.

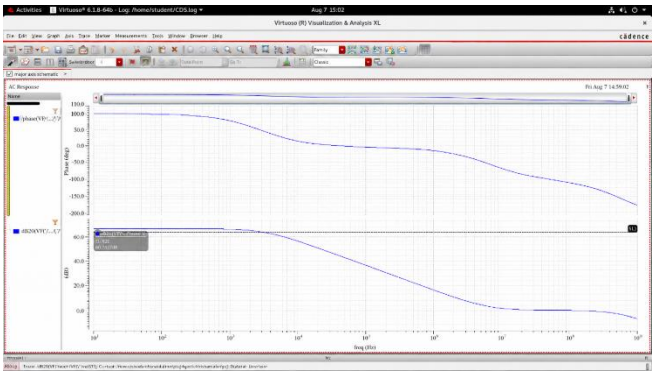


Fig. 6. AC gain and phase response of the 180 nm OTA (schematic).

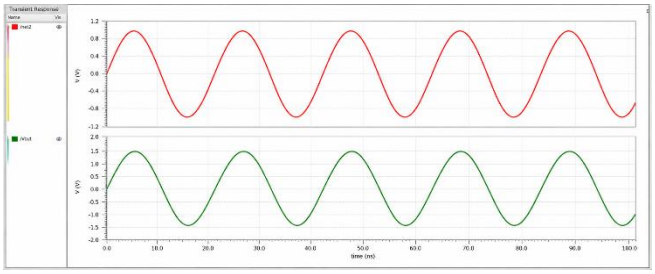


Fig. 7. Transient response of the 180 nm OTA to a 10 mV, 100 kHz sinusoidal input (top) and the corresponding output waveform (bottom), showing linear amplification.

TABLE IV: Final simulated performance of the 180 nm OTA (schematic)

Parameters	Final Simulated Value
Technology	180 nm CMOS
Supply Voltage	1.8 V
DC Gain	66.01dB
Unity-Gain Frequency	10MHz
Phase Margin	140 °
Power Consumption	36 uW
Load Capacitance	1 pF
Compensation Capacitance	9 pF

C. Comparison of the Two Designs

Table V compares the two designs at the schematic stage, which is the only stage where both have results, and shows how far each has been taken. Both designs clear the 60 dB gain target. The 180 nm design gives about 5 dB more gain and uses less power (36 µW against 42.7 µW), while the 45 nm design reaches the higher UGF (17.4 MHz against 10 MHz) at a much lower supply voltage (1.1 V against 1.8 V). The extra gain at 180 nm is expected, because longer channels give each transistor a higher intrinsic gain. Dividing power by supply voltage shows that the 45 nm design draws about 39 µA in total from a 10 µA bias, while the 180 nm design draws about 20 µA from a 20 µA bias.

TABLE V: Comparison of the 45 nm and 180 nm designs

Parameter	45 nm	180 nm
Supply voltage	1.1 V	1.8 V
Bias current	10 µA	20 µA
Load capacitance	1 pF	1 pF
Compensation capacitance	1pF	9 pF
DC gain (schematic)	60.9 dB	66.01 dB
UGF (schematic)	17.4 MHz	10 MHz
Phase margin (schematic)	75.8°	**140°**
Power (schematic)	42.7 µW	36 µW
Layout and LVS	Done, LVS clean	Done, LVS clean
Post-layout simulation	Done	Not yet
Corner analysis (SS/FF)	Done	Not yet

Only the 45 nm design has post-layout and corner results, so for now the effect of layout on phase margin can be judged only there. How much the 180 nm design loses after extraction is the main open question for the comparison.

IX. LAYOUT DESIGN AND VERIFICATION

Both designs were laid out in Cadence Virtuoso after schematic-level verification. Layout turns the transistor-level schematic into physical geometry and brings in the parasitic resistances and capacitances, device matching and routing effects that an ideal schematic simulation leaves out.

A. 45 nm Layout

The 45 nm layout (Fig. 5) was drawn with the input pair and the current mirror placed for good matching and with compact routing. It is LVS clean, meaning that the netlist extracted from the layout matches the schematic. The parasitics extracted from this layout were used for the post-layout and corner results in Section VIII-A.

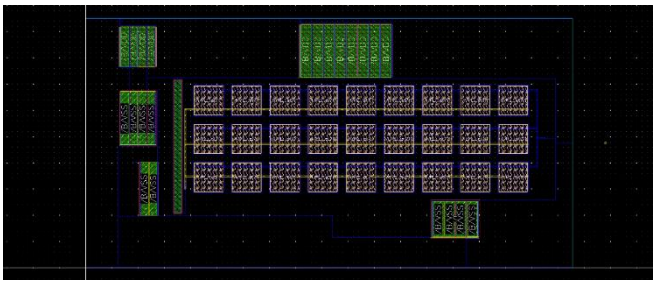


Fig. 5. Layout of the 45 nm OTA (LVS clean).

B. 180 nm Layout

Careful placement of the transistors is needed to preserve the matching assumed in the schematic. The input transistors of the differential pair were laid out with attention to matching, since any mismatch between them adds input-referred offset and degrades common-mode rejection. The current-mirror devices were laid out with matched geometry, the same orientation and close spacing, to reduce mismatch in the mirrored bias currents.

Routing was planned to minimize parasitic resistance and capacitance on sensitive high-impedance nodes, particularly the first-stage output node and the Miller compensation path, since parasitic capacitance at these nodes directly affects the pole locations established in Section VI. Symmetry in the overall floorplan — particularly around the differential signal path — was maintained where possible to further

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reduce systematic mismatch and to keep the layout-induced parasitics balanced between the two halves of the differential pair.



Fig. 8. Layout of the 180 nm OTA.

Design rule check (DRC) and layout-versus-schematic (LVS) verification are required steps before a layout can be called complete. DRC checks that the geometry follows the foundry's manufacturing rules, and LVS checks that the netlist extracted from the layout matches the schematic. The 180 nm layout passes both checks.

DRC result:

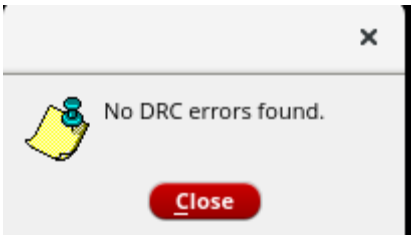


Fig. 9. DRC result of the 180 nm layout (no DRC errors found).

LVS result: The layout matches the schematic and LVS is clean.

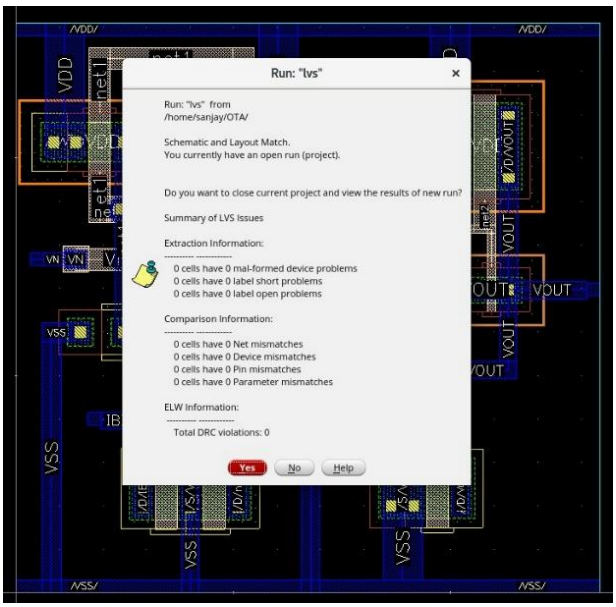


Figure 10: LVS result of 180nm layout

With LVS clean, the 180 nm design is ready for parasitic extraction. Extraction and post-layout simulation of the DC, AC and transient responses, which would be expected to show some loss of gain, bandwidth and phase margin from the added parasitic loading, are the next step.

X. ACTIVE LOW-PASS FILTER APPLICATION

The proposed OTA is intended for use as the active transconductance element of an OTA-C (Gm-C) active low-pass filter. In this class of filter, the OTA converts an input voltage into an output current proportional to its transconductance gm, and this current is used to charge an integrating capacitor C at the output node. Because the OTA behaves as a voltage-controlled current source rather than a voltage amplifier in this configuration, no resistive feedback network is required to set the filter response — the RC-like time constant of a conventional active filter is instead realized as a gm/C ratio.

For a basic first-order OTA-C low-pass section, the cutoff frequency is given by

$$fc = gm / (2\pi C) \qquad (7)$$

which shows that the cutoff frequency scales directly with the OTA's transconductance and inversely with the value of the integrating capacitor. Because gm is itself a function of the bias current (Section IV), this relationship also means that the filter's cutoff frequency can, in principle, be tuned electronically by adjusting the OTA's bias current — a useful property in applications requiring a programmable or process-compensated cutoff frequency.

The low-power characteristics of the proposed OTA are directly relevant to this application: because gm can be set with a comparatively small bias current (Section V), the resulting Gm-C filter can achieve its target cutoff frequency without the static power overhead associated with resistor-based active-RC filters, and without requiring large integrating capacitors, which would otherwise consume significant silicon area at low cutoff frequencies. OTA-C implementations are also well suited to fully integrated, tunable filters, since the cutoff frequency can be adjusted post-fabrication through the bias current rather than through fixed passive component values.

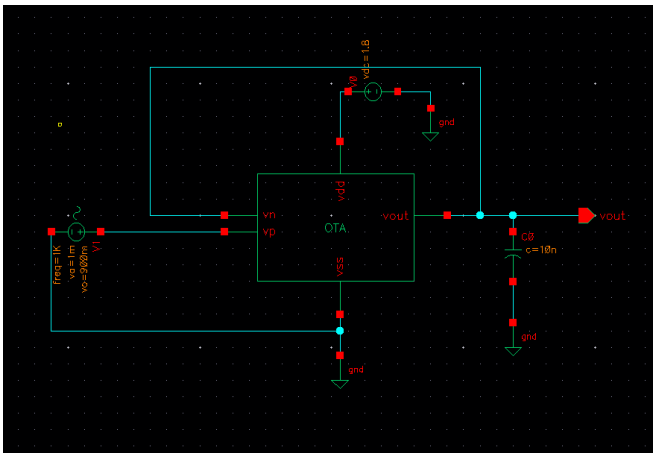


Figure 11: Schematic of the proposed first-order Gm-C (OTA-C) active low-pass filter

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XI. COMPARISON WITH EXISTING WORKS

TABLE VI — Comparison with Existing Two-Stage OTAs

Work	Technology	Supply	Gain	UGF / GBW	Phase Margin	Power		[3]	180nm	1.5 V	120 dB	372.45 MHz	81°	102 uW	Two- stage telescopic OTA
[1]	180nm	1.8 V	51.4dB	18.93 MHZ	65.96°	1.25 mW	Two-s	This work (45 nm)	45nm	1.1 V	60.9 dB	17.4 MHz	75.8°	42.7 µW	Two-stage OTA with R-C Miller compensation
[2]	180nm	1.8 V	90.2 dB	12.05 MHz	68.2°	-	Two-s driv	This work (180 nm)	180nm	1.8 V	66.01 dB	10 MHz	140°	36 uW	Two-stage OTA with miller compensation

XII. CONCLUSION

This paper presented a low-power two-stage Miller-compensated CMOS OTA designed in 45 nm technology, with the same architecture built in 180 nm technology for comparison. The OTA has a differential first stage with a current-mirror active load and a common-source second stage, stabilized by Miller compensation. The 45 nm design, biased at 10 µA from a 1.1 V supply, was taken through the complete flow of schematic, layout, LVS, post-layout simulation and process-corner analysis. It gives 60.9 dB gain, 17.4 MHz UGF, 75.8° phase margin and 42.7 µW at the schematic stage, and 61.0 dB, 11.9 MHz, 59.3° and 42.9 µW after layout, with the gain staying between 58.9 and 61.3 dB across SS and FF corners from −40 to 125 °C. The 180 nm design was optimized through a bias-current sweep from 5 µA to 30 µA and settles at 20 µA. At the schematic level it gives 66.01 dB gain at 36 µW, and it has been taken through layout, DRC and a clean LVS. The role of the Miller compensation capacitor in pole splitting, and its trade-off against bandwidth and slew rate, was analyzed for both designs. The OTA is a suitable transconductance element for a first-order OTA-C low-pass filter, based on the standard fc = gm/(2πC) relationship. Overall, this work shows a practical, trade-off-aware way to design a low-power two-stage OTA at two technology nodes, with the 45 nm design verified through post-layout simulation and corners.

FUTURE SCOPE

The next step is to extract the 180 nm layout and run its post-layout simulation, including corners, so that it can be compared with the 45 nm design at the same stage. The compensation network and layout of the 45 nm design can also be re-tuned to recover phase margin at the worst corner, and Monte Carlo analysis can be added for both designs. Beyond this, deep-learning and AI-based optimization techniques can be explored to optimize transistor sizing, bias current and compensation values, giving a better balance between gain, bandwidth, power consumption, phase margin and area. The proposed OTA and active low-pass filter can also be extended to tunable filters, biomedical systems and other low-power signal-processing applications.

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