Low Power Ternary Analog to Digital Converter

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***Abstract*—In this paper the architectures of the two digit and the three digit ternary analog to digital converter (T-ADC) are designed, and their performance are compared with their respective binary counterparts. The analog comparator and the CMOS logic gates are used in the design of the T-ADC. The output is expected that, a ternary ADC performs better than a two bit binary ADC in terms of dynamic range and power consumption. Thus T-ADC is proved to be a better choice.**

Keywords— Ternary ADC; comparator; encoder; high resolution; step size.

I. INTRODUCTION

High speed and high resolution converters are high demands of the audio and the video signals of the multimedia communication. The fastest way to convert analog signal to digital signal is achieved by direct conversion analog to digital converters(ADC) or flash ADC. The high power dissipation and the large die size are the major drawbacks of the Flash ADCs though they are best suited for large bandwidth applications. In this work, the use of the ternary or base-3 logic system in the design of converters is proposed over the conventional binary logic system based converters. It is observed that in the implementation of the logic function there is reduction in the number of interconnections required which serves as a major advantage with concern for Flash type ADCs. Besides the serial and serial-parallel operations can be performed at high speeds using ternary systems [1][2][3].Comparatively more information can be transmitted over a given set of lines as the ternary digit or a trit contains $\log_2 3$(about 1.58496) bits of information[5-8].The ternary system gain importance in various applications like memories, arithmetic circuits, communications and signal processing[4]. Also the emerging standards of digital communication and signal processing requires analog and digital converters. In this contribution, the T-ADC suitable for C-MOS digital processes is developed.

The organization of the paper is as follows,

Section II introduces T-ADC basics. Section III gives the design and the implementation of the ADCs. Section IV presents the simulations and output analysis. Section V includes the conclusion followed by the reference section.

II. T-ADC BASICS

BASIC ELEMENTS OF A TERNARY ADC

This section describes the design of basic gates used in the construction of a T-ADC. The CMOS logic in 180 nm technology is used in the designing of the logic gates that are present in this section. Inverters, NOR gates and NAND gates together make the CMOS ternary logical family.

A. Ternary Inverter

A Ternary Inverter circuit is shown below in the Fig.1.

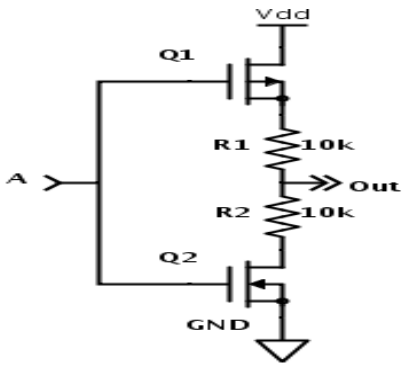

Fig.1. Ternary Inverter

Ternary inverter consists of a PMOS and a NMOS connected via R1 and R2 resistors. These resistors are used to provide the intermediate drop between VDD and VSS. The source of

PMOS is connected to VDD and the source of NMOS is connected to VSS. The output for a ternary input X is defined by the equations:

$$\overline{X} = (2 - X) \qquad (1)$$

B. Ternary NOR

The two input ternary NOR circuit is shown below in the Fig.2

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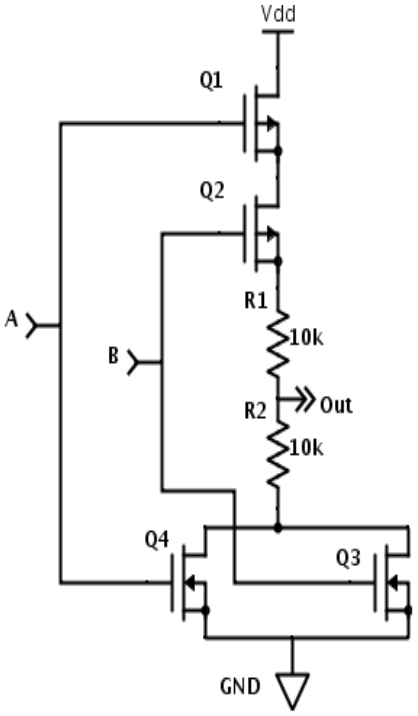

Fig.2. Ternary NOR

It consists of two PMOS transistors in series and two NMOS transistors in parallel connected via resistors R1 and R2. The output of the ternary NOR gate for ternary inputs X and Y is given by:

$$\overline{(X \text{ or } Y)} = \{\overline{\max(X, Y)}\}$$

C. Ternary NAND

The two input ternary NAND circuit is shown in the Fig.3. It consists of two NMOS transistors in series and two PMOS transistors in parallel connected by resistors R1 and R2.

The output of the ternary NAND gate for ternary inputs X and Y is given by:

$$\overline{\quad\quad}\quad\overline{\quad\quad\quad}$$
$$(X \text{ or } Y) = \{\min(X, Y)\}$$

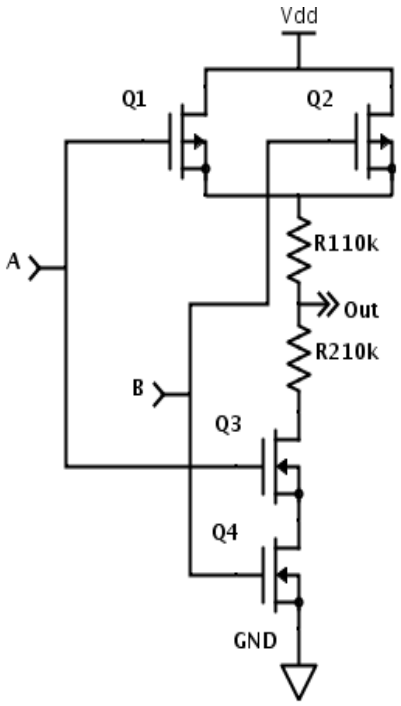

Fig.3. Ternary NAND

The ternary AND and OR gates are constructed by feeding the outputs of ternary NAND and NOR gates to a ternary Inverter.

III. Design And Implementation

A Flash ADC has architecture involving a sample and hold circuit which samples the continuous time input signal. These flat samples are then fed to a comparator which compares the sampled values with the predefined voltage levels determined by a resistor network. The output of the comparator is either valued logic High or logic Low depending on the comparison result. These values are then used by an encoder to decide a proper digital value for the corresponding voltage of the sampled input signal. The Flash architecture used in this work to build an ADC is as shown in the Fig. 4.

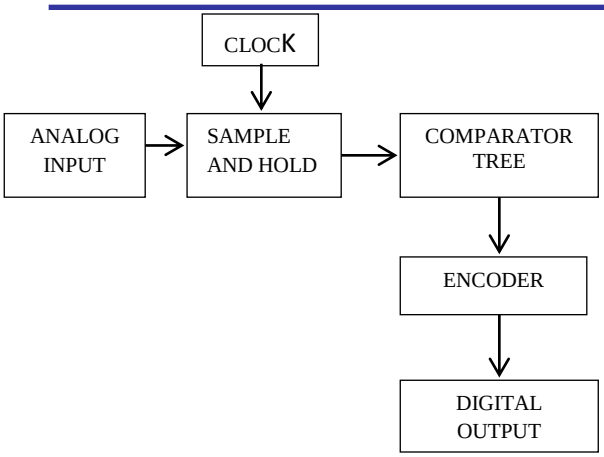

Fig.4. Architecture of a Flash-ADC

A. *Comparator Design*

A comparator, shown in Fig. 5, is a circuit which has a binary output based on the comparison between two input values. It can be defined mathematically as:

$$V_O = \begin{cases} V_{OH}, \text{ if } V_{in+} > V_{in-} \\ V_{OL}, \text{ if } V_{in+} < V_{in-} \end{cases} \quad (4)$$

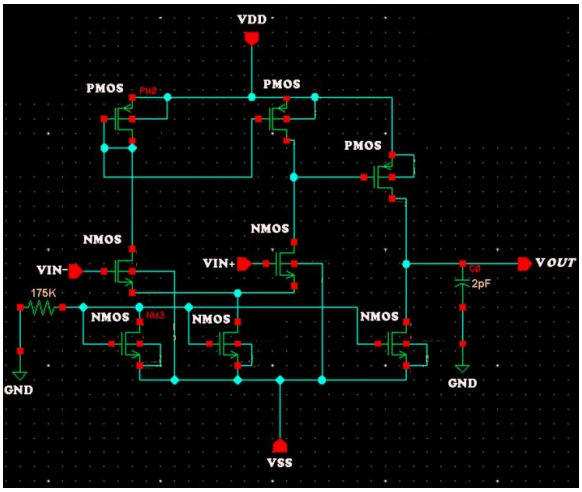

Fig.5. Comparator with NMOS input drivers

B. *Two digit ternary ADC*

A two digit ternary Flash ADC has 3_2=9 quantization levels, and hence, uses 8 comparators. The output of the comparator is fed to the encoder. The encoder circuitry is completely built using ternary logic gates such as ternary AND, OR and INV. Inputs to the encoder are nothing but the outputs of the comparator.

In 180 nm technology, the ternary state Logic 0 is represented as negative value, Logic 1 as 0 and Logic 2 as positive value.

The output logic equations for the encoder are as follows:

$$Y_1 = C_6, C_5 + 1^*C_1, C_2, C_3 \quad (5)$$

$$Y_0 = C_8, C_7 + \overline{C_6}, C_5 + \overline{C3}, C2 + \overline{\quad} \overline{\quad} \overline{\quad} \quad 1^*(C_2,C_1+C_5,C_4+C_8,C_7) \quad (6)$$

$C_1, C_2 \ldots\ldots C_8$ are the outputs of the comparators 1, 2…8 respectively, and Y_1 and Y_0 are the ternary outputs.

Fig. 6. show the complete implementation of the two digit ternary analog to digital converter with Y_1 as MSB and Y_0 as LSB.

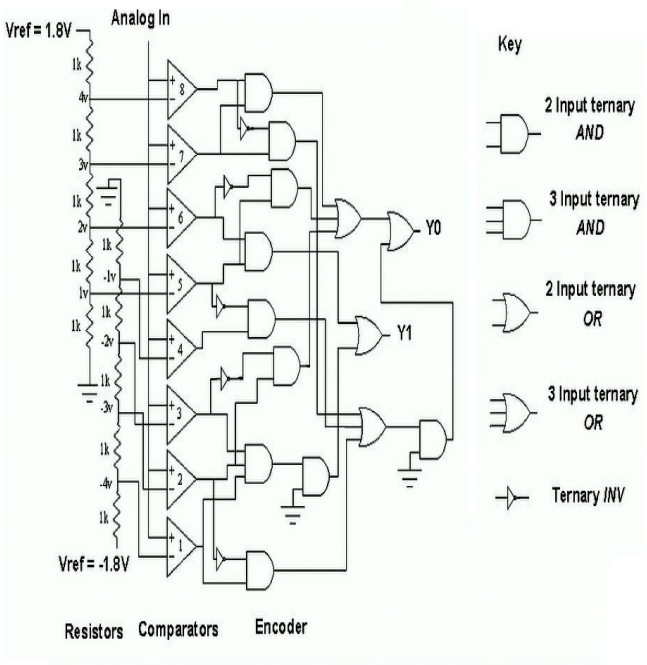

Fig.6. Two digit ternary Analog to Digital Converter

IV. SIMULATION RESULTS AND ANALYSIS

I am implementing this project by using base paper. Implementation is in the progress.

V. CONCLUSION

In this paper, design of a three digit ternary Parallel or Flash ADC is done. The input signal voltage is compared with the reference voltage using the hign precision comparator. Output of this comparator is fed to the encoder. Designed ternary ADCs are compared with the existing binary ADCs. It is expected to obtain higher quantization levels. Similarly, the step size of ternary ADCs is expected to be less than half that of the corresponding binary ADCs. Also, the dynamic range of the ternary ADCs is almost twice that of binary ADCs making them suitable for applications in wideband communication.

VI. REFERENCES

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