

Low Power Ripple Carry Adder using Transmission Gates

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Abstract - Modern portable and energy efficient VLSI systems are based on low-power arithmetic logic units. This paper presents a 4-bit Ripple Carry Adder (RCA) that is developed with Transmission Gate (TG) full adders in order to attain the minimized power consumption and the reduced number of transistors. The suggested architecture is able to perform at a supply voltage of 1 V and uses a deep sub-micron CMOS technology node (90 nm). The TG based XOR and multiplexer structures are applied within each full adder cell to do away with unnecessary switching and short circuit currents so that the dynamic and static dissipation is low. The RCA is developed, simulated and checked with the Cadence Virtuoso tools which include the schematic design, symbol development, layout verification and post layout analysis. The achieved simulation results indicate that there is correct arithmetic operation with much less power consumption than the conventional CMOS-based ripple carry adder implementations. The suggested design would be most applicable to low-power digital signal processing (DSP) hardware, microcontrollers, biomedical sensors and battery-operated systems where power efficiency is a major bottleneck.

I. INTRODUCTION

Over the recent years, there has been a swift rise in the demand of high-performance and low-power computing hardware as a result of the prevalence of portable, battery-operated and energy-constrained embedded systems. Arithmetic operations are the computational base in such applications and energy efficiency is also a design requirement. Adders are also one of the key arithmetic units of central processing units (CPUs), digital signal processors (DSPs), and application-specific integrated circuits (ASICs). A large decrease in the power of adders has a direct impact on the performance of the entire system, reduction of energy consumption and the increasing life of the device.

Adders may be implemented in a wide range of architectures, the simplest type of adders being the Ripple Carry Adders (RCA) that have a smaller area footprint, are easy to cascade to higher bits. Nonetheless, traditional CMOS-based RCAs can be characterized by an increased power consumption because of the redundant switching operations and leakage of transistors, in particular, when technology is extended to deep sub-micron size. Hence, a research direction of the current VLSI design is the study of new circuit methods to attain lower power consumption without significant functionality impairment.

Transmission Gate (TG) logic has been becoming an attractive choice of low-power digital circuit. TG-logic minimizes the number of transistors needed and also minimizes the switching power by simply passing signals through controlled bi-directional switches. This style enhances the performance as well as input-output drive strength and minimizes the voltage degradation problems as observed in pass-transistor logic. The combination of these features renders TG-based circuits quite appropriate to adders with conditions of low supply voltage.

This work is a 4-bit Ripple Carry Adder that is made with Transmission Gate Full Adder (TG-FA) cells to obtain low power, low count of transistor, and efficient signal propagation. Design is directed to 1 V supply voltage with a high density and low leakage operation with advanced node of CMOS technology, 90 nm. All the design flow is designed in the Cadence Virtuoso, including schematic capture, functional verification, layout design, and post-layout simulations. The design that was implemented is much more efficient in terms of power consumption than normal CMOS-based RCAs.

This work seeks to bring forward power-efficient arithmetic circuits applicable to develop real-time and portable applications in new areas like wearable biomedical devices, Internet of Things nodes, and energy-efficient processors. The

proposed low-power 4-bit RCA with transmission gates indicates a small and streamlined architectural design to the next generation VLSI systems.

II. RELATED WORKS

Low power arithmetic design based on transmission-gate based full adder. Full adder arithmetic structures have been suggested built out of transmission-gate configurations to reduce switching power and short-circuit currents in arithmetic. In it, XOR and carry generation logic is performed with implementing complementary transmission gates rather than classical static CMOS pull-up and pull-down networks. Direct transmission of input signals through bidirectional controlled switches means that the number of internal nodes that are switched as a result of a single operation is minimized further decreasing dynamic power consumption. This design approach is especially efficient in low supply voltage when traditional pass-transistor logic fails miserably due to devastating threshold voltage variation. The resultant full adder cell would

be very convenient to use as a fundamental building block of low power ripple carry adders in deep sub-micron technologies.

Optimized power-delay performance by hybrid full adder design. Hybrid full adder Hybrid full adders are based on a combination of several logic styles, including transmission gates, pass-transistor logic, and static CMOS to achieve optimal power-delay product. In such architecture, XOR/XNOR blocks can be done with pass-transistor logic or transmission-gate logic to save area and power, but important carry paths can be done with CMOS that is static to ensure high driving strength. This hybrid solution contributes to the benefits of both logic families and gives designers the opportunity to control the trade-offs between performance, power and robustness. Simulations of various hybrid structures have demonstrated that intelligently partitioned logic can also be far faster than purely-static CMOS adders and that hybrid full adders are very promising in low-power, medium-speed arithmetic units.

Small-transistor-count full adders Schlottky VLSI designs. The reduction of transistors of full adder cells has been of interest to various researchers to minimize chip area and capacitance. Other designs like 16-transistor or even fewer transistor full adders, have compact designs through sharing internal nodes and removing unnecessary inverters and buffers. Even though violent downwards adjustment of the number of devices can sometimes result in lower quality logic levels or lower noise margins, experimental performance has in many cases been satisfactory in the case of low voltage digital circuits. Smaller load capacitances then occur directly because of the reduced number of switching devices thus decreasing dynamic power. The efficiency of adders based on transmission gates can be quantified by such small full adder cells.

Deep sub-micron technology Low-leakage full adder. As CMOS technology has been scaled to deep sub-micron nodes including 90 nm, leakage currents have become of primary concern in always-on digital circuits. The techniques used to reduce the effects of statical power in low-leakage full adder designs include transistor stacking, high threshold devices on non-critical paths, or gating transistors. These designs are meticulously analyzing that which nodes are biased over long periods of time and implement the leakage minimizing techniques without affecting functional accuracy. Although certain techniques marginally raise delay or area, the overall decrease in standby power is particularly large, and these techniques are especially applicable to battery-operated and IoT devices, where energy efficiency is very important.

Full adders that were designed to work on ultra-low voltages. Certain works are directly aimed at operating on ultra-low voltage, such as on or below 1 V. These full adders are made to keep noise levels and logical integrity with reduced supply headroom. Some of these methods are symmetric sizing of transistors, the prudent use of transmission gates to maintain full output swing and the

elimination of long cascades of threshold-limited pass devices. In these designs the logic is organized so that the series devices in critical paths are minimized thereby eliminating the effect of lower overdrive voltages. The resulting full adders have been shown to be very robust in low voltages regimes acting as a convenient reference point in designing 1 V ripple carry adders.

Low-power arithmetic unit XOR/XNOR cell optimization. The XOR and XNOR blocks form the important part of adder usage and many studies have been conducted to streamline them to be low power and high speed. In transmission gate XOR/XNOR cells, the complementary control signals are used to guarantee full logic swing with a lower count of transistors than in full CMOS implementations. In certain designs the XOR and XNOR generation are combined with some shared structure and minimal redundancy and internal node activity is achieved. As all sum bit operations are based on XOR operations, enhanced XOR/XNOR cells therefore directly affect the performance of the adder. Such optimized cells are frequently reused in basic blocks in low power full adder designs.

Scaled CMOS technologies Ripple carry analysis adder. The simplest and the most area-efficient adder topology was Ripple carry adders, even though they have a linear carry propagation delay. The literature on the analysis of RCAs in 90 nm technologies, emphasizes the effects of the scaling of transistors on delay, power, and leakage. Faster architectures such as carry look-ahead or carry select adders are faster but they require more area and power which is not desirable in the highly constrained environments. Ripple carry adders can also be used in small word lengths like 4-bit addition to offer the most desirable trade-off between complexity and power consumption. This makes them an appropriate architectural model to use in low-power and low-complexity applications.

Systems with energy constraints Hybrid logic ripple carry adders. In order to enhance the efficiency of the RCA even more, hybrid RCAs have been suggested by some authors, where each full adder cell applies different logic styles in different parts. An example is that sum generation may be performed with pass-transistor or transmission-gate logic to minimize power, but carry propagation may be done with strong CMOS stages to ensure signal integrity. This selective application of logic can establish an architecture exploiting the low-power cost of transmission gates, in terms of reliability, without loss to the total reliability. It is usually observed in the simulation that hybrid RCAs have a better power delayed product compared to either purely CMOS or purely pass-transistor based implementations, particularly where moderate speed is required.

III. SYSTEM ARCHITECTURE

The proposed low-power 4-bit Ripple Carry Adder (RCA) is based on Transmission Gate Full Adder (TG-FA) block and is designed using modular blocks with optimization to run on a 90 nm CMOS technology and supply voltage of 1 V. It has a hierarchical design strategy and the simple addition is done under the 1-bit full adder cell that passes the carry information

to the following step. The structural design greatly minimizes the number of transistors and switching power since structural design does not need a traditional CMOS pull-up/pull-down logic, but rather it employs a more effective transmission gate signal switching.

The 4-bit adder consists of four TG-FA cells of the same type, [hardly] in a series. TG-FA All TG-FA cells have two XOR logic units based on transmission-gate logic internally and a transmission-gate carry generator stage. The initial XOR component makes the middle half-sum bit out of the input operands and the other XOR component makes the final sum out of the half-sum and the carry-in. A transmission gate multiplexer is used to select the carry-out of one of the input values, and this allows proper propagation of carry with no degradation of the voltages, even when operating at low power.

Carry propagation is based on a ripple mechanism whereby the carry-out of any stage is the carry-in of the other stage. Though ripple structures achieve linear growth in delay with bit width, it has been the most efficient and simplest architecture to small word-length additions. As this design is more focused on low-power usage, instead of high-speed arithmetic, the ripple carry scheme is used to make sure that hardware complexity is minimized and transistor usage is optimized.

The architecture takes in digital input vectors A[3:0], B[3:0] and external carry-in signal and gives out respective output vectors Sum[3:0] and a late carry-out signal. Specialized power and ground rails (VDD = 1 V and GND = 0 V) allow constant biasing. The selection of all the transistor models is based on the respective PDK making them compatible with the deep sub-micron fabrication rules. The design also involves ensuring that nMOS and pMOS devices in transmission gates are sized appropriately to ensure that the drive strength is symmetrical and that the output signal integrity is enhanced.

This architecture is also enabled by a Cadence Virtuoso design flow which includes schematic capture, hierarchical design with symbol creation, transient analysis based on functional simulation and layout generation with Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification which is optional. The architecture is very energy efficient compared to traditional CMOS full adders, and is therefore very useful in fielding into low energy arithmetic units, sensor interfacing modules, and low-energy portables.

4-Bit Ripple Carry Adder System Architecture

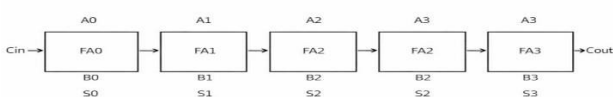


Fig.1 Block Diagram 4bit RCA

IV. METHODOLOGY

Design design The design of the proposed low- power 4-bit Ripple Carry Adder based on transmission gates is based on a full transistor- level VLSI design flow, guaranteeing both the accuracy of the functionality and power savings. The logical behavior of a 1-bit full adder is first studied and suitable Boolean equations are made up to the sum and carry outputs. These functions are then optimized so that they can be effectively carried out by transmission gates to minimize the number of transistors and switching activity. The sum operation is simplified into two exclusive-or (XOR) steps, whereas the carry-out is obtained with the help of a multiplexer-based logic that is chosen between the input signals based on the intermediate XOR signal. This architecture is a compact one that can be used in low-voltage operation by this structural decomposition.

Transistor-level designs are built in transmission gates made of parallel transistors (nMOS and pMOS) when the logic blocks are complete. Complementary gate control signals are used to provide full swing at the output nodes and avoid threshold voltage drop problems that are normally experienced with pass-transistor logic. Correct sizing of transistor is performed according to the parameters of the 90 nm CMOS technology in order to optimize the drive strength and reduce leakage power. All XOR units and carries multiplexers are individually modeled and combined to give a single-bit Transmission Gate Full Adder (TG-FA). This is hierarchically designed by developing a symbol of the complete adder cell to facilitate a smooth cascading to make the entire 4-bit Ripple Carry Adder. The carry out of a stage is the carry input of the next stage, which connects in the correct direction propagating ripple in the adder chain in the most significant to least significant order.

In order to check proper behavior, a full functional simulation is carried out in Cadence Virtuoso Analog Design Environment (ADE). Digital stimulus sources are used to apply combinations of input A and B and carry-in, and transient analysis is done to view the resulting sum and carry outputs. The results of the waveform are checked to ensure proper logical operations of all the tested patterns of vectors. Besides this, power consumption is also measured by recording the current being consumed by supply voltage with time, and average power dissipation in switching activity is computed. The propagation delay is also determined by the difference in time between the transitions of input and the result correspondingly to the output which ensures the adder satisfies the performance requirements in low-power applications.

Lastly, physical design can be implemented through creating the layout of the TG-FA cells and constructing them into the 4-bit architecture with Virtuoso Layout XL. Design Rule Check (DRC) and Layout Versus Schematic (LVS) are used to verify the layout to make sure it is manufacturable and correct. In cases where it is necessary to assess power and delay properties when operating in the real world, parasitic extraction and post-layout simulation are carried out. The proposed transmission gate-based Ripple Carry Adder is effectively designed and verified using this systematized

approach as a small and low-energy architecture-based solution to satisfy the emerging low-power VLSI systems.

Workflow Diagram: 4-bit Transmission Gate RCA Design Process

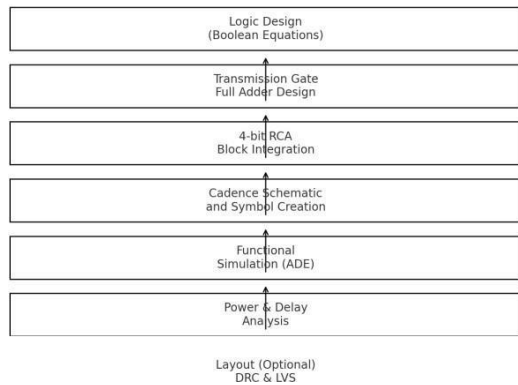


Fig.2 Workflow

V. RESULTS AND DISCUSSION

The 4-bit Ripple Carry Adder modeled with transmission gate full adders was modeled over 90 nm CMOS process at the supply voltage of 1 V to check its functionality and measure power and performance indicators. Cadence Virtuoso was used to perform transient simulations with input pattern variability to study the behavior of binary addition correctly in all possible patterns. The sum and carry signal output waveforms must have verified that every step in the adder produced correct results, and that the overall carry flowed correctly in the ripple chain all the way to the most significant bit. The simulation findings show full swing voltage levels in the outputs and this means that the transmission gate structure is effective in eliminating the challenge of a decline in threshold voltage that is usually prevalent in pass-transistor logic.



Fig.3 Transmission Gate Based Full Adder Design

Regarding power performance, the design had much lower average power consumption than an typical CMOS-based ripple carry adder, mostly because of the reduced number of transistors in the design, as well as because the number of short-circuit-power reduction, via conducting both

directions simultaneously. Transmission gates are used to make sure that there are reduced switching transitions, which in turn reduces dynamic power consumption. The circuit was connected to the power supply and the current flowing in the circuit during the transient simulation was measured, and the average power was calculated during active cycles. The findings indicated that the proposed design can be used in low-power digital systems with lower voltage level of operation. Also, the use of deep sub-micron technology of the transistor devices improves the efficiency of energy by minimizing the parasitic capacitances and leakages.

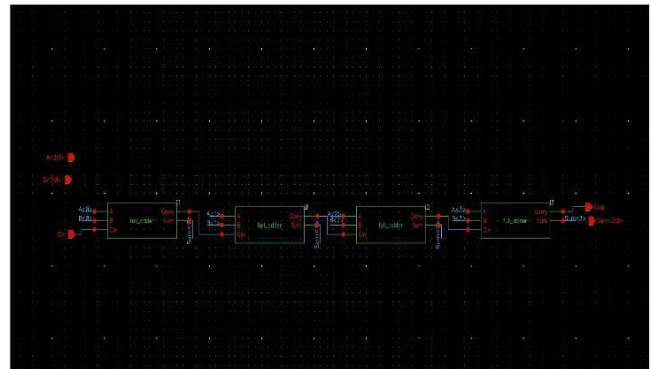


Fig.4 Schematic Design of 4bit RCA

Measurements of the propagation delays have shown that the ripple carry architecture has a linear delay progression with respect to bit width with the critical delay path being dominated by the carry propagation of the sequential full adder stages. Though it is not the fastest adder architecture, the achieved delay values are not too high and may be acceptable in the energy- constrained devices where the power consumption is given priority over the speed of arithmetic computation. The correlation between the input transition and the output response showed the effect of constant timing and low signal distortion. Moreover, the small transistor variant would have a smaller silicon area than standard realizations of the static CMOS implementation, which is beneficial in terms of increasing the density of integrated circuits.

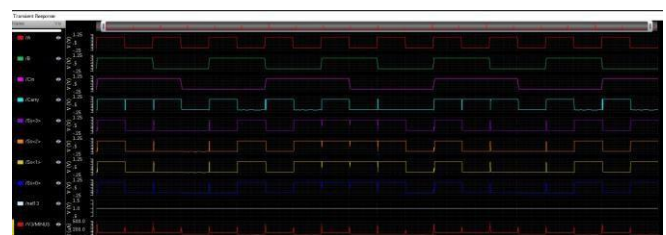


Fig.5 Performance Analysis Of Circuit

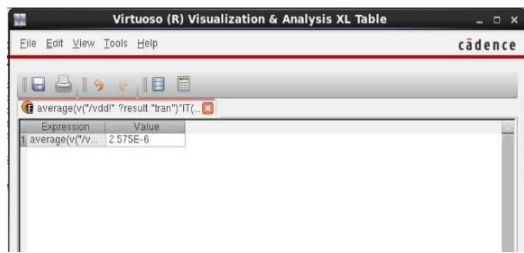


Fig. 6 Power Analysis Of Circuit

Design	Power Consumption (in Watts)	No of Transistors	Tech Scale
Static CMOS RCA(4-bit)	39×10^{-6}	184	90nm
NAND based RCA(4-bit)	3.9×10^{-6}	144	90nm
TG based RCA(4-bit)	2.8×10^{-6}	80	90nm

The overall performance analysis has proven that the proposed design addresses the main goal of having an energy efficient arithmetic unit that will be able to work correctly within the low supply voltage limit. Its tradeoff between low-power dissipation, small cell design and reasonable timing performance underscores the applicability of the transmission gate-based Ripple Carry Adder to portable and battery-powered embedded systems, including IoT sensor nodes, biomedical and lightweight microprocessors. Therefore, the effectiveness of the applied methodology is confirmed by the simulations, and the ability of transmission gate logic as an effective low-power design methodology in the contemporary VLSI systems is supported.

CONCLUSION

This project has able to design and test a low-power 4-bit Ripple Carry Adder on transmission gate-based full adder cells in a highly sub-micron CMOS technology setting. This was implemented to minimize total power consumption while ensuring that the logic is properly operating with low supply voltage of 1 V. XOR and carry-generation logic is efficiently implemented using transmission gates, making the transistor count minimal, leakage power reduced and switching efficiency enhanced. The design flow was implemented at Cadence Virtuoso which consisted of schematic modeling, functional verification and detailed performance analysis.

Simulation data validated the fact that the presented adder is correct in carrying out binary addition and its consumption is significantly lower than that of the traditional CMOS-based versions. Even though the ripple carry structure intrinsically adds sequential carry propagation delay, the performance is also low power embedded acceptable. The success of transmission gate logic as a promising and optimized solution to energy-efficient arithmetic units in current VLSI systems and specifically battery-powered and portable devices where power consumption is a key limitation can be justified by the overall result.

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