Low Power Process Variation Tolerant Schmitt Trigger Based SRAM

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Abstract

Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance at the expense of increased leakage current. Supply voltage scaling is an effective way of reducing dynamic as well as leakage power consumption. However the sensitivity of the circuit parameters increases with reduction of the supply voltage. SRAM bit- cells utilizing minimum sized transistors are susceptible to various random process variations. Hence reducing the memory operating supply voltage, while maintaining the yield is becoming extremely challenging in nano scale technologies. This paper presents solution for high power dissipation of SRAM by reducing the leakage current and increasing the Stability compared with Basic 6T SRAM. In this paper the Schmitt Trigger (ST) based SRAM is proposed to reduce the power consumption. The Schmitt Trigger based SRAM bit cell, feedback is provided by separate control signal where in feedback is provided by the internal nodes.

1. Introduction

The power requirement for battery operated devices such as cell phones and medical devices is even more stringent with the scaling of the device dimensions. Reducing the supply voltage reduces the dynamic power quadratically and leakage power linearly [1]. Hence, supply voltage scaling has remained the major focus of low-power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [2]. However, the reduction in supply voltage may lead to increased memory failures such as read-failure, hold failure and write-failure [3], [4]. For a stable SRAM bit cell operating at lower supply voltages, the stability of the inverter pair should be improved. The proposed Schmitt trigger based differential bit cell having built-in feedback mechanism for improve the stability of the inverter pair [4].

2. Six Transistor SRAM cell (6T):

The 6T memory cell implementation in its simplest form is shown in Figure 1 [5]. The cell is made up of two access transistors (M5 and M6) and a latch formed by two cross coupled inverters (M1, M3 and M2, M4). The pass transistors which are connected to two complementary bit lines BL and BLB are controlled by the word line signal WL. They act as transmission gates providing the bidirectional access between the latch and the bit lines. Before the read operation, the voltages at both bit lines get pre charged to an equalized potential. When this particular memory cell is selected by asserting signal either BL or BLB will be discharged to the ground terminal via M5 and M6. As a result a small potential Difference appears at the bit lines. A sense amplifier detects this potential difference and amplifies it to a full swing signal at the bit lines. During the write operation, the data bit to be written gets transferred to BL whereas its complement gets transferred to BLB. When the cell is selected by WL, the access transistors will store the data bit in a latch formed by two cross coupled inverters. During hold operation, access transistors are turned off and the two cross coupled inverters holds the data as long as the power supply is applied.

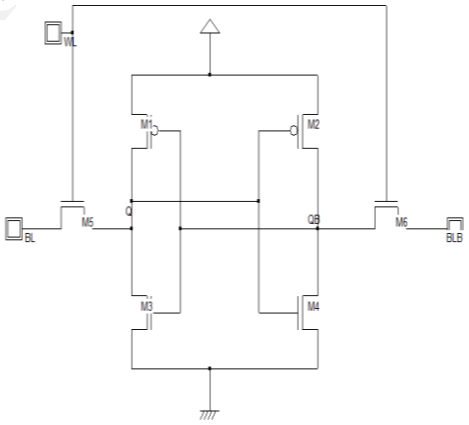

Figure 1: 6T SRAM cell

3. Schmitt Trigger

In the previously reported SRAM cell, the basic element for the data storage is a cross coupled inverter pair. Extra transistors are added to decouple the read and write operations. The cross coupled inverter pair of an SRAM cell operating at low supply voltage consumes high power. So to improve the inverter characteristics, Schmitt Trigger configuration is used. Schmitt trigger is like a comparator which include positive feedback. The output is high for an input is higher than a chosen threshold value. On the other hand the output is low for an input is higher than a chosen threshold value.

The output retains the value if the input between these two. The Schmitt circuit is a general inverter circuitry (double transistor inverter) with two extra transistors for providing the hysteresis [6].The Schmitt trigger circuit is shown in Figure 2 .The double transistor inverter is used because the transistors (M2 and M5) have some higher threshold voltage than M1 and M4 due to body bias effect and due to which the output switches to high from low or low from high when after the ON condition of M2 or M4 respectively. The addition of two more transistors M6 and M3 the circuit is capable to provide hysteresis. When 0 input voltage is applied at the input, both M1 andM2 are in OFF condition while M4 and M5 are in ON condition and output is at high logic level. When the input reaches to threshold voltage of M1 transistor then M1 will be on , while M2 remains OFF and at this time output will be high M3 will be on , so M1 Try to pull down the node between M1 and M2 while M3 try to pulls up this node to voltage VDD-VT , so transistor M2 stays the output to HIGH logic level , now when the input rises up to the threshold voltage of M2 then output switches to low logic level, so effectively our switching point shifted to higher voltage referred as VIH.A Schmitt trigger increases or decreases the switching threshold of the inverter depending upon the direction of input transition [7].This adaptation is achieved with the help of feedback mechanism.

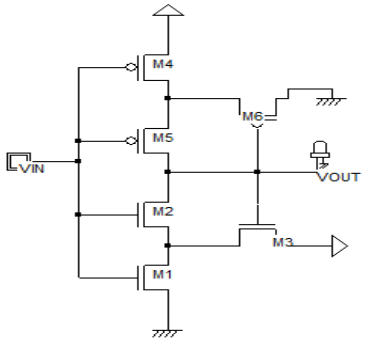

Figure 2: Conventional CMOS Schmitt Trigger

4. Proposed Schmitt Trigger

One possible implementation of a Schmitt trigger is shown in Figure 2.This structure is used to form the inverter of our memory bit cell. The basic Schmitt trigger requires six transistors instead of two transistors to form an inverter. Thus, it would need 14 transistors in total to form an SRAM cell, which would result in large area penalty. Since PMOS transistors are used as weak pull-ups to hold the "1" state, a feedback mechanism in the PMOS pull-up branch is not used. Feedback mechanism is used only in the pull-down path. The modified Schmitt trigger schematic is shown in Figure 3.In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in Figure 3. During 0 ->1 input transition, the feedback transistor (NF) tries to preserve the logic "1" at output (V_{out}) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a 0->1 input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. For the 1->0 input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read stability as well as write-ability of the SRAM bit cell.

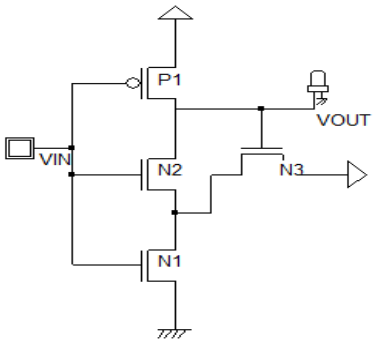

Figure 3: Proposed Schmitt Trigger

5. Schmitt Trigger Based SRAM Bit cell

The complete schematic for the proposed ST based SRAM bit cell is as shown in Figure 4. Transistors PL-NL1-NL2-NFL forms one ST inverter while PR-NR1-NR2-NFR forms another ST inverter. AXL and AXR are the access transistors. The positive feedback from NFL/NFR adaptively changes the switching threshold of the inverter depending on the direction of input transition. During a read operation (with say VL="0" and VR= VDD), due to voltage divider action between the access transistor and the pull-down NMOS, the voltage of VL node rises. If this voltage is higher than the switching threshold (trip point) of the other inverter, the contents of the cell can be flipped, resulting in a read failure event [8].In order to avoid a read failure, the feedback mechanism should increase the switching threshold of the inverter PR-NR1-NR2. Transistors NFR and NR2 raise the voltage at node VNR and increase the switching threshold of the inverter storing "1". Thus, Schmitt trigger action is used to preserve the logic "1" state of the memory cell [9]. The proposed ST based SRAM bit cell utilizes differential operation, giving better noise immunity. It requires no architectural change compared to the conventional 6T cell architecture and hence can be used as a drop-in replacement for the present 6T based designs.

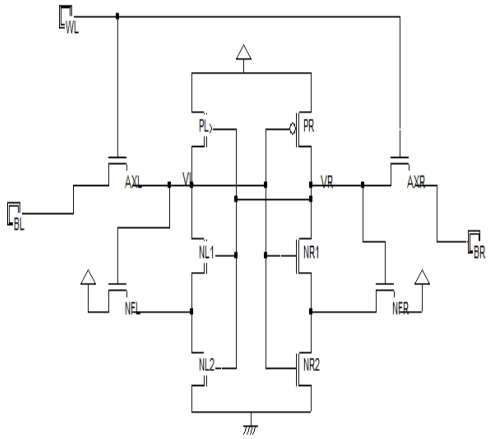

Figure 4: ST-1 bit cell schematic.

6. ST-2 Bit cell

Figure 5 shows the schematics of the ST-2 bit cell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bit lines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bit cell, feedback is provided by separate control signal (WL) unlike the ST-1 bit cell, where in feedback is provided by the internal nodes. In the ST-1 bit cell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback.

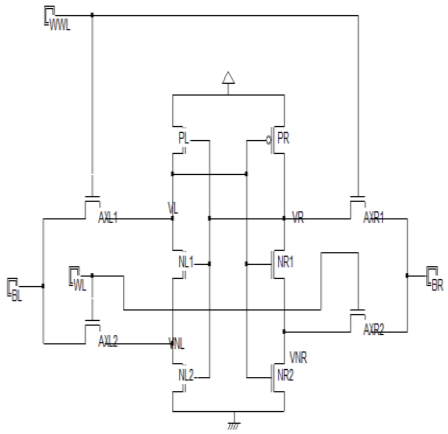

Figure 5: ST-2 bit cell schematic

When VL is increased from 0 to VDD, the other node (VR) makes a transition from VDD to 0. During this time, the feedback mechanism due to NFR-NR2 raises the node voltage VNR and tries to maintain the logic '1' state of the VR node. This gives a near ideal inverter characteristics essential for robust memory bit cell operation.

Table1: Mode of operation of ST-2 bit cell

Mode	WL	WWL
Read Mode	1	0
Write Mode	1	1
Hold Mode	0	0

6. Simulation Results

Simulations are done using MICROWIND6.2a Simulator. The 6T and the proposed ST based bit cells are compared for stability and Power. The Read failure problem in conventional 6T SRAM is flipping the data at the storage nodes due to leakage voltage during read operation. As shown in the Figure 1 during read operation the word line is asserted to low and both bit lines are pre charged to high. Initially BL=0 and BLB=1 and word line WL=1 So Q=0, QB=1. BL=1 that is applied as input for the inverter formed by M2, M4 output of that inverter at the node QB=0 and this is applied as an input for the inverter formed by M1, M3 so the data at the node Q=0 this differential data is taken as the output. But due to the voltage divider action between M6, M4 there is a possibility of producing some leakage voltage at the node QB. Due to scaling of the size of transistors the supply voltage and the threshold voltage are scale down. If the leakage voltage at the storage node QB crosses the threshold voltage of the inverter M1, M3 the data flipped at the storage nodes shown in the fig:6 When the WL=0 the data at the storage nodes should be stable but due to the voltage divider action the data is flipped shown in fig: 6 when BL=1 ,BLB=0 and WL=0 the output at the storage nodes will be VL=1,VR=0 but VL=1,VR=1 are appeared at the output.

In order to avoid this problem extra transistors are added to decouple the read port and write port so the probability of failure can be reduced. In this by adding the feedback transistors increase the switching threshold of the inverter. Initially WL=1 write operation takes place when the input data BL=0,BLB=1 are appeared at the storage nodes VL=0,VR=1 as shown in the Figure 7.

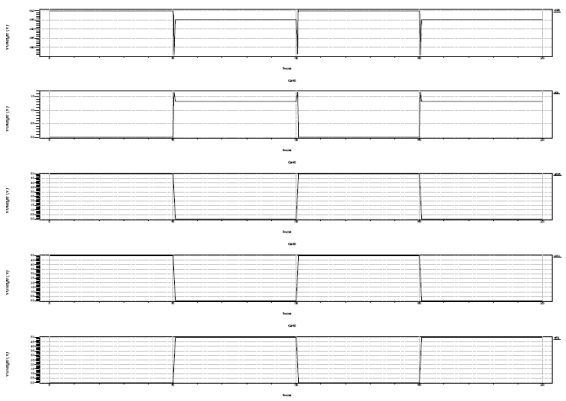

Figure 6: Simulation results of 6T SRAM

Similarly when the input data changes as BL=1, BLB=0 those are appeared at the storage nodes VL=1, VR=0. During read operation WL=0, even though the inputs changes the output doesn't change.

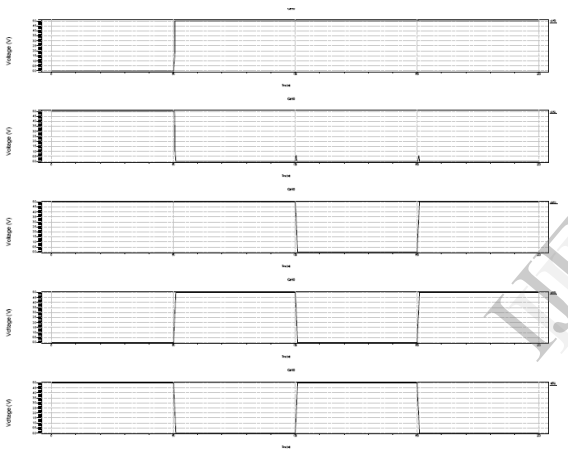

Figure 7: Simulation results of ST1 SRAM

In the ST-2 bit cell configuration two control signals WL, WWL are used to perform the read, write and hold operation as shown in the Table: 1. During write operation WL=1,WWL=1 the inputs BL=0,BLB=1,the output at the storage nodes VL=0,VR=1 as shown in Figure 8. in read operation WL=1,WWL=0 the output at the storage nodes maintains the same data VL=0,VR=1.Similarly hold mode WL=0,WWL=0 the output at the storage nodes maintains the same data VL=0,VR=1. Again When write operation occurs the output at the storage nodes VL=1, VR=0. But in this ST2 bit cell consumes lower leakage than the ST-1 bit cell. This is because, in the ST-2 bit cell, both feedback transistors are OFF in the hold mode unlike the ST-1 bit cell in which only one of the feedback transistors is OFF.

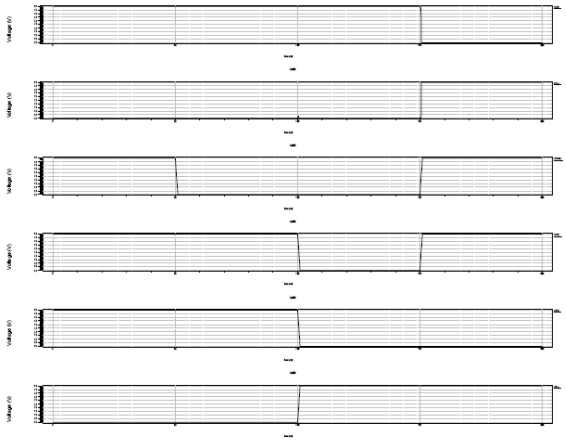

Figure 8: Simulation results of ST2 SRAM

In the 6T conventional SRAM cell Word line WL need to be high for both read and write operations and all transistors are working depends on input so the power consumption is more which is 0.192mW.But in the proposed method the power consumption is reduced to 0.988uW as shown in Table 2.

Table 2: Comparison between SRAM bit cells

SRAM Type	Power	Area
6T	0.192mw	81.6µm2
ST1	0.154mw	136.6µm2
ST2	0.988uw	154.2µm2

Conclusion

Several SRAM bit cells have been proposed having different design goals such as bit density, bit cell area, low voltage operation and architectural timing specifications. In all of the previously reported bit cells, 6T/7T/9T/10T the basic element for the data storage is a cross-coupled inverter pair. Extra transistors are added to decouple the read and write operations. None of the previously reported bit cells incorporate process variation tolerance for improving the stability of the cross coupled inverter pair of an SRAM bit cell operating at low supply voltage. For successful SRAM operation the stability of the cross-coupled inverter is important. Traditionally, device sizing has been adopted to mitigate the effect of process variations. However, device sizing is not effective in improving the bit cell stability at very low supply voltage. Hence, a different design approach for successful low voltage SRAM design in nano scaled technologies is

required. Proposed Schmitt Trigger based SRAM bit cell having built-in feedback mechanism that exhibits the process variation tolerance. It increases the stability of inverter pair by providing built-in feedback mechanism.

References

[1] H. Soeleman and K. Roy, Ultra-low power digital sub threshold logic circuits, *Proc. Int. Symp. Low Power Electronics and Design (ISLPED'98),* 1998, 94–96.

[2] K. Roy and S. Prasad, *Low Power CMOS VLSI Circuit Design* (New York: Wiley, 2000).

[3] N.Yoshinobu, H. Masahi, K. Takayuki and K. Itoh, Reviewand, future prospects of low-voltage RAM circuits, *IBM J. Res. Devel., vol. 47, no. 5/6,* 2003 525–552.

[4] A.Raychowdhury, S.Mukhopadhyay, and K. Roy, A feasibility study of subthreshold SRAM across technology generations, *in Proc. Int. Conf. Computer Design*, Oct. 2005, 417–422.

[5] K. Roy and K.S. Yeo, Low-voltage, low-power VLSI Subsystems (New Delhi: Tata McGraw-Hill International, 2009).

[6] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective* (2nd ed. Englewood Cliffs, NJ: Prentice Hall, 2002.)

[7] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. R. Montoye, L. Sekaric, S. McNab, W. Topol, C. Adams, K. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. Symp. VLSI Technol.*, 2005, pp. 128–129.

[8] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS, *IEEE Trans. Comput. Aided Des, vol. 24, no.12*, Dec. 2005 1859–1880.

[9] Jaydeep P. Kulkarn, Keejong Kim, and Kaushik Roy, A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM *IEEE Journal Of Solid-State Circuits, Vol. 42, No. 10,* October 2007.