Low-Power Mixed-Signal CVNS-Based Adder

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***Abstract*—In this paper, design of a mixed signal 64-bit adder based on continuous valued number system (CVNS) is presented. The CVNS is a novel number system based on signed continuous valued digits. The 64-bit adder is generated by cascading four 16-bit radix-2 CVNS adders. Arithmetic operation in this number system is performed using simple analog circuitry. The number system provides almost carry-free arithmetic structures with digit level redundancy. The adder takes advantage of high speed operation of analog signal processing units, while digital blocks have been used at the output of the adder to provide better driving capability. Truncated summation of the CVNS digits reduces the number of required interconnection in the system, reducing the complexity and hardware cost. On demand for media signal processing application, the adder can perform as a reconfigurable adder.**

***Index Terms*—Continuous valued number system (CVNS), analog digits, mixed signal adder, media signal processing, reconfigurable adder, current mode.**

I. INTRODUCTION

THE need for low-power and high-performance signal processing chips is increasing rapidly especially in the field of wireless communication and hand-held multimedia devices. Adder is an important and basic cell in most of the computational systems. Adder is usually the dominant factor in determining the overall performance of the system. The bottleneck of digital signal processing and digital systems is arithmetic blocks where addition and multiplication operations are the core units.

The Continuous Valued Number System (CVNS) representation can be a potential candidate for implementing area efficient and low power filters, since addition in this number system is almost carry-free [1]. The representation of CVNS in the original form is continuous in which the digits take a continuous value. The basic concepts of CVNS and analog digits are introduced in [2]-[3]. The number system is analog in nature and also can be applied for implementing low-power low-noise arithmetic units. Continuous Valued Number System can open up an alternative path in developing new types of arithmetic and signal processing units.

The CVNS is capable of performing arithmetic operations using analog circuitry in places where digital technology has been applied. However, special class of CVNS can interface with binary systems easily. This class of CVNS simplifies Binary to CVNS conversions and vice-versa and hence yields new architectures.

This paper discusses the design of low power mixed signal CVNS based 64-bit adder which internally uses CVNS representation and is implemented using mixed-signal circuits. The proposed adder does not generate carry information for individual output digit. This factor mainly reduces the number of interconnections in the system and hence reduces the area. This adder takes advantage of maximum reliable resolution of the implementation technology.

In Section II, fundamentals of CVNS are introduced. In this section general properties of CVNS for digit generation and addition are reviewed. In Section III, system design of the adder is presented. In Section IV, the design of 16 bit adder is presented. 64 bit adder is presented in section V. Analog circuitry is given in Section VI followed by the results in Section VII. The conclusion is given in section VIII.

II. CONTINUOUS VALUED NUMBER SYSTEM (CVNS)

CVNS is a novel number system based on signed continuous valued digits. This number system performs arithmetic operations by applying modular reduction operation on continuous real values using simple analog circuitry.

In this section general arithmetic features of the CVNS are introduced.

A. CVNS Digits

A value, x, from a positional number system with radix B within a boundary such that $|x| \leq M$, is mapped to set of CVNS digits, $((x))_i$, in radix-β. A CVNS value, ((x)), is an ensemble of the CVNS digits, $((x))_i$, and can be written as a vector as follows:

$$((x)) \rightarrow \{((x))_n, ((x))_{n-1}, \ldots, ((x))_0 | ((x))_{-1}, \ldots, ((x))_{-k}\} \quad (1)$$

Where $(-k \leq i \leq n)$ represents the indices of the CVNS digits, and the bar (|) represents the radix point. In the CVNS the digits are referred either by their indices or by the level of information they contain. The Parallel method applied to generate CVNS digits has the advantage of higher speed of operation and is called *Modular Reduction Digit Generation*.

TABLE I
RADIX-10 CVNS DIGITS OF AN ARBITRARY VALUE X=37.426 AND THEIR ASSOCIATED INTEGER VALUES

i	1	0	-1	-2	-3
$((x))_i$	3.7426	7.426	4.26	2.6	6
$[((x))_i]$	3	7	4	2	6

TABLE II
CVNS ADDITION BETWEEN TWO ARBITRARY VALUES

i	2	1	0	-1	-2
$((x))_i$	0.5834	5.834	8.34	3.4	4
$((y))_i$	0.7289	7.289	2.89	8.9	9
$((z))_i$	1.3123	3.123	1.23	2.3	3

TABLE III
ADDER OPERATION FOR DIFFERENT WORD LENGTHS, CONTROLLED BY *part 1* AND *part 2* SIGNALS

part1	*part2*	Adder Configuration
0	0	Byte(8-bit)
0	1	Half-Word (16-bit)
1	0	Word (32-bit)
1	1	Double-Word (64-bit)

The CVNS digits are obtained by applying a basic modular reduction operation as follows:

$$((x))_i = \left(\frac{x}{M} . \beta^{n-i+1}\right) mod\beta \qquad (2)$$

where $-k \le i \le n$, *mod* is the modulo operation on any continuous real value such that $(a)mod\beta = a+I.\beta$, where I is an integer and M is the maximum range of representation.

Each CVNS digit consists of two parts: an integer part and a non integer part.

Example: We are going to find radix-10 CVNS digits of a value x = 37.426. Maximum range of representation is considered as M = 100, Therefore the maximum and the minimum index value are n = 1 and k = 3 [2]. The CVNS digits of x = 37.426 and the associated integer values are shown in Table I.

B. *CVNS Addition*

The CVNS addition is by summation of digits without intercommunication and is almost carry free. CVNS addition is performed as follows:

$$((z))_i = (((x))_i + ((y))_i)mod\beta \qquad (3)$$

Example: CVNS addition of two arbitrary values x=58.34 and y=72.89 are shown in Table II. Maximum range of representation is considered M = 100 , n = 2, and k = 2.

The CVNS digits of ((z)) are {1.3123, 3.123, 1.23, 2.3, 3}, which is equivalent to z = 131.23 = 58.34 + 72.89.

III. SYSTEM LEVEL DESIGN OF 64-BIT ADDER

CVNS is a continuous number system and hence it is implemented using VLSI analog circuits. The 64-bit reconfigurable adder is divided into four 16-bit adders, and each adder is divided into four uniform blocks. The outputs and inputs are in binary form.

There are various modes of operation. To change the mode of operation of the 64-bit adder two signals are used namely: *part 1* and *part 2* as shown in Table III.

A 16-bit adder has to be partitioned in order to perform 8-bit operation. Here the control signal breaks down the size of each of the 16-bit adders to 8-bits. This mode of operation is controlled by a signal which is denoted as *ctrl8* and is generated as follows:

$$ctrl8 = (part1 \vee part2). \qquad (4)$$

To perform 32-bit addition two 16-bit adders are combined. The information is exchanged between the two adders, from less informed adder to the more informed adder. According to the Table II, *ctrl32* signal is equivalent to

$$ctrl32 = (part2' \wedge part1). \qquad (5)$$

When both *part1* and *part2* signals are made as one all four 16-bit adders are combined to work as 64-bit adder. Therefore control signals for these for these configurations are as follows:

$$ctrl64 = (part1 \wedge part2). \qquad (6)$$

On-demand these control signals are used to adjust the size and resolution of the adder. The mathematical analysis of each 16-bit adder is given in the next section and is also explained how the cascading of these adders resulted in a reconfigurable 64-bit adder.

IV. 16-BIT CVNS ADDER

The main operations required for the addition are: converting binary data to CVNS, adding CVNS digits and converting final results back to binary. Binary numbers are converted to CVNS representation using equation (2).

The radix of CVNS is chosen equal to 2 to simplify conversion from CVNS to binary representation.

A 16-bit binary value is represented as:

$$x = \sum_{i=0}^{15} x_i 2_i \qquad (7)$$

Relation between binary digits and CVNS representation can be obtained as:

$$((x))_j = \sum_{i=0}^{j} x_i 2^{i-j} \quad 0 \le j \le 15 \qquad (8)$$

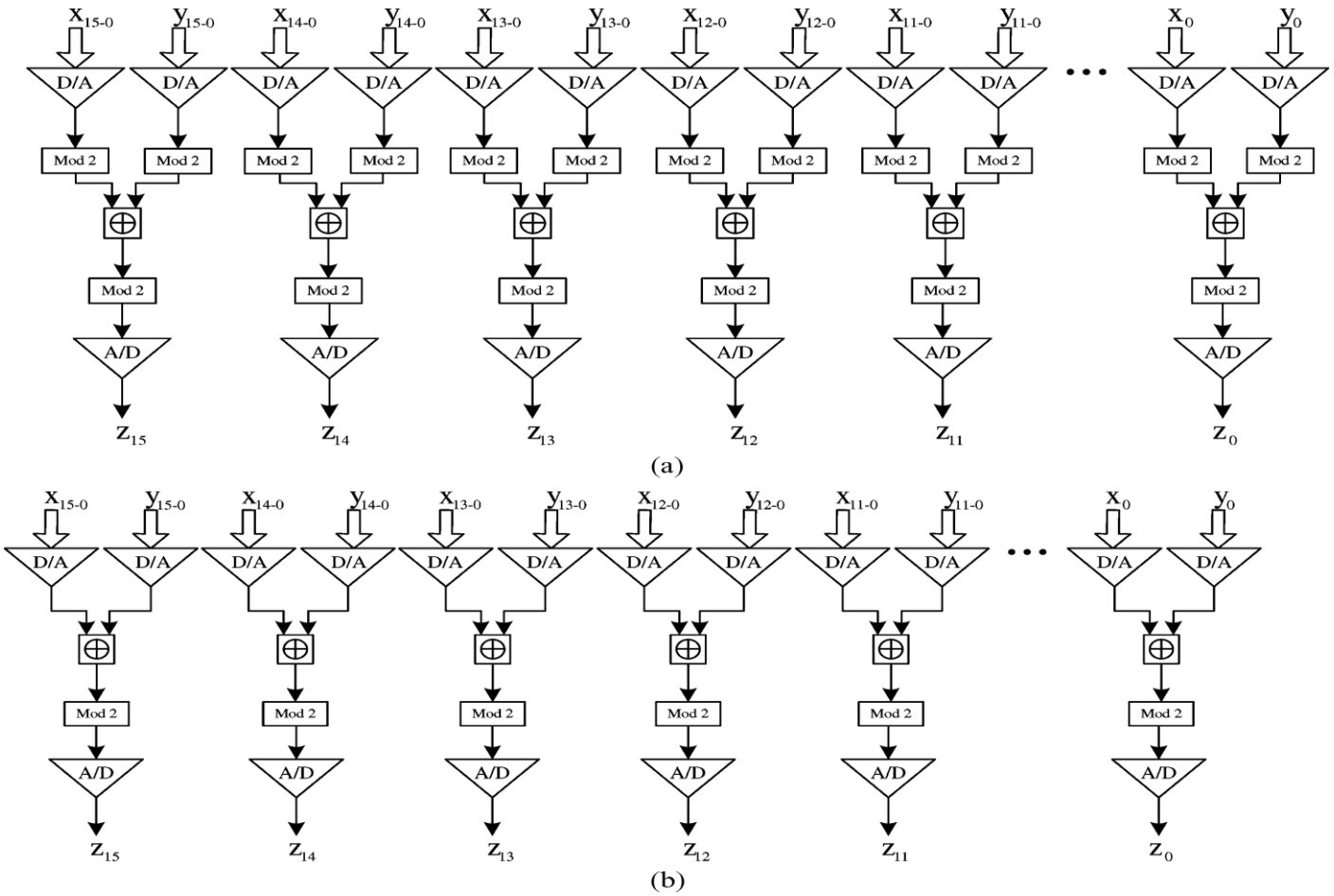

Fig. 1. Original form of CVNS Addition. (b) Improvements made by manipulating the mathematical analysis of CVNS addition, and eliminating one gate in the addition

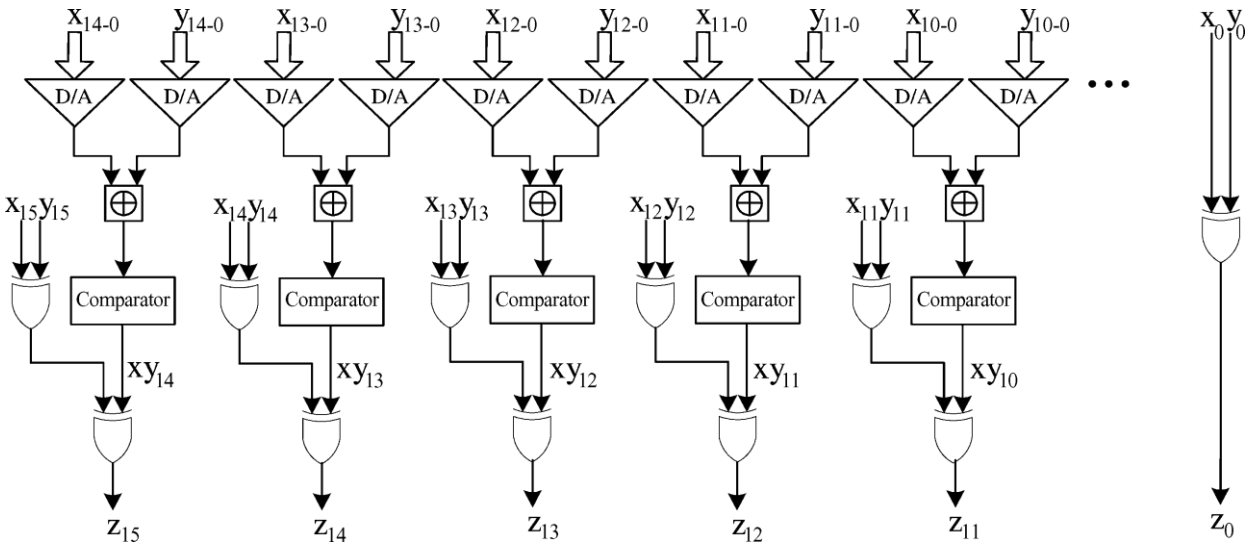

Fig. 2. Block level addition representation of mixed-signal CVNS.

The modular reduction operator can be eliminated since the above equation is pre congruent. Fig. 1 shows the block

level representation of the improvements made to the CVNS adder. Fig. 1(a) shows the original form of CVNS addition and Fig. 1(b) shows the improved block made by eliminating the modular reduction operator.

Two CVNS values ((x)) and ((y)) are summed as:

$$((z))_j = (((x))_i + ((y))_j = \sum_{i=0}^{j}(x_i + y_j)2^{i-j} mod 2 \qquad (9)$$

The term $((z))_j$ is in the CVNS form and it has to be converted to binary form [4].

For values of $((z))_j \in [0,1)$ binary digit z_j is equal to 0 and for of $((z))_j \in [1,2)$ binary digit z_j is equal to 1. At this stage, low radix of CVNS removes modular reduction operation (*mod2*) and combines CVNS to binary conversion by replacing with XOR and generates the binary outcome of the adder as:

$$z_j = x_j \oplus y_j \oplus x_{yj} \qquad (7)$$

where $\oplus$ denotes logical XOR function. Fig. 2 shows the block level representation of mixed signal CVNS adder.

To implement $((z))_j$, a high resolution analog environment equivalent to 16-bit is required. Hence the above equation can be changed to perform summation over a fixed sized group of bits of length 4.

Since mapping is based on uniform groups, only three different Tr signals are required. Fig. 3 shows the gate level design of each 16-bit adder.

The truncation signals are given by:

$$Tr_{t+4:t+7} = gt_{(1+t)} + rt_{(1+t)} Cin_{(t)} \qquad (8)$$

$$Tr_{t+8:t+11} = ctrl8.in_{8+t} + ctrl8'(gt_{(2+t)} + rt_{(2+t)} gt_{(1+t)} + rt_{(2+t)} rt_{(1+t)} Cin_t) \qquad (9)$$

$$Tr_{t+12:t+15} = gt_{(3+t)} + rt_{3+t} Tr_{t+8:t+11} \qquad (10)$$

where gt and rt signals are:

$$gt_k = \begin{cases} 1 \; if \; \sum_{i=4k}^{4k-1}(x_i + y_i)2^{i-4k+1} \geq 2 \\ 0 \qquad otherwise \end{cases} \qquad (11)$$

and

$$rt_k = \begin{cases} 1 \; if \; \sum_{i=4k}^{4k-1}(x_i + y_i)2^{i-4k+1} \geq 1.825 \\ 0 \qquad otherwise \end{cases} \qquad (12)$$

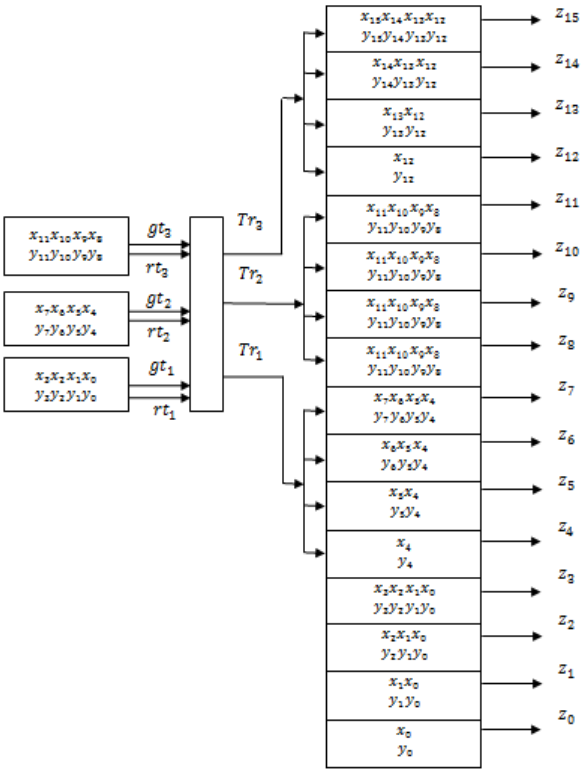

Fig. 3. Gate level design of each 16-bit adder

The three truncation signals are the only signals that are passed from the second layer to the third. The CVNS addition is performed in three main stages: first evaluation of gt and rt signals from each group of input digits, secondly, combining data of gt and rt to generate truncation signals and finally to evaluate the final results and convert the data back to binary.

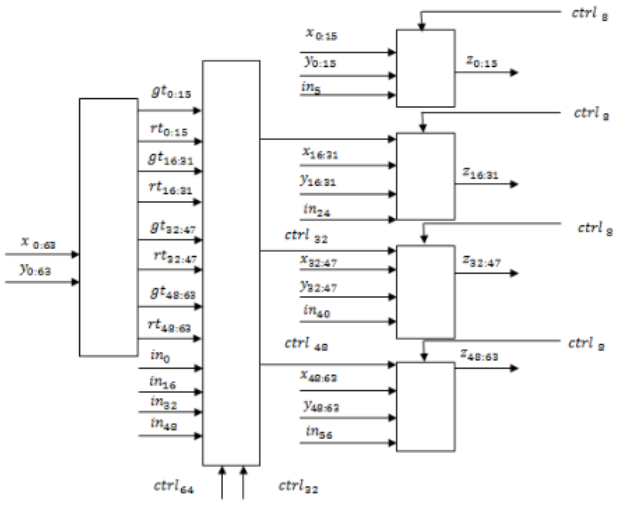

Fig. 4. General Configuration of the 64-bit adder

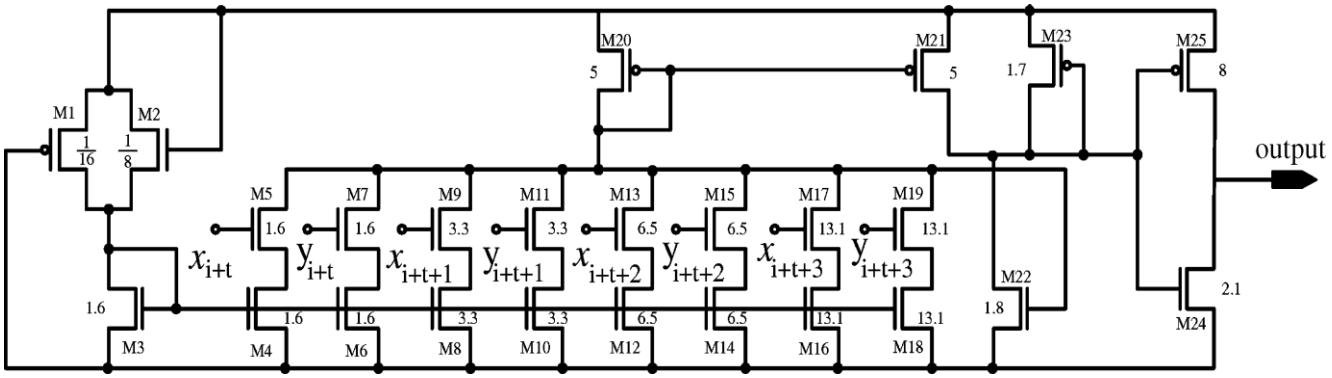

Fig. 5. Modular reduction circuit, and additional operations including binary to the CVNS conversion and current mode CVNS addition.

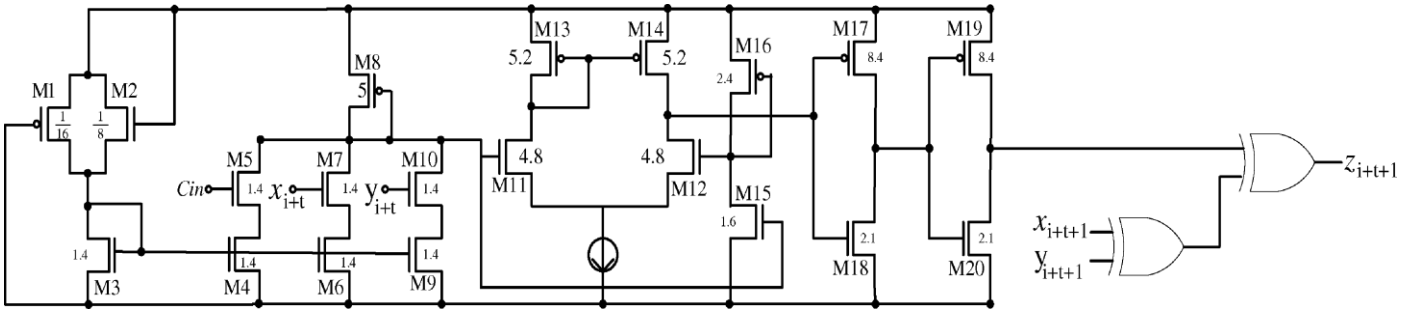

Fig. 6. Mixed-signal gate used of revaluating the summation of two CVNS digits

V. 64-BIT CVNS ADDER

The reconfigurable 64-bit adder is generated by cascading four 16-bit radix-2 CVNS adders. This CVNS adder has unique design and hence it is suitable for media processing and SoC applications. In this adder, information is generated locally for addition; hence the number of required inter-connections is reduced. The carries out of each 16-bit adder are the only global information. Fig. 4 shows the general configuration of 64-bit adder.

VI. CURRENT MODE CIRCUITS

The CVNS adder is implemented using differential style analog circuits. Circuit operations are in current mode to achieve low-noise, high-speed and low-power adder.

The gate used for generating gt and rt signals is shown in Fig. 5. Binary digits in groups of length 4 are converted into analog values using current mode digital-to-analog converter (DAC). The comparator threshold is data dependent; data is compared with its complement value (1.875-i). The output of the comparator goes high when the added current is higher than 2 or 1.875 for generating gt and rt signals respectively. The power consumption is static and is directly related to the biasing current [5].

Fig. 6 shows the schematic of the circuit which performs digital to CVNS conversion, CVNS addition in form of adding two currents, and evaluating the binary output. Fig. 7 shows the schematic of the XOR gate which is used at the output and it is a simple design of 6 transistors. Fig. 8 shows the gate for generating the truncation signal within the 16-bit adder along with the control signal *ctrl8*.

When the signal is LOW, the adder operates in normal mode and when the signal is HIGH, it indicates that the adder has to be broken down to 8-bit.

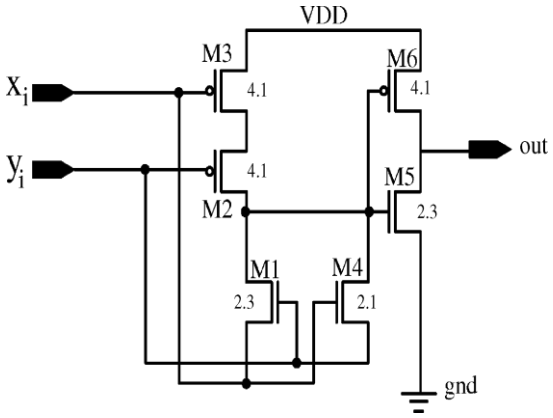

Fig. 7. XOR gate used for generating the output binary digit.

The proposed CVNS adder has been implemented in TSMC CMOS 90nm technology. One of the advantages of CVNS adder is that the information is carried by a few interconnections and the layout of the adder can be very

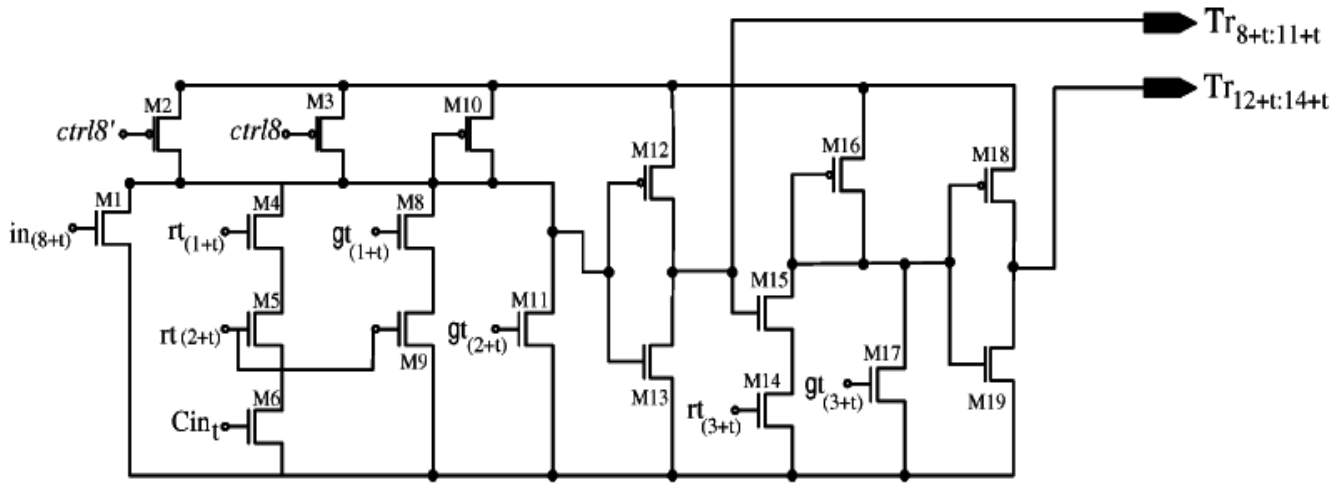

Fig. 8.Module for generating the truncation signal to the more informed bit

compact and hence the required area is low. The area can be reduced if CVNS radix was chosen a value higher than 2, such as 4 or 8.

VII. RESULTS

Cadence analysis tools are used for simulating and to synthesize RTL schematic diagram for the 64-bit addition. The efficiency of the adders is not only evaluated in terms of worst case delay, power consumption or area, but also by power delay product [6]. The CVNS power consumption stays almost the same regardless of the fan-in and fan-out and the frequency of the adder. The reduction in area of the CVNS is due to the fact that operations are in current-mode.

VIII. CONCLUSIONS

Design and implementation of a mixed signal 64bit adder based on CVNS is demonstrated in this paper. The CVNS adder is implemented using Cadence Software. CVNS with high speed analog circuit opens up a new path for performing signal processing tasks, in places where traditionally digital logic has been employed. The proposed adder has low power dissipation. After synthesis, lower area consumption in case of 90nm than 180nm can be observed. The new mixed-signal configuration can eliminate the modular reduction. Moreover, output conversion gate was integrated within the addition gate for further reduction in area of arithmetic unit. In this design, carry information is generated locally for each block. This property reduces the design complexity and allows us to easily partition the adder on demand and make it suitable for media signal processing.

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